



BSS138

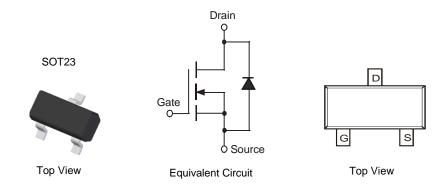
N-CHANNEL ENHANCEMENT MODE MOSFET

Features

- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability
- PPAP Capable (Note 4)

Mechanical Data

- Case: SOT23
- Case Material: Molded Plastic. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Matte Tin Finish Annealed over Alloy 42 Leadframe (Lead Free Plating). Solderable per MIL-STD-202, Method 208 (3)
- Terminal Connections: See Diagram
- Weight: 0.008 grams (Approximate)



Ordering Information (Note 5)

Part Number	Qualification	Case	Packaging
BSS138-7-F	Commercial	SOT23	3000/Tape & Reel
BSS138-13-F	Commercial	SOT23	10000/Tape & Reel
BSS138Q-7-F	Automotive	SOT23	3000/Tape & Reel

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant

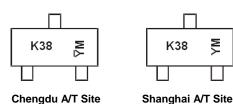
 See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.

3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

4. Automotive products are AEC-Q101 qualified and are PPAP capable. Automotive, AEC-Q101 and standard products are electrically and thermally the same, except where specified. For more information, please refer to http://www.diodes.com/product_compliance_definitions.html.

5. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/

Marking Information



 $\begin{array}{l} \mathsf{K38}=\mathsf{Product Type Marking Code} \\ \mathsf{YM}=\mathsf{Date Code Marking for SAT (Shanghai Assembly/ Test Site)} \\ \overline{\mathsf{YM}}=\mathsf{Date Code Marking for CAT (Chengdu Assembly/ Test Site)} \\ \mathsf{Y} \text{ or } \overline{\mathsf{Y}}=\mathsf{Year (ex: E=2017)} \\ \mathsf{M}=\mathsf{Month (ex: 9=September)} \end{array}$

Date Code Key

Date Obuc Rey															
Year	1998	1999	2000		2002	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025
Code	J	K	L		Ν	D	Е	F	G	Н	I	J	K	L	М
Month	Jan	Fe	b	Mar	Apr	May	Ju	n	Jul	Aug	Sep	Oc	t I	Nov	Dec
Code	1	2		3	4	5	6		7	8	9	0		Ν	D

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Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	50	V
Drain-Gate Voltage $R_{GS} \le 20 K\Omega$	V _{DGR}	50	V
Gate-Source Voltage Continuous	N	±20	V
Gate-Source Voltage Non Repetitive, Pulse Width<50µs	V _{GSS}	±40	V
Drain Current Continuous	I _D	200	mA
Pulsed Drain Current (10µs Pulse Duty Cycle = 1%)	I _{DM}	1	А

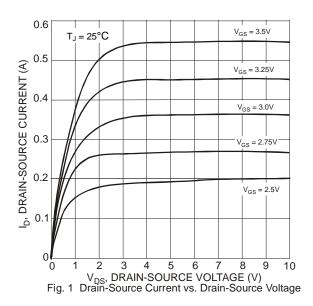
Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

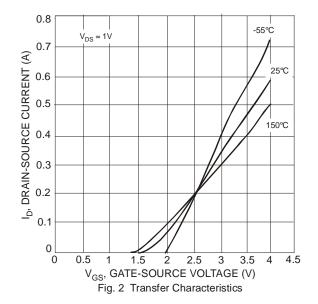
Characteristic	Symbol	Value	Unit
Power Dissipation (Note 6)	PD	300	mW
Thermal Resistance, Junction to Ambient (Note 6)	R ₀ JA	417	°C/W
Operating and Storage Temperature Range	TJ, T _{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

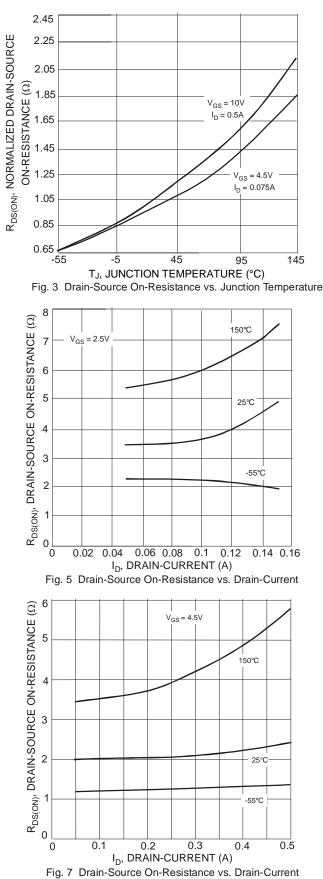
Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 7)						·	
Drain-Source Breakdown Voltage	BV _{DSS}	50	75		V	$V_{GS} = 0V, I_D = 250 \mu A$	
Zero Gate Voltage Drain Current	IDSS			0.5	μA	$V_{DS} = 50V, V_{GS} = 0V$	
Gate-Body Leakage	I _{GSS}	_		±100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 7)						·	
Gate Threshold Voltage	V _{GS(TH)}	0.5	1.2	1.5	V	$V_{DS} = V_{GS}, I_D = 250 \mu A$	
Static Drain-Source On-Resistance	R _{DS(ON)}	_	1.4	3.5	Ω	$V_{GS} = 10V, I_D = 0.22A$	
Forward Transconductance	g fs	100		_	mS	V _{DS} = 25V, I _D = 0.2A, f = 1.0KHz	
DYNAMIC CHARACTERISTICS						·	
Input Capacitance	Ciss			50	pF		
Output Capacitance	Coss	_		25	pF	V _{DS} = 10V, V _{GS} = 0V, f = 1.0MHz	
Reverse Transfer Capacitance	C _{rss}	_		8.0	pF	1	
SWITCHING CHARACTERISTICS							
Turn-On Delay Time	t _{D(ON)}			20	ns	V 20V I 0.24 P 500	
Turn-Off Delay Time	tD(OFF)	_		20	ns	$V_{DD} = 30V, I_D = 0.2A, R_{GEN} = 509$	

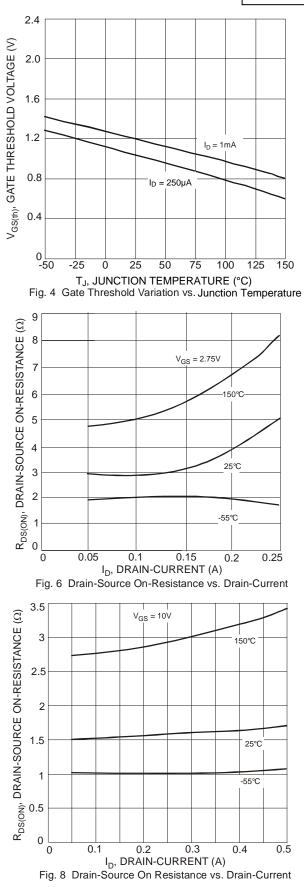
 Device mounted on FR-4 PCB 1.0 x 0.75 x 0.062 inch pad layout as shown on Diodes Incorporated's suggested pad layout, which can be found on our website at http://www.diodes.com/package-outlines.html.
Short duration pulse test used to minimize self-heating effect. Notes:





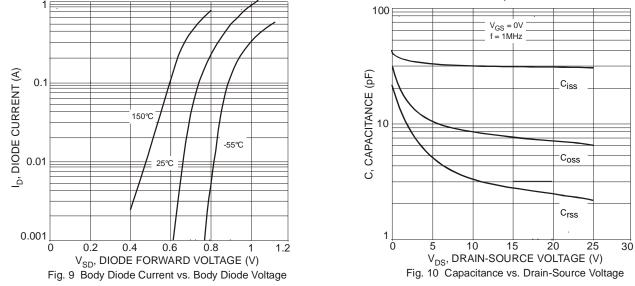






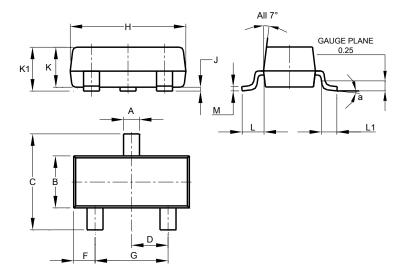


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Package Outline Dimensions

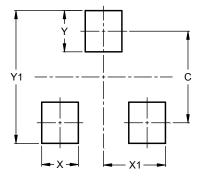
Please see http://www.diodes.com/package-outlines.html for the latest version.



SOT23							
Dim	Min	Min Max					
Α	0.37	0.51	0.40				
в	1.20	1.40	1.30				
С	2.30	2.50	2.40				
D	0.89	1.03	0.915				
F	0.45	0.60	0.535				
G	1.78	2.05	1.83				
H	2.80	3.00	2.90				
J	0.013	0.10	0.05				
К	0.890	1.00	0.975				
K1	0.903	1.025					
L	0.45	0.61	0.55				
L1	0.25	0.55	0.40				
Μ	0.085	0.150	0.110				
а	0°	8°					
All	All Dimensions in mm						

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.



Dimensions	Value (in mm)				
С	2.0				
Х	0.8				
X1	1.35				
Y	0.9				
Y1	2.9				



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