
LOW-VOLTAGE AND LOW-POWER STEREO AUDIO DIGITAL-TO-ANALOG CONVERTER WITH HEADPHONE AMPLIFIER

FEATURES

- Multilevel DAC Including Headphone Amplifier
- Analog Performance (V_{CC} , $V_{HP} = 2.4$ V):
 - Dynamic Range: 98 dB Typ
 - THD+N at 0 dB: 0.1% Typ
 - THD+N at –20 dB: 0.04% Typ
 - Output Power at $R_L = 16 \Omega$: 13 mW (Stereo), 26 mW (Monaural)
- 1.6-V to 3.6-V Single Power Supply
- Low Power Dissipation: 6.5 mW at V_{CC} , $V_{HP} = 2.4$ V
- System Clock: 128 f_S , 192 f_S , 256 f_S , 384 f_S
- Sampling Frequency: 5 kHz to 50 kHz
- Software Control (PCM1770):
 - 16-, 20-, 24-Bit Word Available
 - Left-, Right-Justified, and I²S
 - Slave/Master Selectable
 - Digital Attenuation: 0 dB to –62 dB, 1 dB/Step
 - 44.1-kHz Digital De-Emphasis
 - Zero Cross Attenuation
 - Digital Soft Mute
 - Monaural Analog-In With Mixing
 - Monaural Speaker Mode
- Hardware Control (PCM1771):
 - Left-Justified and I²S
 - 44.1-kHz Digital De-Emphasis
 - Monaural Analog-In With Mixing
- Pop-Noise-Free Circuit
- 3.3-V Tolerant
- Packages: TSSOP-16 and VQFN-20

APPLICATIONS

- Portable Audio Player
- Cellular Phone
- PDA
- Other Applications Requiring Low-Voltage Operation

DESCRIPTION

The PCM1770 and PCM1771 devices are CMOS, monolithic, integrated circuits which include stereo digital-to-analog converters, headphone circuitry, and support circuitry in small TSSOP-16 and VQFN-20 packages.

The data converters use TI's enhanced multilevel Δ - Σ architecture, which employs noise shaping and multilevel amplitude quantization to achieve excellent dynamic performance and improved tolerance to clock jitter. The PCM1770 and PCM1771 devices accept several industry standard audio data formats with 16- to 24-bit data, left-justified, I²S, etc., providing easy interfacing to audio DSP and decoder devices. Sampling rates up to 50 kHz are supported. A full set of user-programmable functions is accessible through a 3-wire serial control port, which supports register write functions.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted⁽¹⁾

| | PCM1770 PCM1771 |
|---|--------------------|
| Supply voltage: V_{CC} , V_{HP} | –0.3 V to 4 V |
| Supply voltage differences: V_{CC} , V_{HP} | ±0.1 V |
| Ground voltage differences | ±0.1 V |
| Digital input voltage | –0.3 V to 4 V |
| Input current (any terminals except supplies) | ±10 mA |
| Operating temperature | –40°C to 125°C |
| Storage temperature | –55°C to 150°C |
| Junction temperature | 150°C |
| Lead temperature (soldering) | 260°C, 5 s |
| Package temperature (IR reflow, peak) | 260°C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range

| | MIN | NOM | MAX | UNIT |
|--|----------------|------|------|------|
| Supply voltage: V_{CC} , V_{HP} | 1.6 | 2.4 | 3.6 | V |
| Digital input logic family | CMOS | | | |
| Digital input clock frequency | System clock | 0.64 | 19.2 | MHz |
| | Sampling clock | 5 | 50 | kHz |
| Analog output load resistance | 16 | | | Ω |
| Analog input level ($V_{HP} = 2.4$ V) | | | 1.4 | Vp-p |
| Operating free-air temperature, T_A | –25 | | 85 | °C |

ELECTRICAL CHARACTERISTICS

 all specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = V_{HP} = 2.4\text{ V}$, $f_S = 44.1\text{ kHz}$, system clock = $256 f_S$ and 24-bit data, $R_L = 16\ \Omega$, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | PCM1770PW, PCM1771PW, PCM1770RGA, PCM1771RGA | | | UNIT |
|---|-----------------------------------|---------------------------------------|---|----------|-----|---------------|
| | | | MIN | TYP | MAX | |
| Resolution | | | 24 | | | Bits |
| OPERATING FREQUENCY | | | | | | |
| Sampling frequency (f_S) | | | 5 | | 50 | kHz |
| System clock frequency | | | 128f _S , 192f _S , 256f _S , 384f _S | | | |
| DIGITAL INPUT/OUTPUT⁽¹⁾⁽²⁾ | | | | | | |
| Logic family | | CMOS compatible | | | | |
| V_{IH} | Input logic level | | 0.7 V_{CC} | | | VDC |
| V_{IL} | | | 0.3 V_{CC} | | | VDC |
| I_{IH} | Input logic current | $V_{IN} = V_{CC}$ | 10 | | | μA |
| I_{IL} | | $V_{IN} = 0\text{ V}$ | -10 | | | μA |
| V_{OH} | Output logic level ⁽³⁾ | $I_{OH} = -2\text{ mA}$ | 0.7 V_{CC} | | | VDC |
| V_{OL} | | $I_{OL} = 2\text{ mA}$ | 0.3 V_{CC} | | | VDC |
| DYNAMIC PERFORMANCE (HEADPHONE OUTPUT) | | | | | | |
| Full-scale output voltage | | 0 dB | 0.55 V_{HP} | | | Vp-p |
| Dynamic range | | EIAJ, A-weighted | 90 | 98 | | dB |
| Signal-to-noise ratio | | EIAJ, A-weighted | 90 | 98 | | dB |
| THD+N | Total harmonic distortion + noise | 0 dB (13 mW) | 0.1% | | | |
| | | -20 dB (0.1 mW) | 0.04% | 0.1% | | |
| Output power | | Stereo | 10 | 13 | | mWrms |
| | | Monaural | 20 | 26 | | mWrms |
| Channel separation | | | 64 | 72 | | dB |
| Load resistance | | | 14 | 16 | | Ω |
| DC ACCURACY | | | | | | |
| Gain error | | | ± 2 | ± 8 | | %FSR |
| Gain mismatch, channel-to-channel | | | ± 2 | ± 8 | | %FSR |
| Bipolar zero error | | $V_{OUT} = 0.5 V_{CC}$ at BPZ | ± 30 | ± 75 | | mV |
| ANALOG LINE INPUT (MIXING CIRCUIT) | | | | | | |
| Analog input voltage range | | | 0.584 V_{HP} | | | Vp-p |
| Gain (analog input to headphone output) | | | 0.67 | | | |
| Analog input impedance | | | 10 | | | k Ω |
| THD+N | Total harmonic distortion + noise | $A_{IN} = 0.56 V_{HP}$ (peak-to-peak) | 0.1% | | | |
| DIGITAL FILTER PERFORMANCE | | | | | | |
| Pass band | | | 0.454 f_S | | | |
| Stop band | | | 0.546 f_S | | | |
| Pass-band ripple | | | ± 0.04 | | | dB |
| Stop-band attenuation | | | -50 | | | dB |
| Group delay | | | 20/ f_S | | | |
| 44.1-kHz de-emphasis error | | | ± 0.1 | | | dB |
| ANALOG FILTER PERFORMANCE | | | | | | |

(1) Digital inputs and outputs are CMOS compatible.

(2) All logic inputs are 3.3-V tolerant and not terminated internally.

(3) LRCK and BCK terminals

ELECTRICAL CHARACTERISTICS (continued)

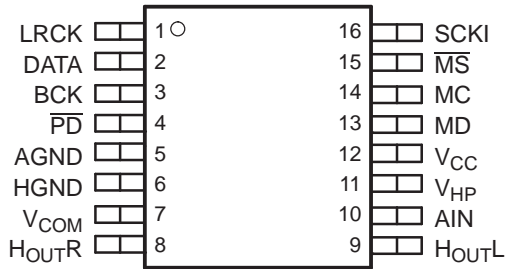
all specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = V_{HP} = 2.4\text{ V}$, $f_S = 44.1\text{ kHz}$, system clock = $256 f_S$ and 24-bit data, $R_L = 16\ \Omega$, unless otherwise noted

| PARAMETER | TEST CONDITIONS | PCM1770PW, PCM1771PW, PCM1770RGA, PCM1771RGA | | | UNIT |
|------------------------------------|--------------------|---|-----------|-----|--------------------|
| | | MIN | TYP | MAX | |
| Frequency response | at 20 kHz | | ± 0.2 | | dB |
| POWER SUPPLY REQUIREMENTS | | | | | |
| Voltage range, V_{CC} , V_{HP} | | 1.6 | 2.4 | 3.6 | VDC |
| I_{CC} | Supply current | BPZ input | 1.5 | 2.5 | mA |
| I_{HP} | | BPZ input | 1.2 | 2.5 | |
| $I_{CC} + I_{HP}$ | | Power down ⁽⁴⁾ | | 5 | 15 |
| Power dissipation | | BPZ input | 6.5 | 12 | mW |
| | | Power down ⁽⁴⁾ | 12 | 36 | μW |
| TEMPERATURE RANGE | | | | | |
| Operation temperature | | -25 | | 85 | $^\circ\text{C}$ |
| θ_{JA} | Thermal resistance | PCM1770PW, -71PW: 16-terminal TSSOP | 150 | | $^\circ\text{C/W}$ |
| | | PCM1770RGA, -71RGA: 20-terminal VQFN | 130 | | |

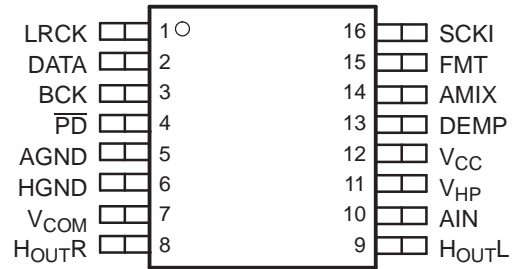
(4) All input signals are held static.

PIN ASSIGNMENTS

**PCM1770
PW PACKAGE
(TOP VIEW)**

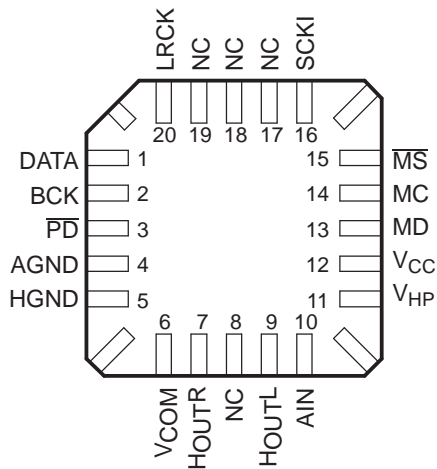


**PCM1771
PW PACKAGE
(TOP VIEW)**



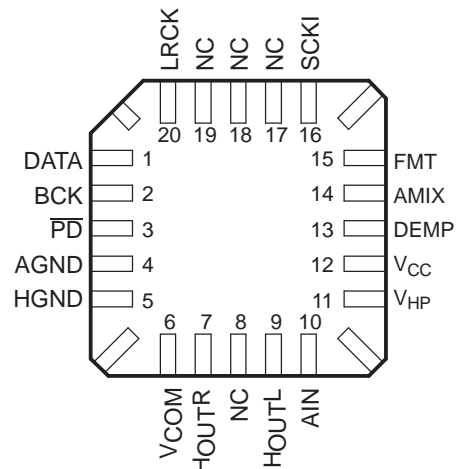
P0001-02

**PCM1770
RGA PACKAGE
(TOP VIEW)**



NC – No internal connection

**PCM1771
RGA PACKAGE
(TOP VIEW)**



P0002-02

TERMINAL FUNCTIONS
PCM1770PW

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|-------------------|-----|-----|---|
| AGND | 5 | – | Analog ground. This is a return for V_{CC} . |
| AIN | 10 | I | Monaural analog signal mixer input. The signal can be mixed with the outputs of the L- and R-channel DACs. |
| BCK | 3 | I/O | Serial bit clock. Clocks the individual bits of the audio data input, DATA. In the slave interface mode, this clock is input from an external device. In the master interface mode, the PCM1770 device generates the BCK output to an external device. |
| DATA | 2 | I | Serial audio data input |
| HGND | 6 | – | Analog ground. This is a return for V_{HP} . |
| H _{OUTL} | 9 | O | L-channel analog signal output of the headphone amplifiers |
| H _{OUTR} | 8 | O | R-channel analog signal output of the headphone amplifiers |
| LRCK | 1 | I/O | Left and right clock. Determines which channel is being input on the audio data input, DATA. The frequency of LRCK must be the same as the audio sampling rate. In the slave interface mode, this clock is input from an external device. In the master interface mode, the PCM1770 device generates the LRCK output to an external device. |
| MC | 14 | I | Mode control port serial bit clock input. Clocks the individual bits of the control data input, MD. |
| MD | 13 | I | Mode control port serial data input. Controls the operation mode on the PCM1770 device. |
| \overline{MS} | 15 | I | Mode control port select. The control port is active when this terminal is low. |
| \overline{PD} | 4 | I | Reset input. When low, the PCM1770 device is powered down, and all mode control registers are reset to default settings. |
| SCKI | 16 | I | System clock input |
| V_{CC} | 12 | – | Power supply for all analog circuits except the headphone amplifier. |
| V_{COM} | 7 | – | Decoupling capacitor connection. An external 10- μ F capacitor connected from this terminal to analog ground is required for noise filtering. Voltage level of this terminal is 0.5 V_{HP} nominal. |
| V_{HP} | 11 | – | Analog power supply for the headphone amplifier circuits. The voltage level must be the same as V_{CC} . |

TERMINAL FUNCTIONS (CONTINUED)
PCM1770RGA

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|-------------------|------------------|-----|---|
| AGND | 4 | – | Analog ground. This is a return for V_{CC} . |
| AIN | 10 | I | Monaural analog signal mixer input. The signal can be mixed with the outputs of the L- and R-channel DACs. |
| BCK | 2 | I/O | Serial bit clock. Clocks the individual bits of the audio data input, DATA. In the slave interface mode, this clock is input from an external device. In the master interface mode, the PCM1770 device generates the BCK output to an external device. |
| DATA | 1 | I | Serial audio data input |
| HGND | 5 | – | Analog ground. This is a return for V_{HP} . |
| H _{OUTL} | 9 | O | L-channel analog signal output of the headphone amplifiers |
| H _{OUTR} | 7 | O | R-channel analog signal output of the headphone amplifiers |
| LRCK | 20 | I/O | Left and right clock. Determines which channel is being input on the audio data input, DATA. The frequency of LRCK must be the same as the audio sampling rate. In the slave interface mode, this clock is input from an external device. In the master interface mode, the PCM1770 device generates the LRCK output to an external device. |
| MC | 14 | I | Mode control port serial bit clock input. Clocks the individual bits of the control data input, MD. |
| MD | 13 | I | Mode control port serial data input. Controls the operation mode on the PCM1770 device. |
| \overline{MS} | 15 | I | Mode control port select. The control port is active when this terminal is low. |
| NC | 8, 17, 18, 19 | – | No connect |
| \overline{PD} | 3 | I | Reset input. When low, the PCM1770 device is powered down, and all mode control registers are reset to default settings. |
| SCKI | 16 | I | System clock input |
| V_{CC} | 12 | – | Power supply for all analog circuits except the headphone amplifier. |
| V_{COM} | 6 | – | Decoupling capacitor connection. An external 10- μ F capacitor connected from this terminal to analog ground is required for noise filtering. Voltage level of this terminal is 0.5 V_{HP} nominal. |
| V_{HP} | 11 | – | Analog power supply for the headphone amplifier circuits. The voltage level must be the same as V_{CC} . |

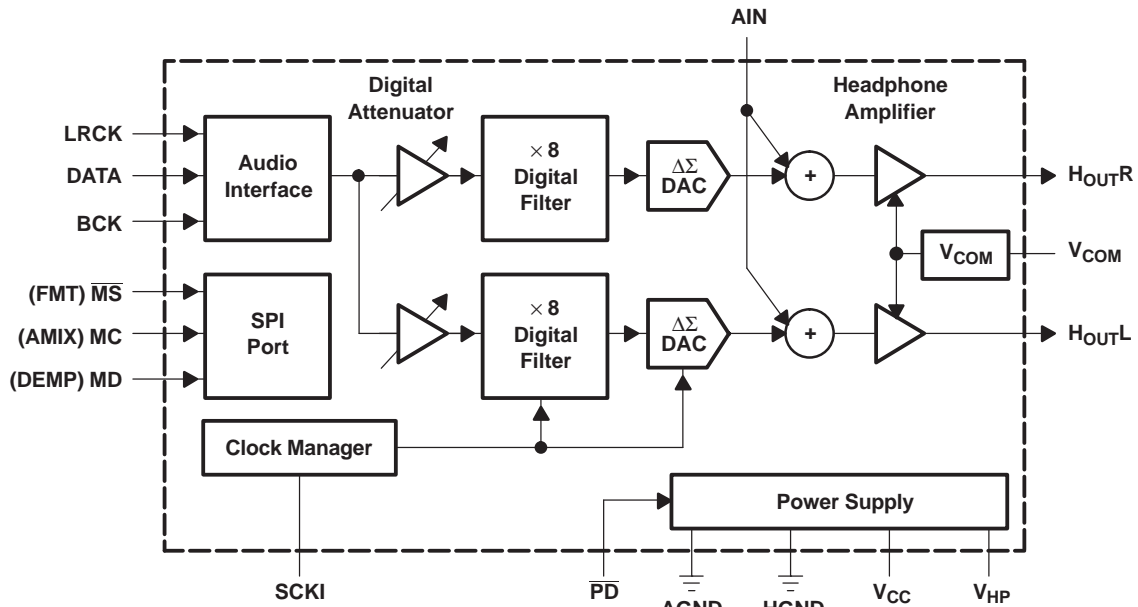
TERMINAL FUNCTIONS (CONTINUED)**PCM1771PW**

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|-------------------|-----|-----|---|
| AGND | 5 | – | Analog ground. This is a return for V_{CC} . |
| AIN | 10 | – | Monaural analog signal mixer input. The signal can be mixed with the outputs of the L- and R-channel DACs. |
| AMIX | 14 | I | Analog mixing control |
| BCK | 3 | I | Serial bit clock. Clocks the individual bits of the audio data input, DATA. |
| DATA | 2 | I | Serial audio data input |
| DEMP | 13 | I | De-emphasis control |
| FMT | 15 | I | Data format select |
| HGND | 6 | – | Analog ground. This is a return for V_{HP} . |
| H _{OUTL} | 9 | O | L-channel analog signal output of the headphone amplifiers |
| H _{OUTR} | 8 | O | R-channel analog signal output of the headphone amplifiers |
| LRCK | 1 | I | Left and right clock. Determines which channel is being input on the audio data input, DATA. The frequency of LRCK must be the same as the audio sampling rate. |
| \overline{PD} | 4 | I | Reset input. When low, the PCM1771 device is powered down, and all mode control registers are reset to default settings. |
| SCKI | 16 | I | System clock input |
| V_{CC} | 12 | – | Power supply for all analog circuits except the headphone amplifier. |
| V_{COM} | 7 | – | Decoupling capacitor connection. An external 10- μ F capacitor connected from this terminal to analog ground is required for noise filtering. Voltage level of this terminal is 0.5 V_{HP} nominal. |
| V_{HP} | 11 | – | Analog power supply for the headphone amplifier circuits. The voltage level must be the same as V_{CC} . |

PCM1771RGA

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|-------------------|------------------|-----|---|
| AGND | 4 | – | Analog ground. This is a return for V_{CC} . |
| AIN | 10 | – | Monaural analog signal mixer input. The signal can be mixed with the outputs of the L- and R-channel DACs. |
| AMIX | 14 | I | Analog mixing control |
| BCK | 2 | I | Serial bit clock. Clocks the individual bits of the audio data input, DATA. |
| DATA | 1 | I | Serial audio data input |
| DEMP | 13 | I | De-emphasis control |
| FMT | 15 | I | Data format select |
| HGND | 5 | – | Analog ground. This is a return for V_{HP} . |
| H _{OUTL} | 9 | O | L-channel analog signal output of the headphone amplifiers |
| H _{OUTR} | 7 | O | R-channel analog signal output of the headphone amplifiers |
| LRCK | 20 | I | Left and right clock. Determines which channel is being input on the audio data input, DATA. The frequency of LRCK must be the same as the audio sampling rate. |
| NC | 8, 17, 18, 19 | – | No connect |
| \overline{PD} | 3 | I | Reset input. When low, the PCM1771 device is powered down, and all mode control registers are reset to default settings. |
| SCKI | 16 | I | System clock input |
| V_{CC} | 12 | – | Power supply for all analog circuits except the headphone amplifier |
| V_{COM} | 6 | – | Decoupling capacitor connection. An external 10- μ F capacitor connected from this terminal to analog ground is required for noise filtering. Voltage level of this terminal is 0.5 V_{HP} nominal. |
| V_{HP} | 11 | – | Analog power supply for the headphone amplifier circuits. The voltage level must be the same as V_{CC} . |

FUNCTIONAL BLOCK DIAGRAM



(): PCM1771

B0001-02

TYPICAL PERFORMANCE CURVES

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = V_{HP} = 2.4\text{ V}$, $f_S = 44.1\text{ kHz}$, system clock = $256 f_S$, 24-bit data, and $R_L = 16\ \Omega$, unless otherwise noted.

Digital Filter

Digital Filter (De-Emphasis Off)

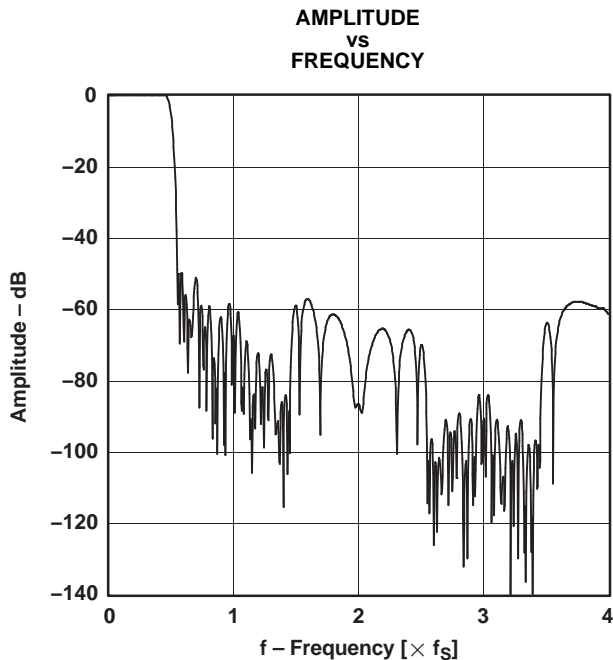


Figure 1.

G001

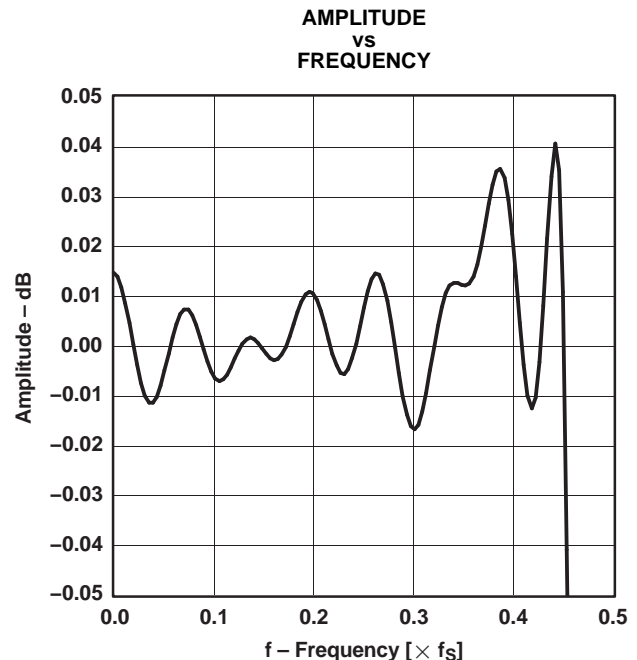


Figure 2.

G002

TYPICAL PERFORMANCE CURVES (continued)

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = V_{HP} = 2.4\text{ V}$, $f_s = 44.1\text{ kHz}$, system clock = $256 f_s$, 24-bit data, and $R_L = 16\ \Omega$, unless otherwise noted.

De-Emphasis Curves

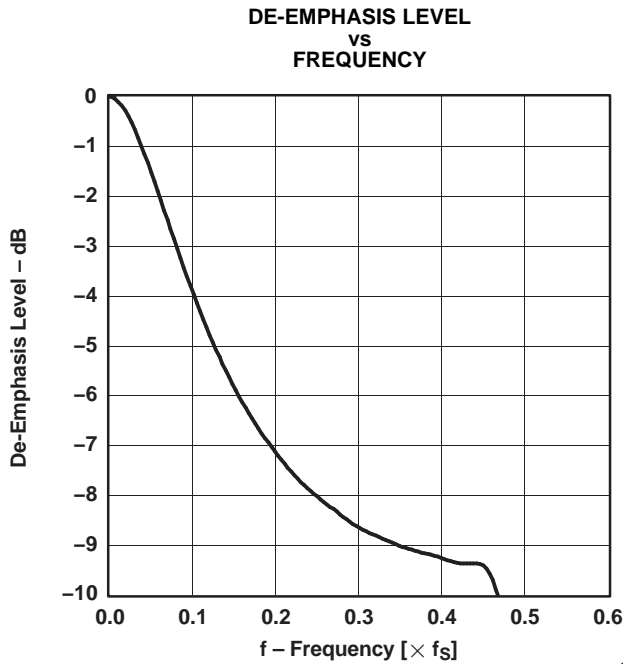


Figure 3.

G003

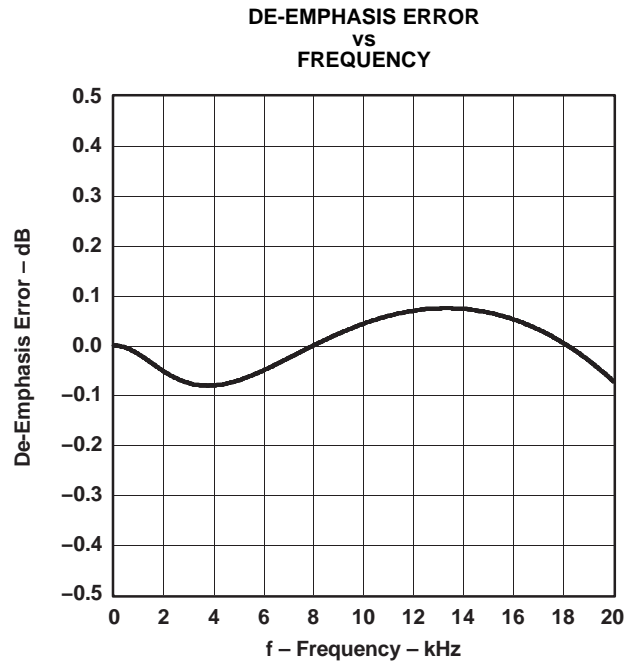


Figure 4.

G004

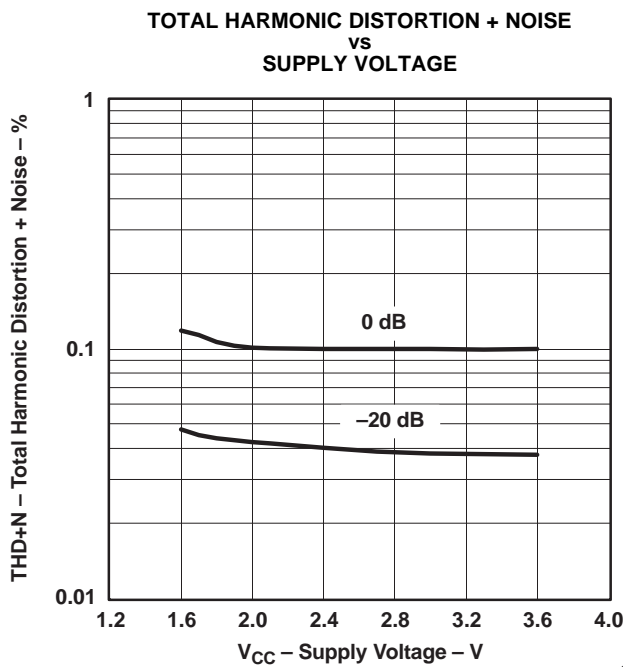


Figure 5.

G005

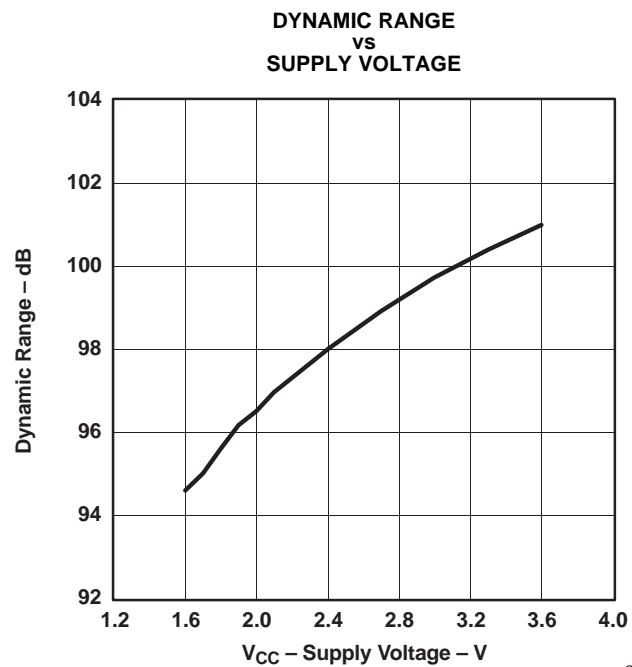


Figure 6.

G006

TYPICAL PERFORMANCE CURVES (continued)

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = V_{HP} 2.4\text{ V}$, $f_S = 44.1\text{ kHz}$, system clock = $256 f_S$, 24-bit data, and $R_L = 16\ \Omega$, unless otherwise noted.

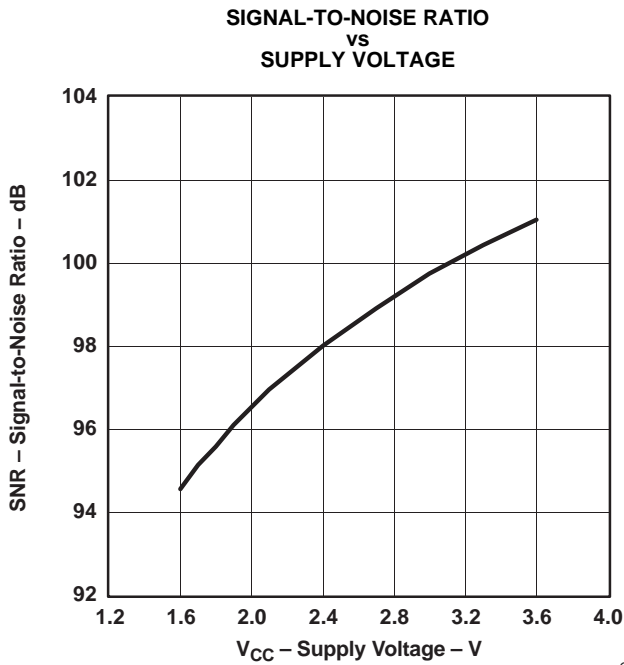


Figure 7.

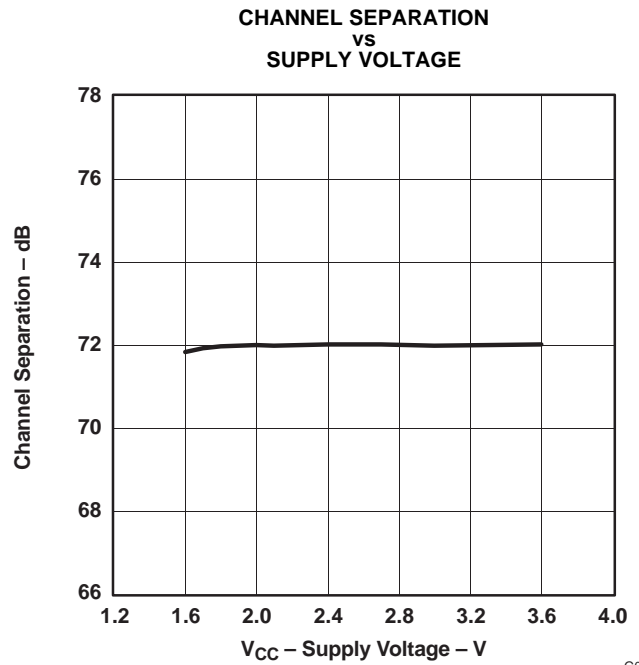


Figure 8.

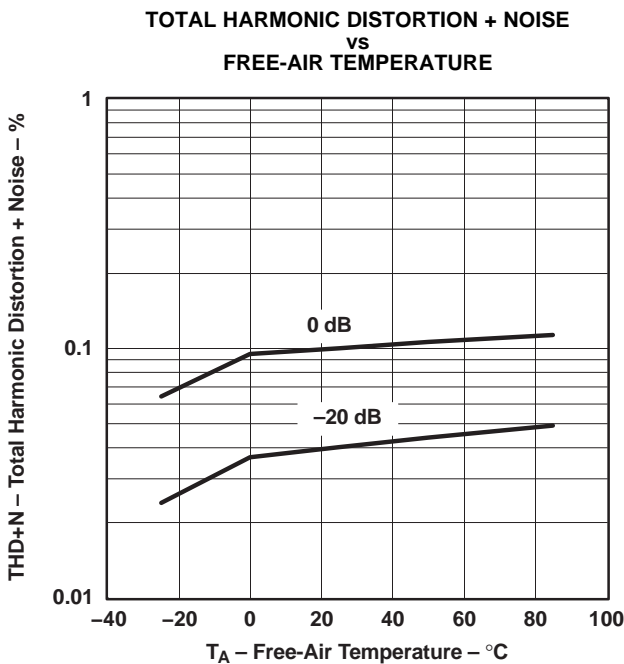


Figure 9.

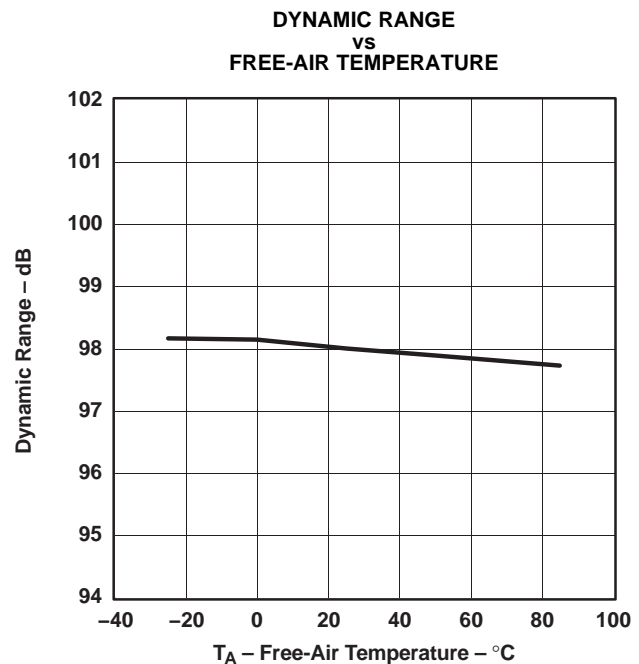


Figure 10.

TYPICAL PERFORMANCE CURVES (continued)

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = V_{HP} 2.4\text{ V}$, $f_S = 44.1\text{ kHz}$, system clock = $256 f_S$, 24-bit data, and $R_L = 16\ \Omega$, unless otherwise noted.

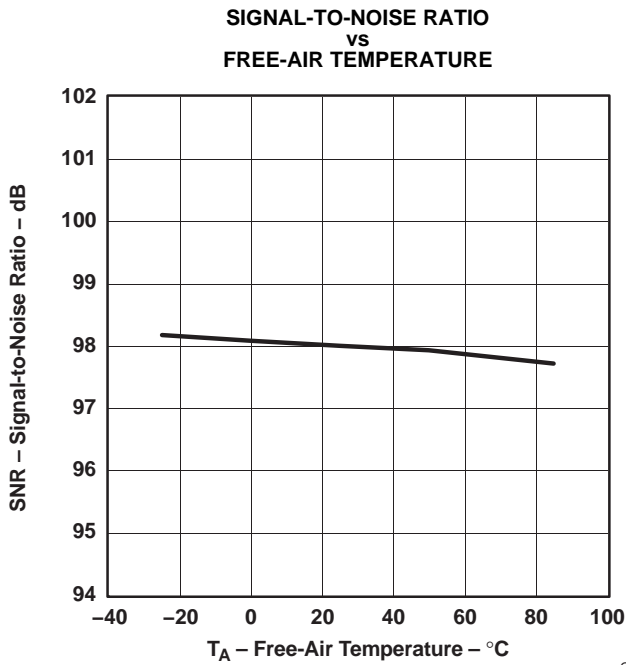


Figure 11.

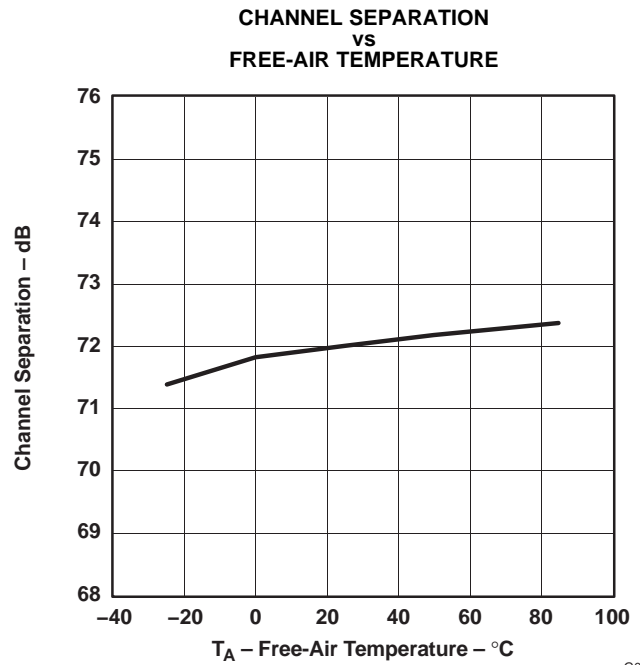


Figure 12.

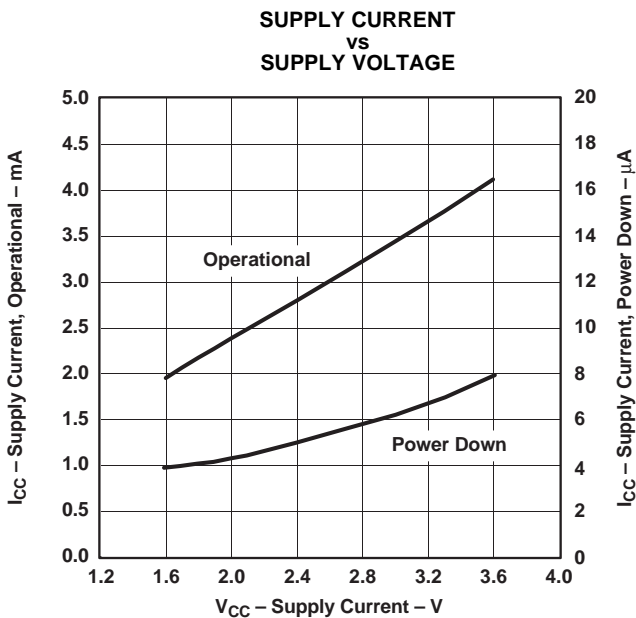


Figure 13.

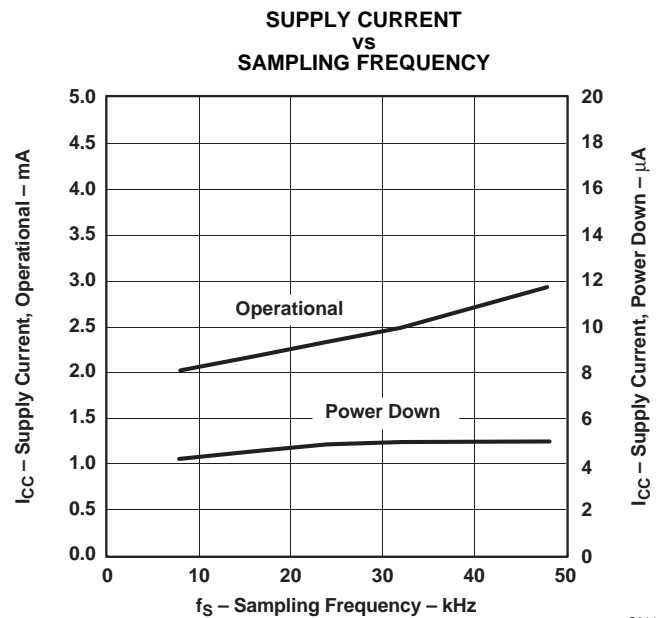


Figure 14.

TYPICAL PERFORMANCE CURVES (continued)

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = V_{HP} 2.4\text{ V}$, $f_S = 44.1\text{ kHz}$, system clock = $256 f_S$, 24-bit data, and $R_L = 16\ \Omega$, unless otherwise noted.

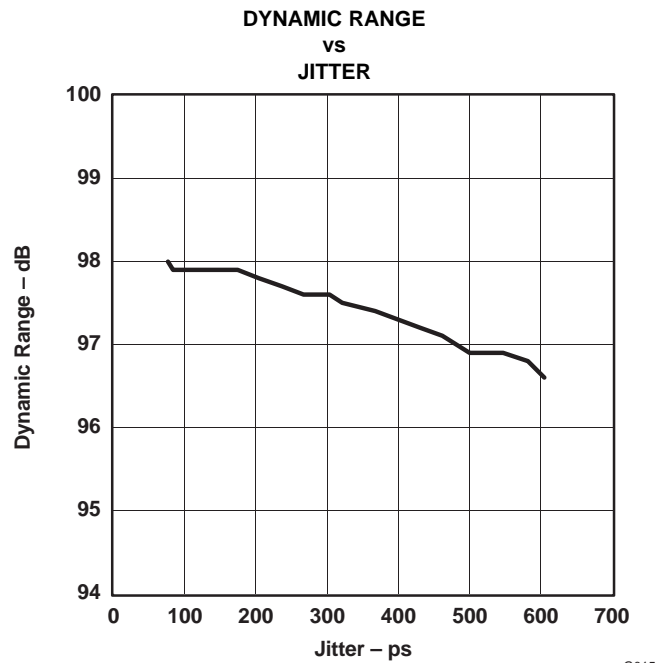


Figure 15.

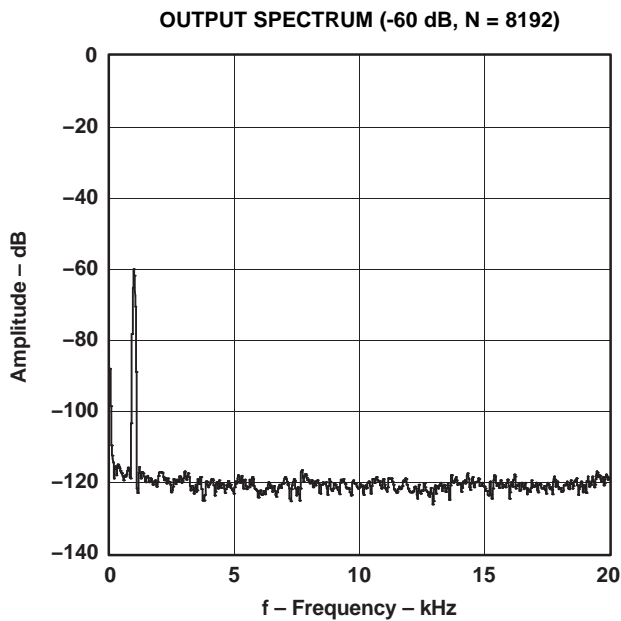


Figure 16.

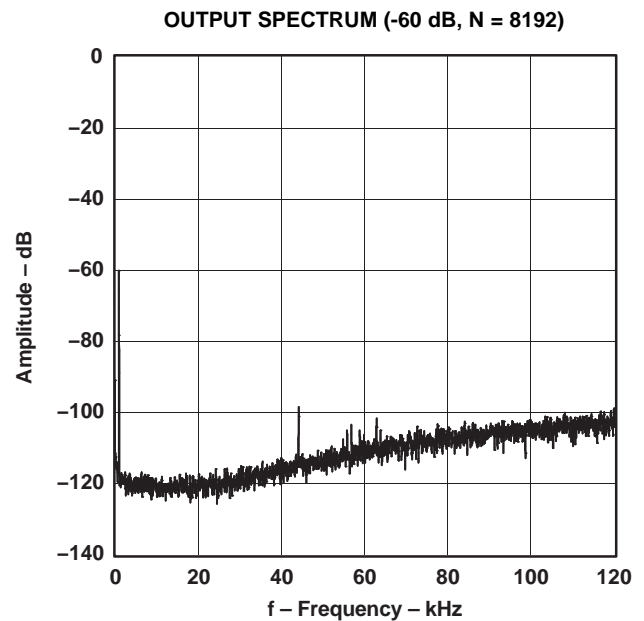


Figure 17.

DETAILED DESCRIPTION

System Clock, Reset, and Functions

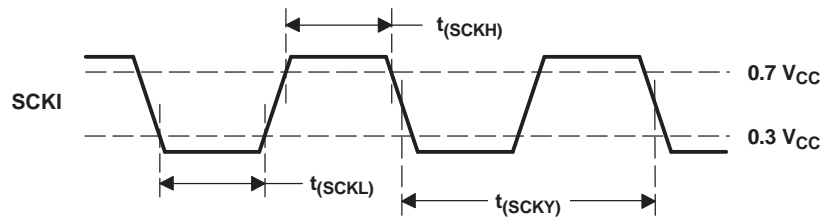
System Clock Input

The PCM1770 and PCM1771 devices require a system clock for operating the digital interpolation filters and multilevel Δ - Σ modulators. The system clock is applied at terminal 16 (SCKI). Table 1 shows examples of system clock frequencies for common audio sampling rates.

Figure 18 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase jitter and noise.

Table 1. System Clock Frequency for Common Audio Sampling Frequencies

| SAMPLING FREQUENCY, LRCK | SYSTEM CLOCK FREQUENCY, SCKI (MHz) | | | |
|--------------------------|------------------------------------|--------------------|--------------------|--------------------|
| | 128 f _S | 192 f _S | 256 f _S | 384 f _S |
| 48 kHz | 6.144 | 9.216 | 12.288 | 18.432 |
| 44.1 kHz | 5.6448 | 8.4672 | 11.2896 | 16.9344 |
| 32 kHz | 4.096 | 6.144 | 8.192 | 12.288 |
| 24 kHz | 3.072 | 4.608 | 6.144 | 9.216 |
| 22.05 kHz | 2.8224 | 4.2336 | 5.6448 | 8.4672 |
| 16 kHz | 2.048 | 3.072 | 4.096 | 6.144 |
| 12 kHz | 1.536 | 2.304 | 3.072 | 4.608 |
| 11.025 kHz | 1.4112 | 2.1168 | 2.8224 | 4.2336 |
| 8 kHz | 1.024 | 1.536 | 2.048 | 3.072 |



T0005-02

| PARAMETER | MIN | UNIT |
|--|-----|------|
| t _(SCKH) System clock pulse duration, HIGH | 7 | ns |
| t _(SCKL) System clock pulse duration, LOW | 7 | ns |
| t _(SCKY) System clock pulse cycle time ⁽¹⁾ | 52 | ns |

(1) 1/(128 f_S), 1/(192 f_S), 1/(256 f_S) or 1/(384 f_S)

Figure 18. System Clock Timing

Power On/Off Reset

The PCM1770/71 always must have the $\overline{\text{PD}}$ pin set from LOW to HIGH once after power-supply voltages V_{CC} and V_{HP} have reached the specified voltage range and stable clocks SCKI, BCK, and LRCK are being supplied for the power-on sequence. A minimum time of 1 ms after both the clock and power-supply requirements are met is required before the $\overline{\text{PD}}$ pin changes from LOW to HIGH, as shown in Figure 19. Subsequent to the $\overline{\text{PD}}$ LOW-to-HIGH transition, the internal logic state is held in reset for 1024 system clock cycles prior to the start of the power-on sequence. During the power-on sequence, H_{OUTL} and H_{OUTR} increase gradually from ground level, reaching an output level that corresponds to the input data after a period of $9334/f_{\text{S}}$. When powering off, the $\overline{\text{PD}}$ pin is set from HIGH to LOW first. Then H_{OUTL} and H_{OUTR} decrease gradually to ground level over a period of $9334/f_{\text{S}}$, as shown in Figure 20, after which power can be removed without creating pop noise. When powering on or off, adhering to the timing requirements of Figure 19 and Figure 20 ensures that pop noise does not occur. If the timing requirements are not met, pop noise might occur.

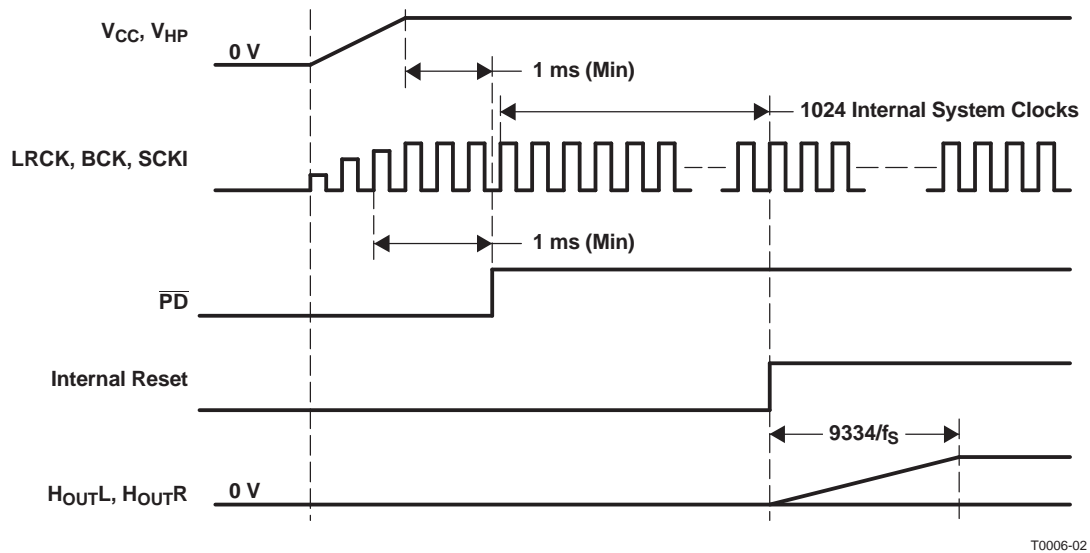


Figure 19. Power-On Sequence

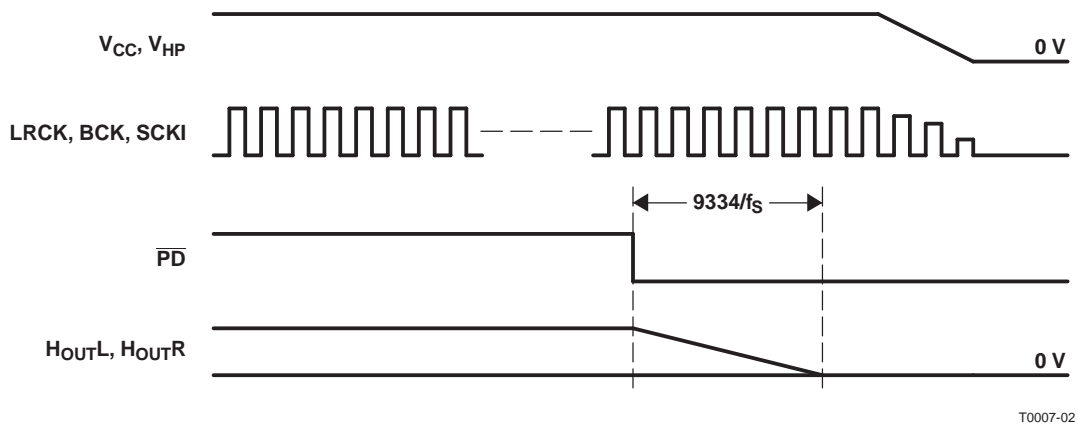


Figure 20. Power-Off Sequence

Power-Up/-Down Sequence and Reset

The PCM1770 device has two kinds of power-up/-down methods: the $\overline{\text{PD}}$ terminal through hardware control and PWRD (register 4, B0) through software control. The PCM1771 device has only the $\overline{\text{PD}}$ terminal through hardware control for the power-up/-down sequence. The power-up or power-down sequence operates the same as the power-on or power-off sequence. When powering up or down using the $\overline{\text{PD}}$ terminal, all digital circuits are reset except for maintaining the logic states of the registers. Figure 21 shows the power-up/power-down sequence.

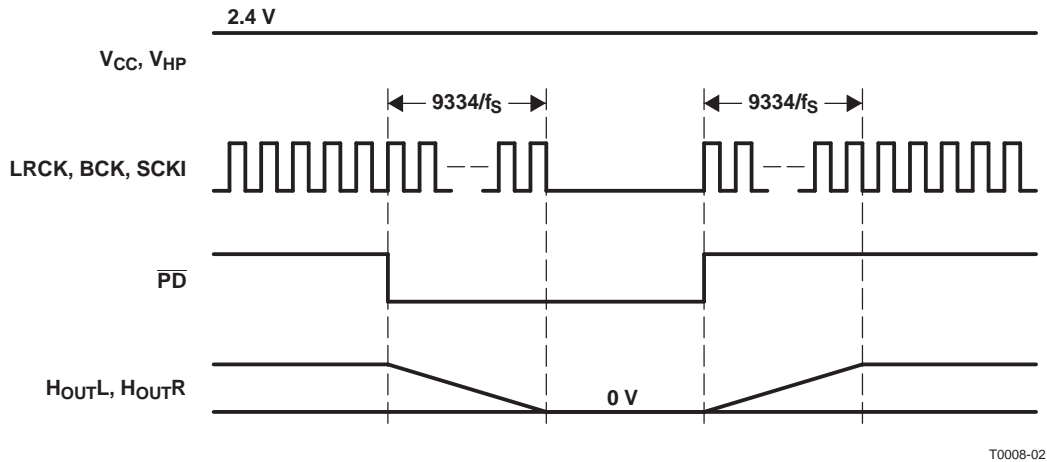


Figure 21. Power-Down and Power-Up Sequences

Audio Serial Interface

The audio serial interface for the PCM1770 and PCM1771 devices consists of a 3-wire synchronous serial port. It includes terminals 1 (LRCK), 2 (DATA), and 3 (BCK). BCK is the serial audio bit clock, and it clocks the serial data present on DATA into the audio interface serial shift register. Serial data is clocked into the PCM1770 and PCM1771 devices on the rising edge of BCK. LRCK is the serial audio left/right word clock. It latches serial data into the serial audio interface internal registers.

Both LRCK and BCK of the PCM1770 device support the slave and master modes, which are set by FMT (register 3). LRCK and BCK are outputs during the master mode and inputs during the slave mode.

In slave mode, BCK and LRCK are synchronous to the audio system clock, SCKI. Ideally, it is recommended that LRCK and BCK be derived from SCKI. LRCK is operated at the sampling frequency, f_s . BCK can be operated at 32, 48, or 64 times the sampling frequency.

In master mode, BCK and LRCK are derived from the system clock and these terminals are outputs. BCK and LRCK are synchronous to SCKI. LRCK is operated at the sampling frequency, f_s . BCK can be operated at 64 times the sampling frequency.

The PCM1770 and PCM1771 devices operate under LRCK synchronized with the system clock. The PCM1770 and PCM1771 devices do not need a specific phase relationship between LRCK and the system clock, but do require the synchronization of LRCK and the system clock. If the relationship between the system clock and LRCK changes more than ± 3 BCK during one sample period, internal operation of the PCM1770 and PCM1771 devices halts within $1/f_s$, and the analog output is kept in last data until resynchronization between system clock and LRCK is completed.

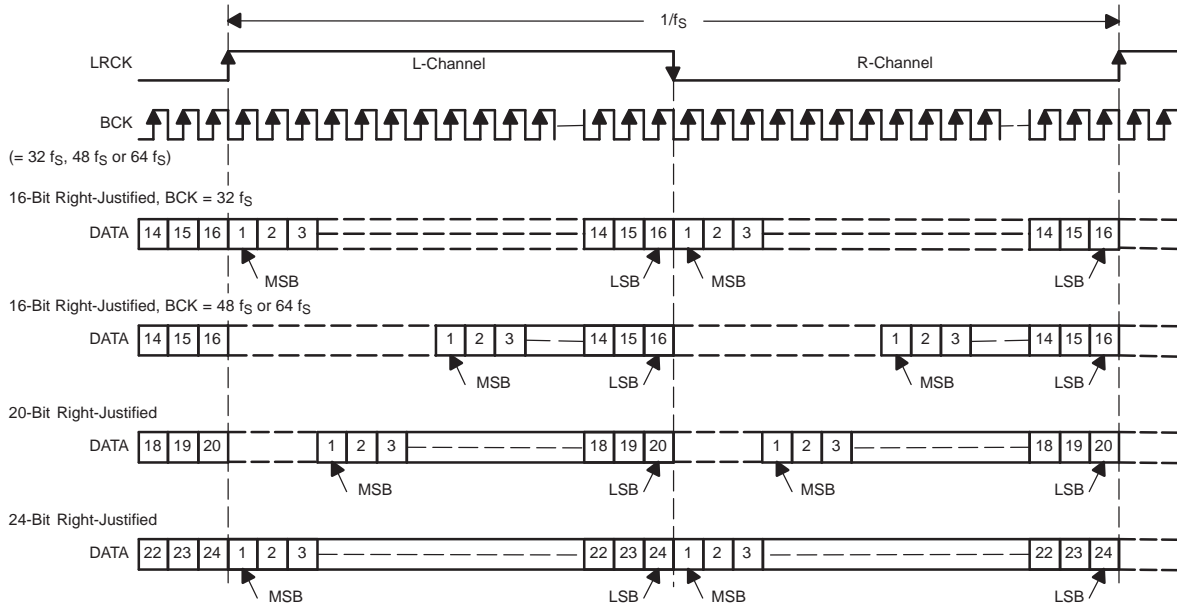
Audio Data Formats and Timing

The PCM1770 device supports industry-standard audio data formats, including standard, I²S, and left-justified. The PCM1771 device supports the I²S and left-justified data formats. [Table 2](#) lists the main features of the audio data interface. [Figure 22](#) shows the data formats. Data formats are selected using the format bits, FMT[2:0] of control register 3 in the case of the PCM1770 device, and are selected using the FMT terminal in the case of the PCM1771 device. The default data format is 24-bit, left-justified, slave mode. All formats require binary 2s complement, MSB-first audio data. [Figure 23](#) shows a detailed timing diagram for the serial audio interface in slave mode. [Figure 24](#) shows a detailed timing diagram for the serial audio interface in master mode.

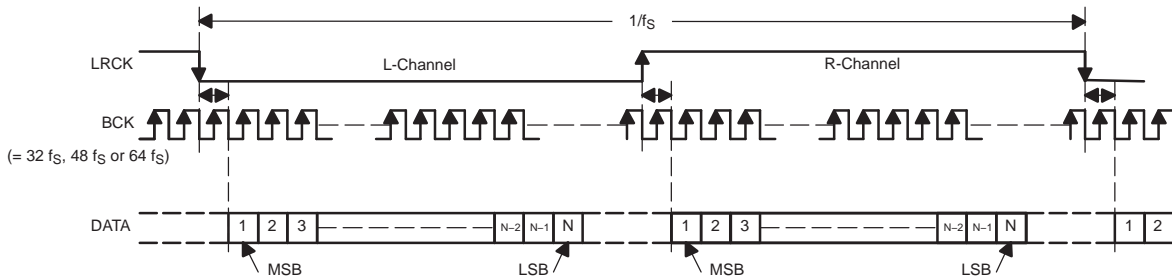
Table 2. Audio Data Interface

| AUDIO-DATA INTERFACE FEATURE | | CHARACTERISTIC |
|------------------------------|-----------|--|
| Audio data interface format | (PCM1770) | Standard, I ² S, left-justified |
| | (PCM1771) | I ² S, left-justified |
| Audio data bit length | | 16-, 20-, 24-bit selectable |
| Audio data format | | MSB-first, 2s-complement |

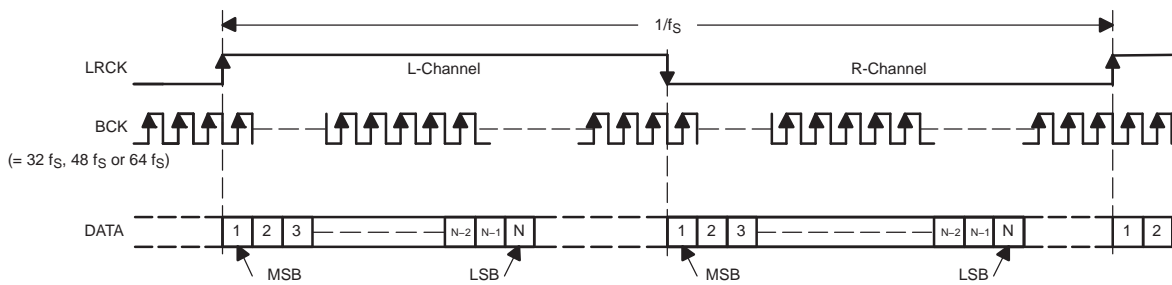
(1) Standard Data Format; L-Channel = HIGH, R-Channel = LOW (Slave Mode)



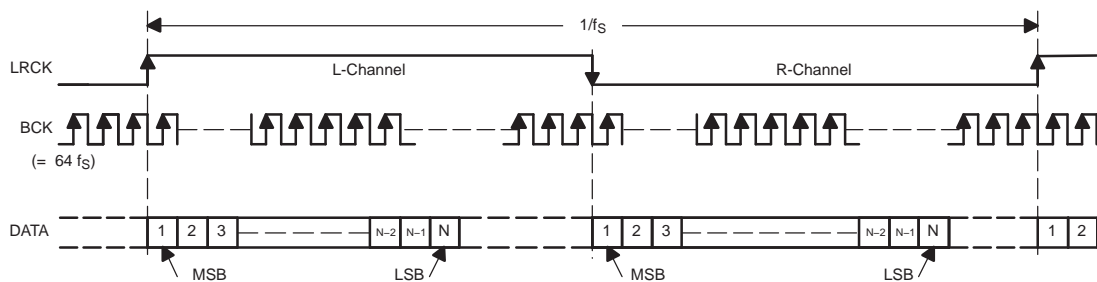
(2) I²S Data Format; L-Channel = LOW, R-Channel = HIGH (Slave Mode)



(3) Left-Justified Data Format; L-Channel = HIGH, R-Channel = LOW (Slave Mode)

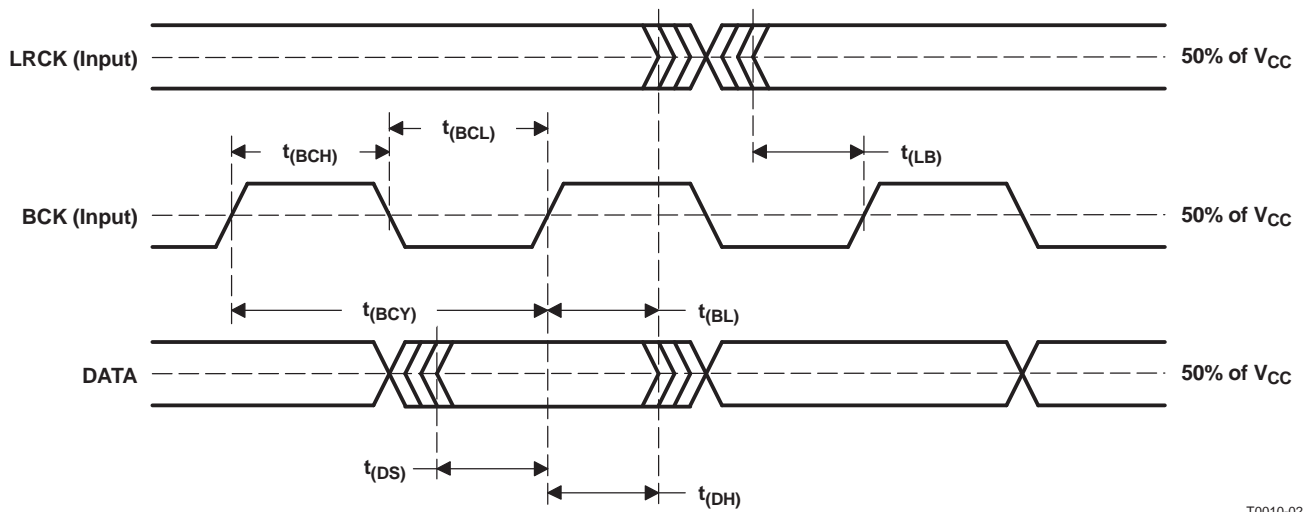


(4) Left-Justified Data Format; L-Channel = HIGH, R-Channel = LOW (Master Mode)
 (The frequency of BCK is $64 f_s$ and SCK1 is $256 f_s$ only)



T0009-01

Figure 22. Audio Data Input Formats

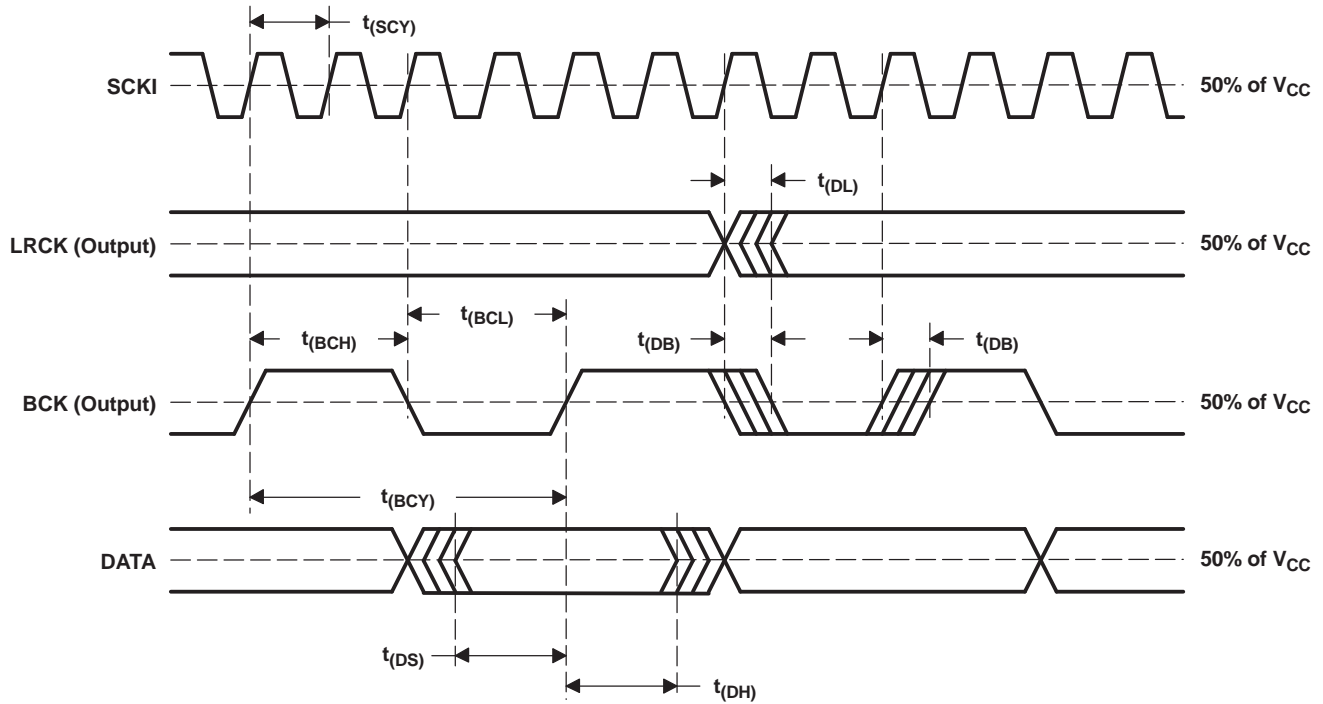


T0010-02

| PARAMETER | | MIN | MAX | UNIT |
|-------------|------------------------------|--------------------|-----|------|
| $t_{(BCY)}$ | BCK pulse cycle time | $1/(64 f_S)^{(1)}$ | | |
| $t_{(BCH)}$ | BCK high-level time | 35 | | ns |
| $t_{(BCL)}$ | BCK low-level time | 35 | | ns |
| $t_{(BL)}$ | BCK rising edge to LRCK edge | 10 | | ns |
| $t_{(LB)}$ | LRCK edge to BCK rising edge | 10 | | ns |
| $t_{(DS)}$ | DATA set-up time | 10 | | ns |
| $t_{(DH)}$ | DATA hold time | 10 | | ns |

(1) f_S is the sampling frequency.

Figure 23. Audio Interface Timing (Slave Mode)



T0011-02

| PARAMETER | | MIN | MAX | UNIT |
|-------------|---------------------------------|---------------------|-----|------|
| $t_{(SCY)}$ | SCKI pulse cycle time | $1/(256 f_S)^{(1)}$ | | |
| $t_{(DL)}$ | LRCK edge from SCKI rising edge | 0 | 40 | ns |
| $t_{(DB)}$ | BCK edge from SCKI rising edge | 0 | 40 | ns |
| $t_{(BCY)}$ | BCK pulse cycle time | $1/(64 f_S)^{(1)}$ | | |
| $t_{(BCH)}$ | BCK high-level time | 146 | | ns |
| $t_{(BCL)}$ | BCK low-level time | 146 | | ns |
| $t_{(DS)}$ | DATA setup time | 10 | | ns |
| $t_{(DH)}$ | DATA hold time | 10 | | ns |

(1) f_S is up to 48 kHz. f_S is the sampling frequency.

Figure 24. Audio Interface Timing (Master Mode)

Hardware Control (PCM1771)

The digital functions of the PCM1771 device are capable of hardware control. [Table 3](#) shows selectable formats, [Table 4](#) shows de-emphasis control, and [Table 5](#) shows analog mixing control.

Table 3. Data Format Select

| FMT | DATA FORMAT |
|------------|--|
| Low | 16- to 24-bit, left-justified format |
| High | 16- to 24-bit, I ² S format |

Table 4. De-Emphasis Control

| DEMP | DE-EMPHASIS FUNCTION |
|-------------|-----------------------------|
| Low | 44.1-kHz de-emphasis OFF |
| High | 44.1-kHz de-emphasis ON |

Table 5. Analog Mixing Control

| AMIX | ANALOG MIXING |
|-------------|----------------------|
| Low | Analog mixing OFF |
| High | Analog mixing ON |

Software Control (PCM1770)

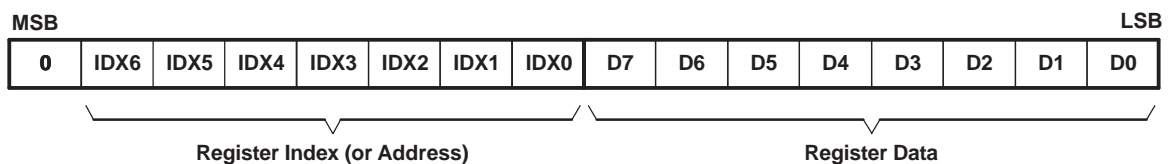
The PCM1770 device has many programmable functions that can be controlled in the software-control mode. The functions are controlled by programming the internal registers using \overline{MS} , MC, and MD.

The software-control interface is a 3-wire serial port that operates asynchronously to the serial audio interface. The serial control interface is used to program the on-chip mode registers. MD is the serial data input, used to program the mode registers. MC is the serial bit clock, used to shift data into the control port. \overline{MS} is the mode control port select signal.

Register Write Operation (PCM1770)

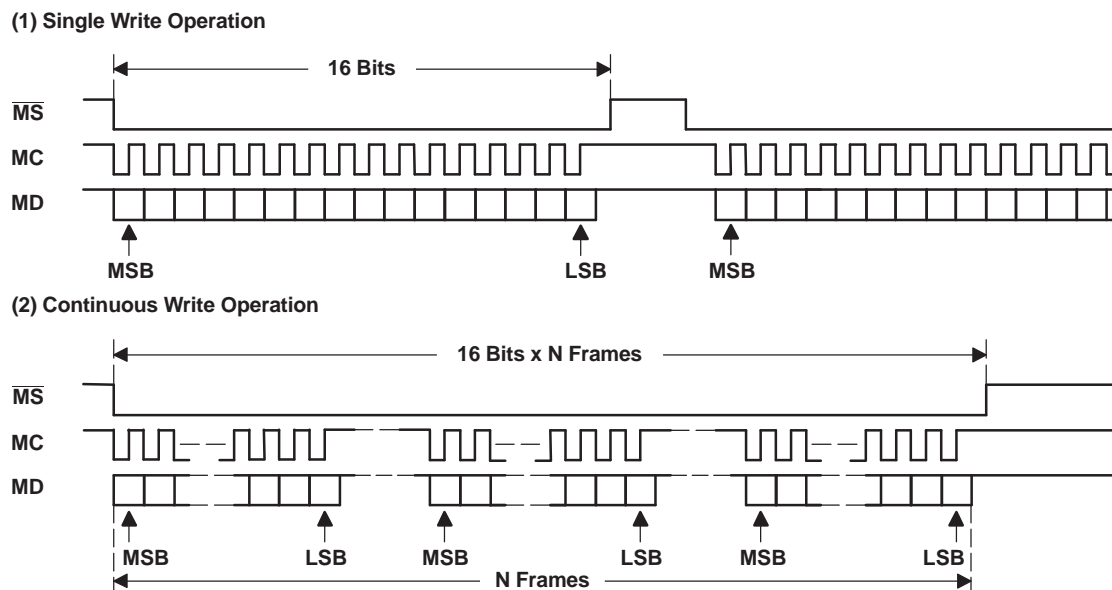
All write operations for the serial control port use 16-bit data words. Figure 25 shows the control data word format. The most significant bit must be 0. There are seven bits, labeled $IDX[6:0]$, that set the register index (or address) for the write operation. The eight least significant bits, $D[7:0]$, contain the data to be written to the register specified by $IDX[6:0]$.

Figure 26 shows the functional timing diagram for writing to the serial control port. To write data into the mode register, the data is clocked into an internal shift register on the rising edge of the MC clock. Serial data can change on the falling edge of the MC clock and must be stable on the rising edge of the MC clock. The \overline{MS} signal must be low during the write mode and the rising edge of the \overline{MS} signal must be aligned with the falling edge of the last MC clock pulse in the 16-bit frame. The MC clock can run continuously between transactions while the \overline{MS} signal is low.



R0001-01

Figure 25. Control Data Word Format for MD

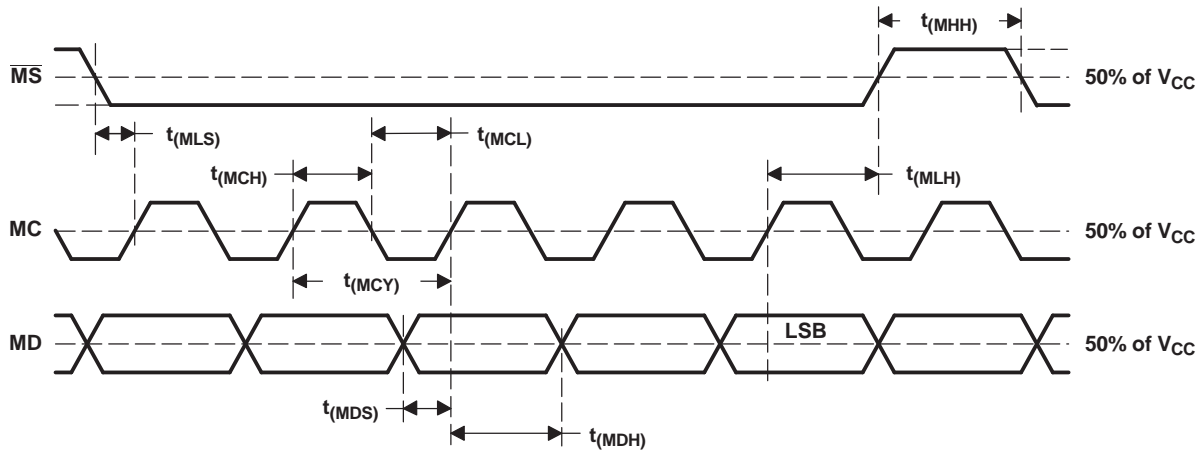


T0012-01

Figure 26. Register Write Operation

Control Interface Timing Requirements (PCM1770)

Figure 27 shows a detailed timing diagram for the serial control interface. These timing parameters are critical for proper control port operation.



T0013-02

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|--|-------------|--------------------|-----|-----|------|
| MC pulse cycle time | $t_{(MCY)}$ | 100 ⁽¹⁾ | | | ns |
| MC low-level time | $t_{(MCL)}$ | 50 | | | ns |
| MC high-level time | $t_{(MCH)}$ | 50 | | | ns |
| \overline{MS} high-level time | $t_{(MMH)}$ | (2) | | | ns |
| \overline{MS} falling edge to MC rising edge | $t_{(MLS)}$ | 20 | | | ns |
| \overline{MS} hold time | $t_{(MLH)}$ | 20 | | | ns |
| MD hold time | $t_{(MDH)}$ | 15 | | | ns |
| MD setup time | $t_{(MDS)}$ | 20 | | | ns |

(1) When MC runs continuously between transactions, MC pulse cycle time is specified as $3/(128 f_s)$, where f_s is sampling rate.

(2) $3/(128 f_s)$ s (min), where f_s is sampling rate.

Figure 27. Control Interface Timing

Mode Control Registers (PCM1770)

User-Programmable Mode Controls

The PCM1770 device has a number of user-programmable functions that can be accessed via mode control registers. The registers are programmed using the serial control interface, as discussed in the *Software Control (PCM1770)* section. [Table 6](#) lists the available mode control functions, along with their reset default conditions and associated register index.

Register Map

[Table 7](#) shows the mode control register map. Each register includes an index (or address) indicated by the $IDX[6:0]$ bits.

Table 6. User-Programmable Mode Controls

| FUNCTION | RESET DEFAULT | REGISTER NO. | BIT(S) |
|--|---------------------------------|--------------|--------------------|
| Soft mute control, L/R independently | Disabled | 01 | MUTL, MUTR |
| Digital attenuation level setting, 0 dB to –63 dB in 1-dB steps, L/R independently | 0 dB | 01, 02 | ATL[5:0], ATR[5:0] |
| Oversampling rate control (128 f _S , 192 f _S , 256 f _S , 384 f _S) | 128 f _S oversampling | 03 | OVER |
| Polarity control for analog output for R-channel DAC | Not inverted | 03 | RINV |
| Analog mixing control for analog in, AIN (terminal 14) | Disabled | 03 | AMIX |
| 44.1-kHz de-emphasis control | Disabled | 03 | DEM |
| Audio data format select | 24-bit, left-justified format | 03 | FMT[2:0] |
| Zero cross attenuation | Disabled | 04 | ZCAT |
| Power-down control | Disabled | 04 | PWRD |

Table 7. Mode Control Register Map

| REGIS TER | IDX [6:0] (B14-B8) | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|-----------|--------------------|-----|------|------|------|------|------|------|------|--------------------|--------------------|--------------------|------|--------------------|--------------------|--------------------|------|
| 01 | 01h | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | MUTR | MUTL | ATL5 | ATL4 | ATL3 | ATL2 | ATL1 | ATL0 |
| 02 | 02h | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV ⁽¹⁾ | RSV ⁽¹⁾ | ATR5 | ATR4 | ATR3 | ATR2 | ATR1 | ATR0 |
| 03 | 03h | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | OVER | RSV ⁽¹⁾ | RINV | AMIX | DEM | FMT2 | FMT1 | FMT0 |
| 04 | 04h | 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV ⁽¹⁾ | RSV ⁽¹⁾ | RSV ⁽¹⁾ | ZCAT | RSV ⁽¹⁾ | RSV ⁽¹⁾ | RSV ⁽¹⁾ | PWR |

(1) RSV is reserved for test operation. It must be set to 0 during regular operation.

Register Definitions

Register 01

| | | | | | | | | | | | | | | | |
|------------|------------|------------|------------|------------|------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | MUTR | MUTL | ATL5 | ATL4 | ATL3 | ATL2 | ATL1 | ATL0 |

IDX[6:0]: 000 0001b

MUTx: Soft Mute Control

Where, x = L or R, corresponding to the headphone output H_{OUTL} or H_{OUTR}.

Default value: 0

| | |
|----------------|-------------------------|
| MUTL, MUTR = 0 | Mute disabled (default) |
| MUTL, MUTR = 1 | Mute enabled |

The mute bits, MUTL and MUTR, enable or disable the soft mute function for the corresponding headphone outputs, H_{OUTL} and H_{OUTR}. The soft mute function is incorporated into the digital attenuators. When mute is disabled (MUTx = 0), the attenuator and DAC operate normally. When mute is enabled by setting MUTx = 1, the digital attenuator for the corresponding output is decreased from the current setting to the infinite attenuation, one attenuator step (1 dB) at a time. This provides pop-free muting of the headphone output.

By setting MUTx = 0, the attenuator is increased one step at a time to the previously programmed attenuation level.

ATL[5:0]: Digital Attenuation Level Setting for Headphone Output, H_{OUTL}

Default value: 11 1111b

Headphone output H_{OUTL} includes a digital attenuation function. The attenuation level can be set from 0 dB to –62 dB, in 1-dB steps. Changes in attenuator levels are made by incrementing or decrementing by one step (1 dB) for every 8/f_s time interval until the programmed attenuator setting is reached. Alternatively, the attenuation level may be set to infinite attenuation (or mute).

The following table shows the attenuation levels for various settings:

| ATL[5:0] | ATTENUATION LEVEL SETTING |
|-----------------|----------------------------------|
| 11 1111b | 0 dB, no attenuation (default) |
| 11 1110b | –1 dB |
| 11 1101b | –2 dB |
| : | : |
| 00 0010b | –61 dB |
| 00 0001b | –62 dB |
| 00 0000b | Mute |

Register 02

| | | | | | | | | | | | | | | | |
|------------|------------|------------|------------|------------|------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV | RSV | ATR5 | ATR4 | ATR3 | ATR2 | ATR1 | ATR0 |

IDX[6:0]: 000 0010b

ATR[5:0]: Digital Attenuation Level Setting for Headphone Output, H_{OUTR}

Default value: 11 1111b

Headphone output H_{OUTR} includes a digital attenuation function. The attenuation level can be set from 0 dB to –62 dB, in 1-dB steps. Changes in attenuator levels are made by incrementing or decrementing by one step (1 dB) for every 8/f_s time interval until the programmed attenuator setting is reached. Alternatively, the attenuation level can be set to infinite attenuation (or mute).

To set the attenuation levels for ATR[5:0], see the table for ATL[5:0], register 01.

Register 03

| | | | | | | | | | | | | | | | |
|-----|------|------|------|------|------|------|------|------|-----|------|------|-----|------|------|------|
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | OVER | RSV | RINV | AMIX | DEM | FMT2 | FMT1 | FMT0 |

IDX[6:0]: 000 0011b

OVER: Oversampling Control

Default value: 0

| | |
|----------|--|
| OVER = 0 | 128f _S oversampling |
| OVER = 1 | 192f _S , 256f _S , 384f _S oversampling |

The OVER bit controls the oversampling rate of the Δ-Σ D/A converters. When it operates at a low sampling rate, less than 24 kHz, this function is recommended.

RINV: Polarity Control for Headphone Output, H_{OUTR}

Default value: 0

| | |
|----------|-----------------|
| RINV = 0 | Not inverted |
| RINV = 1 | Inverted output |

The RINV bits allow the user to control the polarity of the headphone output, H_{OUTR}. This function can be used to connect the monaural speaker using the BTL connection method. This bit is recommended to be 0 during the power-up/-down sequence for minimizing audible pop noise.

AMIX: Analog Mixing Control for External Analog Signal, AIN

Default value: 0

| | |
|----------|------------------------------------|
| AMIX = 0 | Disabled (not mixed) |
| AMIX = 1 | Enabled (mixing to the DAC output) |

The AMIX bit allows the user to mix analog input (AIN) with headphone outputs (H_{OUTL}/H_{OUTR}) internally.

DEM: 44.1-kHz De-Emphasis Control

Default value: 0

| | |
|---------|----------|
| DEM = 0 | Disabled |
| DEM = 1 | Enabled |

The DEM bit enables or disables the digital de-emphasis filter for the 44.1-kHz sampling rate.

FMT[2:0]: Audio Interface Data Format

Default value: 000

The FMT[2:0] bits select the data format for the serial audio interface. The following table shows the available format options.

| FMT[2:0] | Audio Data Format Selection |
|----------|---|
| 000 | 16- to 24-bit, left-justified format (default) |
| 001 | 16- to 24-bit, I ² S format |
| 010 | 24-bit right-justified data |
| 011 | 20-bit right-justified data |
| 100 | 16-bit right-justified data |
| 101 | 16- to 24-bit, left-justified format, master mode |
| 110 | Reserved |
| 111 | Reserved |

Register 04

| | | | | | | | | | | | | | | | |
|-----|------|------|------|------|------|------|------|-----|-----|-----|------|-----|-----|-----|------|
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| 0 | IDX6 | IDX5 | IDX4 | IDX3 | IDX2 | IDX1 | IDX0 | RSV | RSV | RSV | ZCAT | RSV | RSV | RSV | PWRD |

IDX[6:0]: 0000 0100b

ZCAT: Zero Cross Attenuation

Default value: 0

| | |
|----------|------------------------------|
| ZCAT = 0 | Normal attenuation (default) |
| ZCAT = 1 | Zero cross attenuation |

This bit enables changing the signal level on zero crossing during attenuation control or muting. If the signal does not cross BPZ beyond $512/f_s$ (11.6 ms at 44.1-kHz sampling rate), the signal level is changed similarly to normal attenuation control. This function is independently monitored for each channel; moreover, change of signal level is alternated between both channels. [Figure 28](#) shows an example of zero cross attenuation.

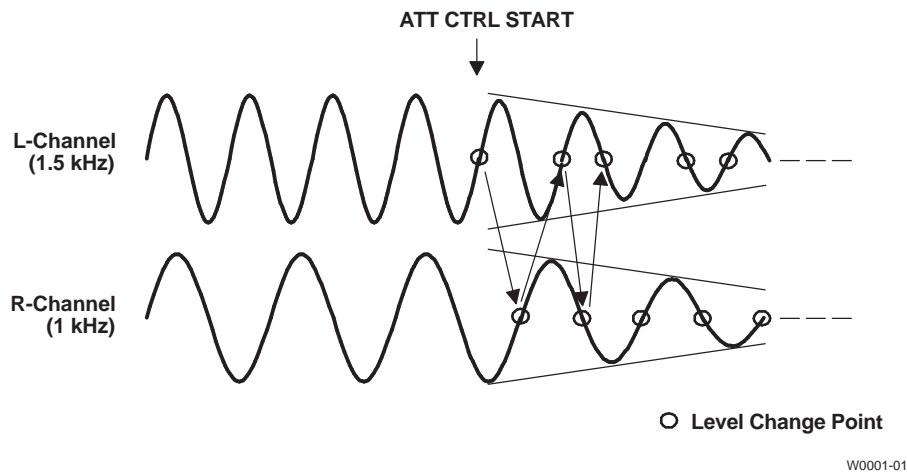


Figure 28. Example of Zero Cross Attenuation

PWRD: Power Down Control

Default value: 0

| | |
|----------|----------------------------|
| PWRD = 0 | Normal operation (default) |
| PWRD = 1 | Power-down state |

This bit is used to enter into low-power mode. Note that PWRD has no reset function.

When this bit is set to 1, the PCM1770 device enters low-power mode and all digital circuits are reset except the register states, which remain unchanged.

Analog In/Out

Headphone Output (Stereo)

The PCM1770 and PCM1771 devices have two independent headphone amplifiers, and the amplifier outputs are provided at the H_{OUTL} and H_{OUTR} terminals. Because the capability of the headphone output is designed for driving a 16-Ω impedance headphone, less than a 16-Ω impedance headphone is not recommended. A resistor and a capacitor must be connected to H_{OUTL} and H_{OUTR} to ensure proper output loading.

Monaural Output (BTL Mode/Monaural Speaker)

The monaural output can be created by summing the left and right headphone outputs. When in the BTL mode, the user must set the headphone output levels to –3 dB using the ATL[5:0] bits in register 01 and the ATR[5:0] bits in register 02. Moreover, invert the polarity of the right headphone output by using the RINV bit on control register 03. The RINV bit is recommended to be 0 during the power-up/-down sequence for minimizing audible pop noise.

Analog Input

The PCM1770 and PCM1771 devices have an analog input, AIN (terminal 10). The AMIX bit (PCM1770) or the AMIX terminal (PCM1771) allows the user to mix AIN with the headphone outputs (H_{OUTL} and H_{OUTR}) internally. When in the mixing mode, an ac-coupling capacitor is needed for AIN. But if AIN is not used, AIN must be open and the AMIX bit (PCM1770) must be disabled or the AMIX terminal (PCM1771) must be low.

Because AIN does not have an internal low-pass filter, it is recommended that the bandwidth of the input signal into AIN is limited to less than 100 kHz. The source of signals connected to AIN must be connected by low impedance.

Although the maximum input voltage on AIN is designed to be as large as 0.584 V_{HP} (peak-to-peak), the user must attenuate the input voltage on AIN and control the digital input data so that each line output (H_{OUTL} and H_{OUTR}) does not exceed 0.55 V_{HP} (peak-to-peak) in the mixing mode.

V_{COM} Output

One unbuffered common-mode voltage output terminal, V_{COM}, is brought out for decoupling purposes. This terminal is nominally biased to a dc voltage level equal to 0.5 V_{HP} and connected to a 10-μF capacitor. In the case of a capacitor smaller than 10 μF, pop noise can be generated during the power-on/-off or power-up/-down sequences.

APPLICATION INFORMATION

Connection Diagrams

[Figure 29](#) shows the basic connection diagram with the necessary power supply bypassing and decoupling components. It is recommended that the component values shown in [Figure 29](#) be used for all designs.

The use of series resistors ($22\ \Omega$ to $100\ \Omega$) is recommended for the SCKI, LRCK, BCK, and DATA inputs. The series resistor combines with the stray PCB and device input capacitance to form a low-pass filter that reduces high-frequency noise emissions and helps to dampen glitches and ringing present on the clock and data lines.

Power Supplies and Grounding

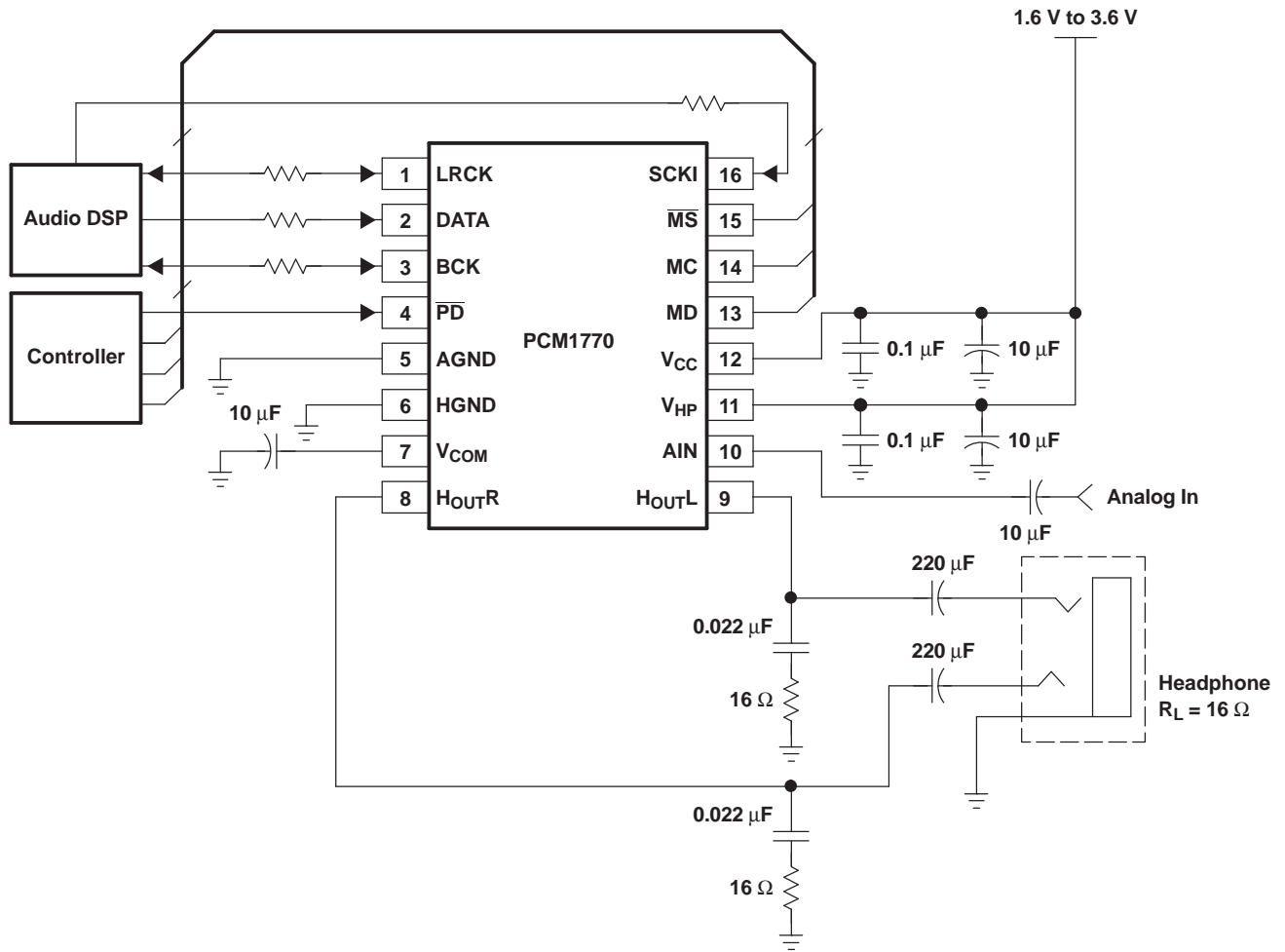
The PCM1770 and PCM1771 devices require a 2.4-V typical analog supply for V_{CC} and V_{HP} . These 2.4-V supplies power the DAC, analog output filter, and other circuits. For best performance, these 2.4-V supplies must be derived from the analog supply using a linear regulator, as shown in [Figure 29](#).

[Figure 29](#) shows the proper power supply bypassing. The $10\text{-}\mu\text{F}$ capacitors must be tantalum or aluminum electrolytic, while the $0.1\text{-}\mu\text{F}$ capacitors are ceramic (X7R type is recommended for surface-mount applications).

Short-Circuit Protection

Continuous shorting of H_{OUTL} and H_{OUTR} to GND, to a power supply, or to each other is not permitted, as protection circuitry for an output short is not implemented in the device. If the possibility of shorting cannot be eliminated in an application, an $8\text{-}\Omega$ or higher series resistor must be added between the phase compensation circuits of the H_{OUTX} pins and the application circuitry (headphone jack in [Figure 29](#)).

APPLICATION INFORMATION (continued)



S0008-01

Figure 29. Basic Connection Diagram

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from D Revision (April 2005) to E Revision | Page |
|---|-------------|
| • Changed MCKI to SCKI | 29 |
| • Corrected errors, added recommended parts, and changed incorrect symbols | 30 |
| Changes from C Revision (May 2004) to D Revision | Page |
| • Changed data sheet to new format | 1 |
| • Changed value for power-supply voltage | 2 |
| • Removed package/ordering information, reformatted, and appended at end of data sheet | 2 |
| • Added new Recommended Operating Conditions table to data sheet..... | 2 |
| • Changed page layout for Terminal Function tables..... | 6 |
| • Changed page layout of Figure 13 and Figure 14 | 12 |
| • In Figure 22 , added arrows to all rising edges of BCK for data formats (2), (3), and (4) | 18 |
| • Added new subsection, Short-Circuit Protection, with information concerning protection of output pins..... | 29 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| PCM1770PW | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 1770 | Samples |
| PCM1770PWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 1770 | Samples |
| PCM1770RGA | ACTIVE | VQFN | RGA | 20 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 1770 | Samples |
| PCM1770RGAR | ACTIVE | VQFN | RGA | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 1770 | Samples |
| PCM1771PW | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 1771 | Samples |
| PCM1771PWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 1771 | Samples |
| PCM1771RGA | ACTIVE | VQFN | RGA | 20 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | | 1771 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=100ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| PCM1770PWR | TSSOP | PW | 16 | 2000 | 330.0 | 17.4 | 6.8 | 5.4 | 1.6 | 8.0 | 16.0 | Q1 |
| PCM1770RGAR | VQFN | RGA | 20 | 2000 | 330.0 | 13.4 | 4.4 | 4.4 | 1.3 | 8.0 | 12.0 | Q1 |
| PCM1771PWR | TSSOP | PW | 16 | 2000 | 330.0 | 17.4 | 6.8 | 5.4 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| PCM1770PWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| PCM1770RGAR | VQFN | RGA | 20 | 2000 | 367.0 | 367.0 | 35.0 |
| PCM1771PWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 38.0 |



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

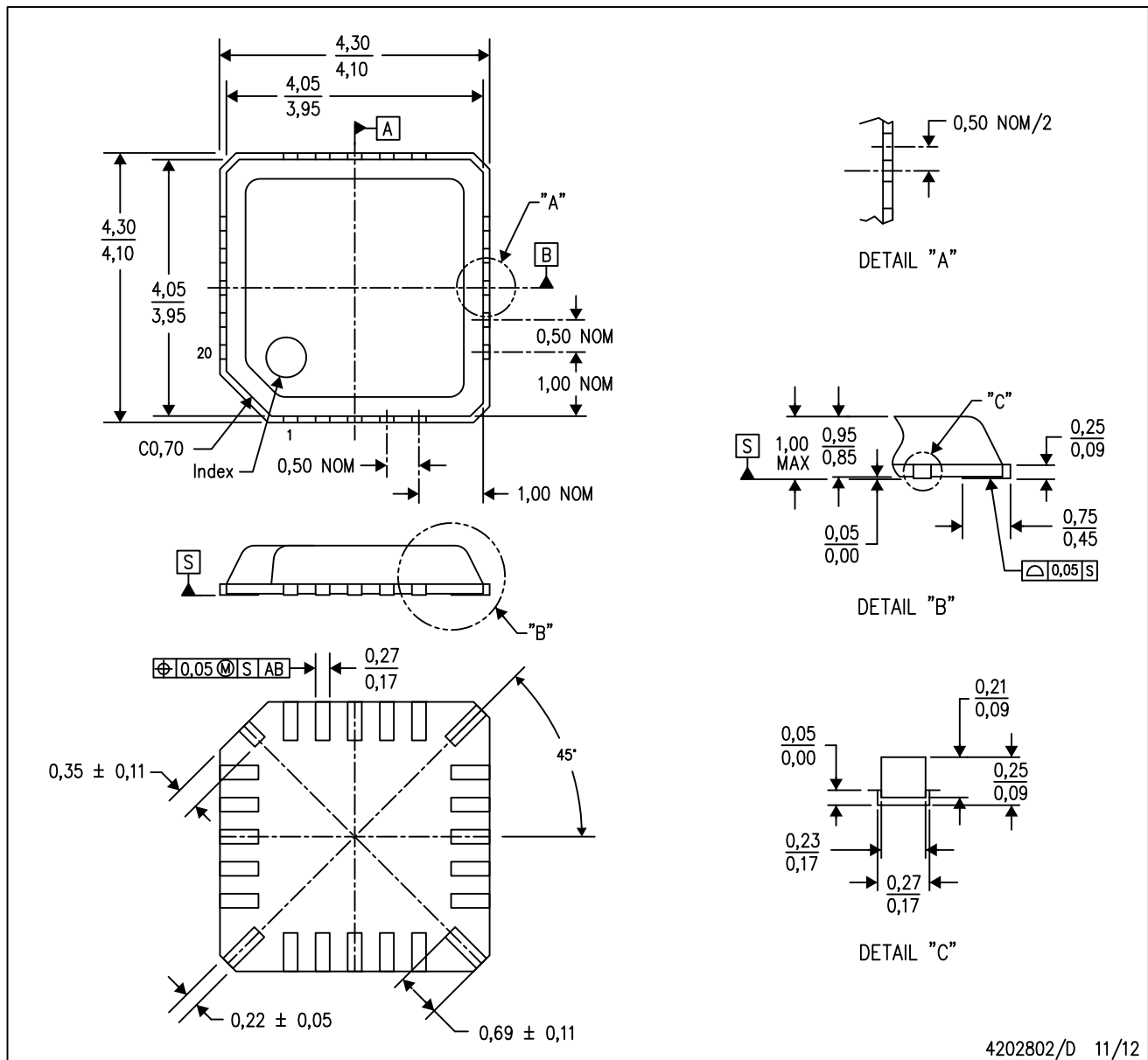
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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGA (S-PQFP-N20)

PLASTIC QUAD FLATPACK



4202802/D 11/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - These dimensions include package bend.
 - Falls within EIAJ: EDR-7324.

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