SN74CBTLV3126 Low-voltage quadruple FET bus switch

1 Features

- Standard ’126-Type Pinout
- 5-Ω Switch Connection Between Two Ports
- Rail-to-Rail Switching on Data I/O Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-up Performance Exceeds 100 mA per JESD 78, Class II

2 Applications

- Datacenter and enterprise computing
- Broadband fixed Access
- Building Automation
- Wired Networking
- Motor Drives

3 Description

The SN74CBTLV3126 quadruple FET bus switch features independent line switches. Each switch is disabled when the associated output-enable (OE) input is low.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The SN74CBTLV3126 device has isolation during power off.

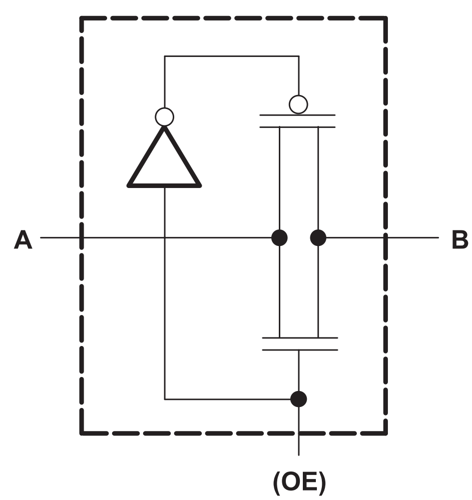
To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pull down resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Device Information[(1)]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74CBTLV3126	SOIC (D) (14)	8.65 mm × 3.91 mm
	TVSOP (DGV) (14)	3.60 mm x 4.40 mm
	TSSOP (PW) (14)	5.00 mm x 4.40 mm
	VQFN (RGY) (14)	4.00 mm x 3.50 mm
	SSOP (DBQ) (16)	4.90 mm x 3.90 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

Simplified Schematic, Each FET Switch



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4 Revision History

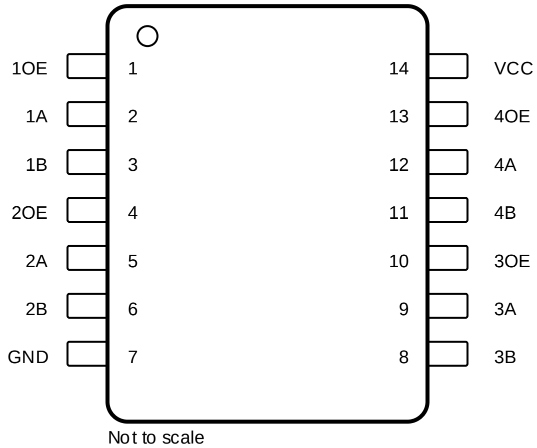
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (October 2003) to Revision J **Page**

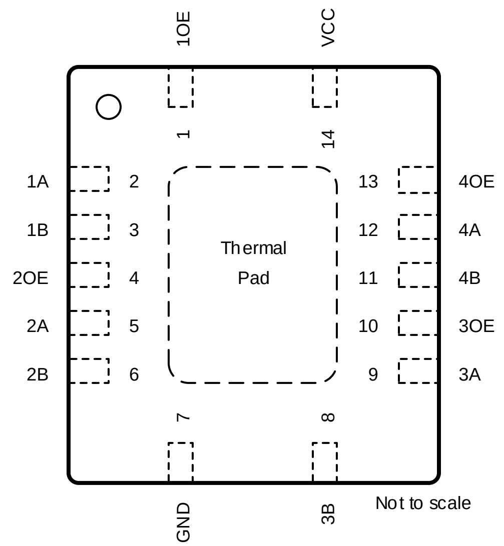
- Added *Device Information* table, *ESD Ratings* table, *Feature Description* section, Device *Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section... 1
- Added V_{IH} MAX values in the *Recommended Operating Conditions* table ... 5

5 Pin Configuration and Functions

D, DGV, PW Package
14 Pin (SOIC, TVSOP, TSSOP)
(Top View)



RGY Package
14 Pin (VQFN)
(Top View)

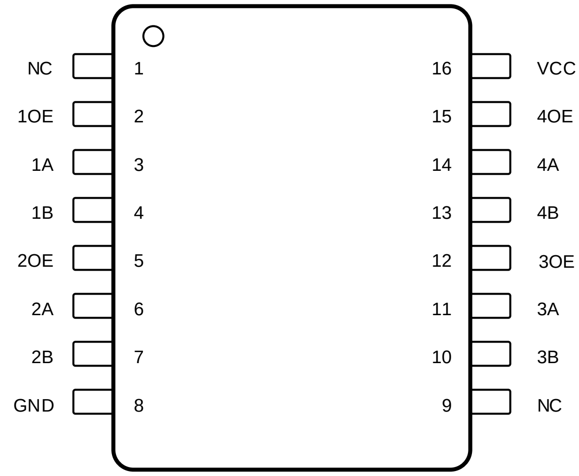


Pin Functions, D, DGV, PW, RGY

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
1OE	1	I	Output Enable, active low
1A	2	I/O	Channel 1 input/output
1B	3	I/O	Channel 1 input/output
2OE	4	I	Output Enable, active low
2A	5	I/O	Channel 2 input/output
2B	6	I/O	Channel 2 input/output
GND	7		Ground
3B	8	I/O	Channel 3 input/output
3A	9	I/O	Channel 3 input/output
3OE	10	I	Output Enable, active low
4B	11	I/O	Channel 4 input/output
4A	12	I/O	Channel 4 input/output
4OE	13	I	Output Enable, active low
V_{CC}	14	P	Power supply

(1) I = input, O = output, I/O = input and output, P = power

DBQ Package
16 Pin (SSOP)
(Top View)



Not to scale

Pin Functions, DBQ

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
NC	1	-	No Connection
1OE	2	I	Output Enable, active low
1A	3	I/O	Channel 1 input/output
1B	4	I/O	Channel 1 input/output
2OE	5	I	Output Enable, active low
2A	6	I/O	Channel 2 input/output
2B	7	I/O	Channel 2 input/output
GND	8	-	Ground
NC	9	-	No Connection
3B	10	I/O	Channel 3 input/output
3A	11	I/O	Channel 3 input/output
3OE	12	I	Output Enable, active low
4B	13	I/O	Channel 4 input/output
4A	14	I/O	Channel 4 input/output
4OE	15	I	Output Enable, active low
V_{CC}	16	P	Power Supply

(1) I = input, O = output, I/O = input and output, P = power

6 Specifications

6.1 Absolute Maximum Ratings[(1)]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range[(2)]		–0.5	4.6	V
$I_{I/O}$	Continuous channel current			128	mA
I_{IK}	Input clamp current	$V_{I/O} < 0$		–50	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions[(1)]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	V_{CC}	V
		V_{CC} = 2.7 V to 3.6 V	2	V_{CC}	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
T_A	Operating free-air temperature		–40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs,* literature number SCBA004.

6.4 Thermal Information

THERMAL METRIC[(1)]		SN74CBTLV3126					UNIT
		D SOIC	DGV TVSOP	PW (TSSOP)	RGY (VQFN)	DBQ (SSOP)	
		14 PINS	14 PINS	14 PINS	14 PINS	16 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	100.6	154.8	123.3	59.6	118.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55.5	64.5	53.0	71.3	66.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.8	88.4	66.3	35.6	62.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	17.0	11.1	9.3	4.2	20.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	56.4	87.4	65.7	35.7	61.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	16.1	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[(1)]	MAX	UNIT
V_{IK}		V_{CC} = 3 V,	I_I = –18 mA				–1.2	V
I_I		V_{CC} = 3.6 V,	V_I = V_{CC} or GND				±1	µA
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 3.6 V				10	µA
I_{CC}		V_{CC} = 3.6 V,	I_O = 0,	V_I = V_{CC} or GND			10	µA
ΔI_{CC}[(2)]	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			300	µA
C_i	Control inputs	V_I = 3 V or 0				2.5		pF
$C_{io(OFF)}$		V_O = 3 V or 0,	OE = GND			7		pF
r_{on}[(3)]		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0	I_I = 64 mA		5	8	Ω
				I_I = 24 mA		5	8	
			V_I = 1.7 V,	I_I = 15 mA		27	40	
		V_{CC} = 3 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 24 mA		5	7	
			V_I = 2.4 V,	I_I = 15 mA		10	15	

(1) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(2) This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.
(3) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

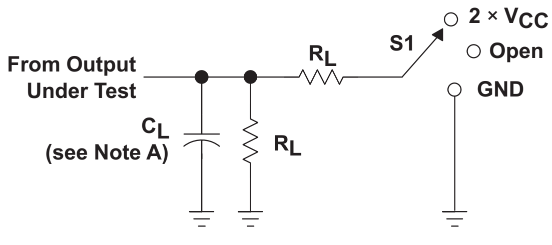
6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}[(1)]	A or B	B or A		0.15		0.25	ns
t_{en}	OE	A or B	1.6	4.5	1.9	4.2	ns
t_{dis}	OE	A or B	1.3	4.7	1	4.8	ns

(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

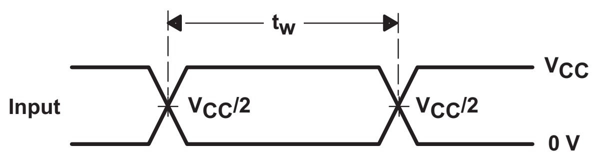
7 Parameter Measurement Information



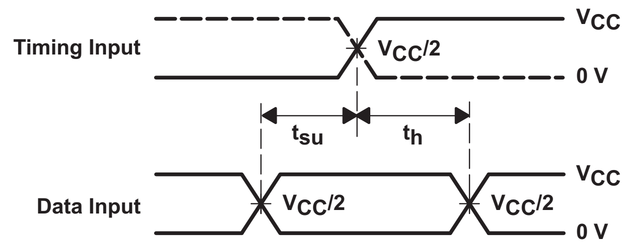
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

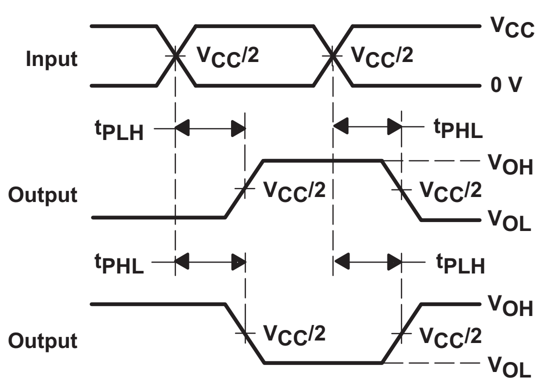
V_{CC}	C_L	R_L	V_Δ
2.5 V ±0.2 V	30 pF	500 Ω	0.15 V
3.3 V ±0.3 V	50 pF	500 Ω	0.3 V



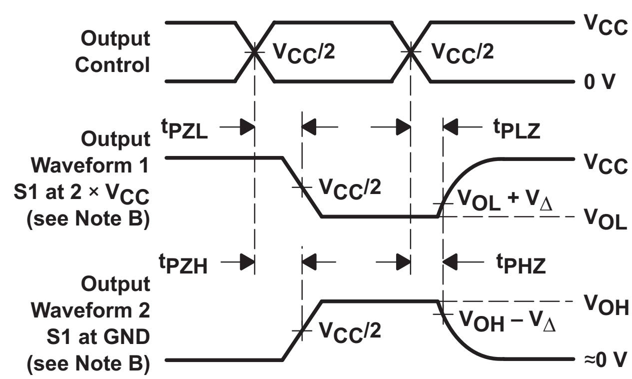
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.

D. The outputs are measured one at a time with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PZL} and t_{PZH} are the same as t_{en}.

G. t_{PLH} and t_{PHL} are the same as t_{pd}.

H. All parameters and waveforms are not applicable to all devices.

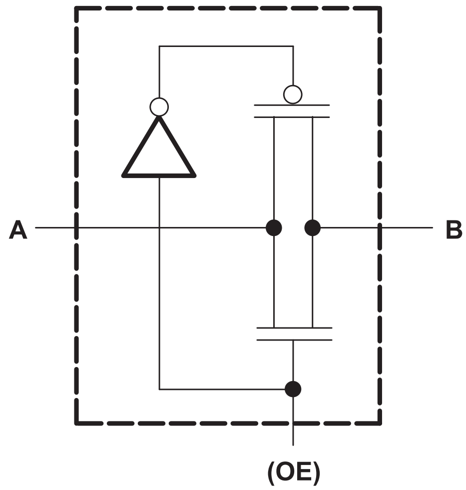
Figure 1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74CBTLV3257 device is a 4-bit 1-of-1 high-speed FET multiplexer and demultiplexer. The low ON-state resistance of the switch allows connections to be made with minimal propagation delay. The FET multiplexers and demultiplexers are disabled when the output-enable (OE) input is high. This device is fully specified for partial-power-down applications using Ioff. The Ioff feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off. To ensure the high-impedance state during power up or power down, OE should be tied to VCC through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

8.2 Functional Block Diagram



8.3 Feature Description

The SN74CBTLV3126 features 5-Ω switch connection between ports, allowing for low signal loss across the switch. Rail-to-rail switching on data I/O allows for full voltage swing outputs. Ioff supports partial-power-down mode operation, protecting the chip from voltages at output ports when it is not powered on. Latch-up performance exceeds 100 mA per JESD 78, Class II.

8.4 Device Functional Modes

8.4.1 Function Table (Each Bus Switch)

Table 1 shows the truth table for the SN74CBTLV3126.

Table 1. Truth Table

INPUT OE	FUNCTION
L	Disconnect
H	A port = B port

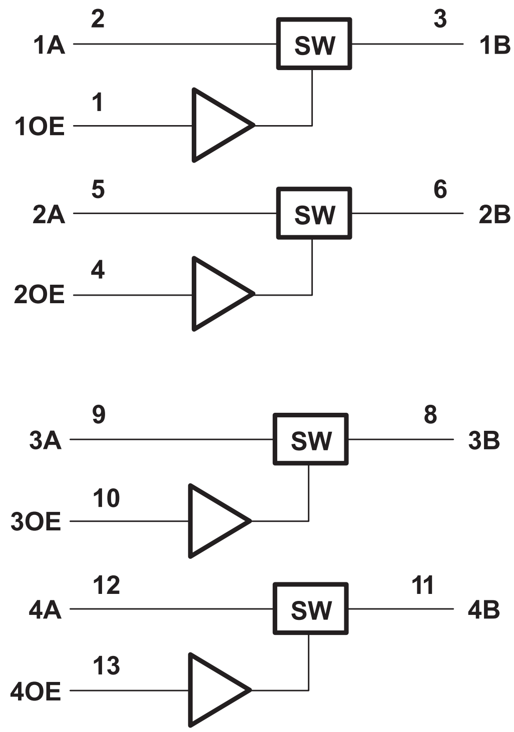


Figure 2. Logic Diagram (Positive Logic)

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

One useful application to take advantage of the SN74CBTLV3126 features is isolating various protocols from a possessor or MCU such as JTAG, SPI, or standard GPIO signals. The device provides excellent isolation performance when the device is powered. The added benefit of powered-off protection allows a system to minimize complexity by eliminating the need for power sequencing in hot-swap and live insertion applications.

9.2 Typical Application

9.2.1 Protocol / Signal Isolation

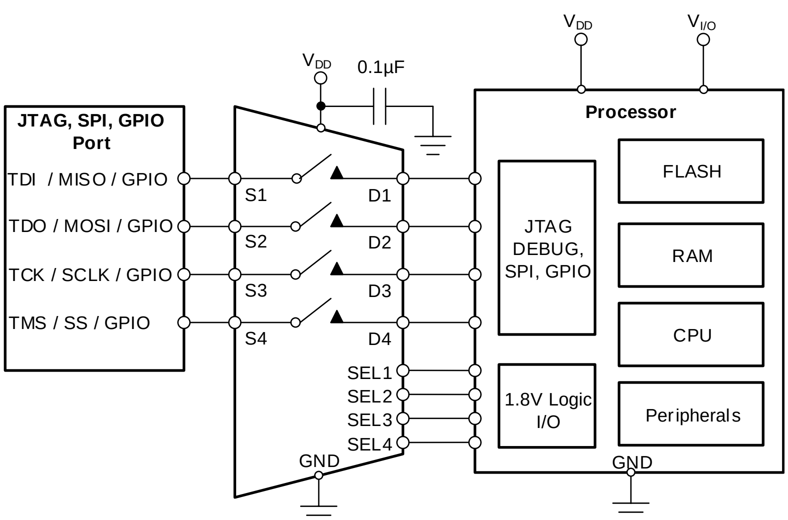


Figure 3. Typical appliction

9.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 2.

Table 2. Design Parameters

PARAMETERS	VALUES
Supply (V_{DD})	3.3 V
Input / Output signal range	0 V to 3.3 V
Control logic thresholds	1.8 V compatible

9.2.1.2 Detailed Design Procedure

The SN74CBTLV3126 can be operated without any external components except for the supply decoupling capacitors. TI recommended that the digital control pins (OE) be pulled up to V_{CC} or down to GND to avoid undesired switch state that could result from the floating pin. All inputs signals passing through the switch must fall within the recommend operating conditions of the SN74CBTLV3126 including signal range and continuous current. For this design example, with a supply of 3.3 V, the signals can range from 0 V to 3.3 V when the device is powered. This example can also utilize the Powered-off Protection feature and the inputs can range from 0 V to 3.3 V when VDD = 0 V.

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the Recommended Operating Conditions table. Each VCC terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF bypass capacitor is recommended. If multiple pins are labeled VCC, then a 0.01-μF or 0.022-μF capacitor is recommended for each VCC because the VCC pins are tied together internally. For devices with dual supply pins operating at different voltages, for example VCC and VDD, a 0.1-μF bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight, and therefore; some traces must turn corners. Figure 4 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

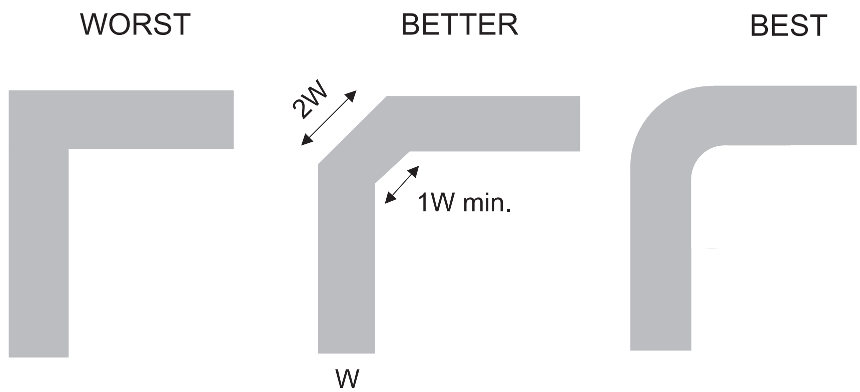


Figure 4. Trace Example

Route the high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Do not route high speed signal traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.

- Avoid stubs on the high-speed signals traces because they cause signal reflections.
- Route all high-speed signal traces over continuous GND planes, with no interruptions.
- Avoid crossing over anti-etch, commonly found with plane splits.
- When working with high frequencies, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in Figure 5.

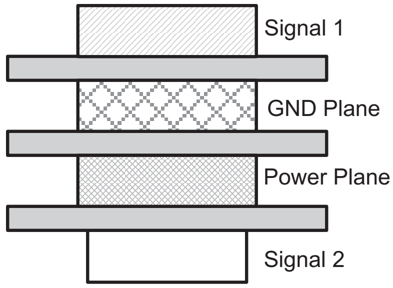


Figure 5. Example Layout

The majority of signal traces must run on a single layer, preferably Signal 1. Immediately next to this layer must be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

Figure 6 illustrates an example of a PCB layout with the SN74CBTLV3126. Some key considerations are:

Layout Guidelines (continued)

Decouple the V_{DD} pin with a 0.1-µF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} supply.

High-speed switches require proper layout and design procedures for optimum performance.

Keep the input lines as short as possible.

Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.

Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

11.2 Layout Example

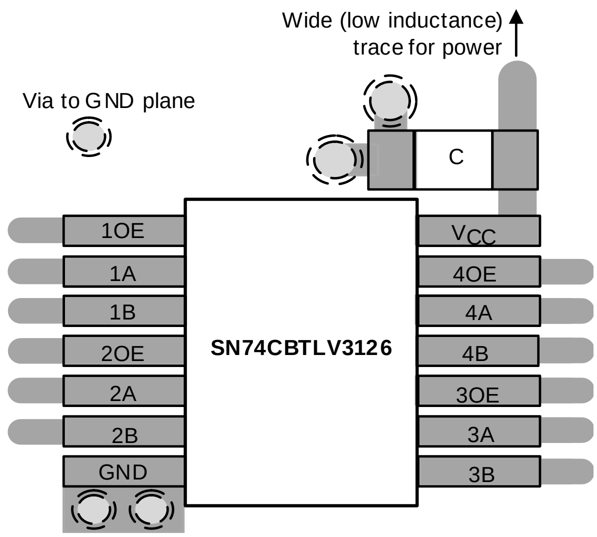


Figure 6. Example Layout

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74CBTLV3126RGYRG4	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL126	Samples
SN74CBTLV3126D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3126	Samples
SN74CBTLV3126DBQR	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL126	Samples
SN74CBTLV3126DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3126	Samples
SN74CBTLV3126DGVR	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL126	Samples
SN74CBTLV3126DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3126	Samples
SN74CBTLV3126PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL126	Samples
SN74CBTLV3126PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL126	Samples
SN74CBTLV3126RGYR	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL126	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

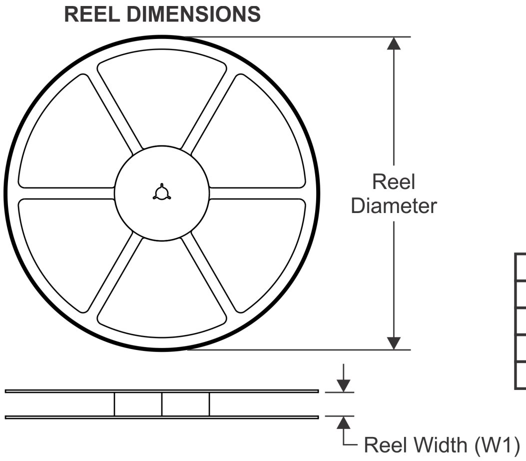
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

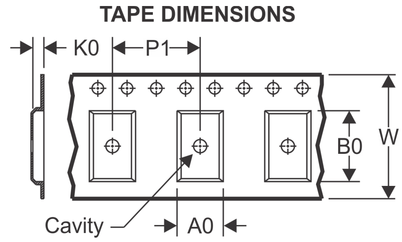
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

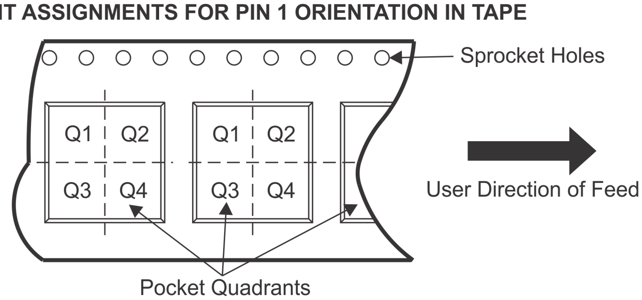
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





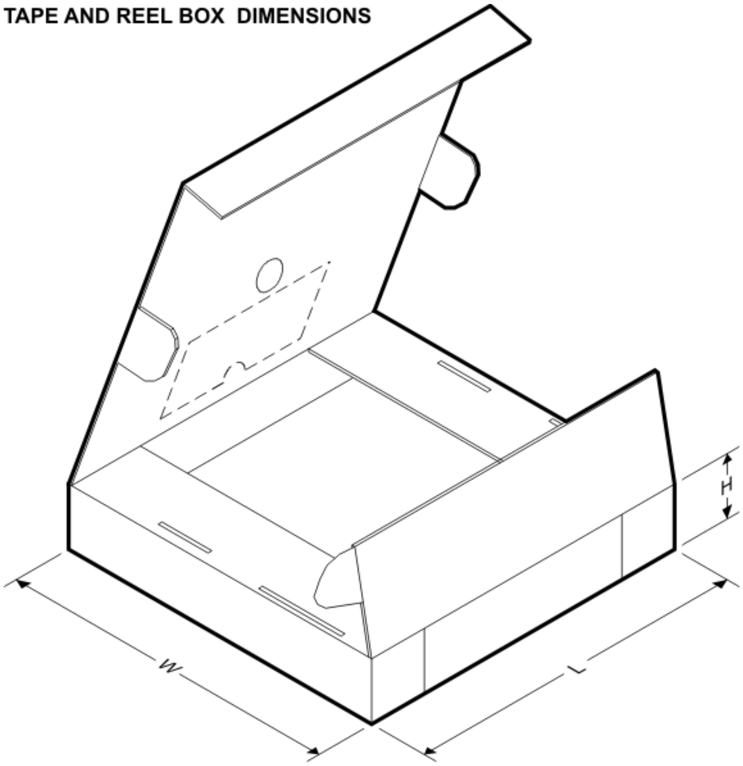
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBTLV3126DBQR	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
SN74CBTLV3126DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74CBTLV3126DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CBTLV3126PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CBTLV3126RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

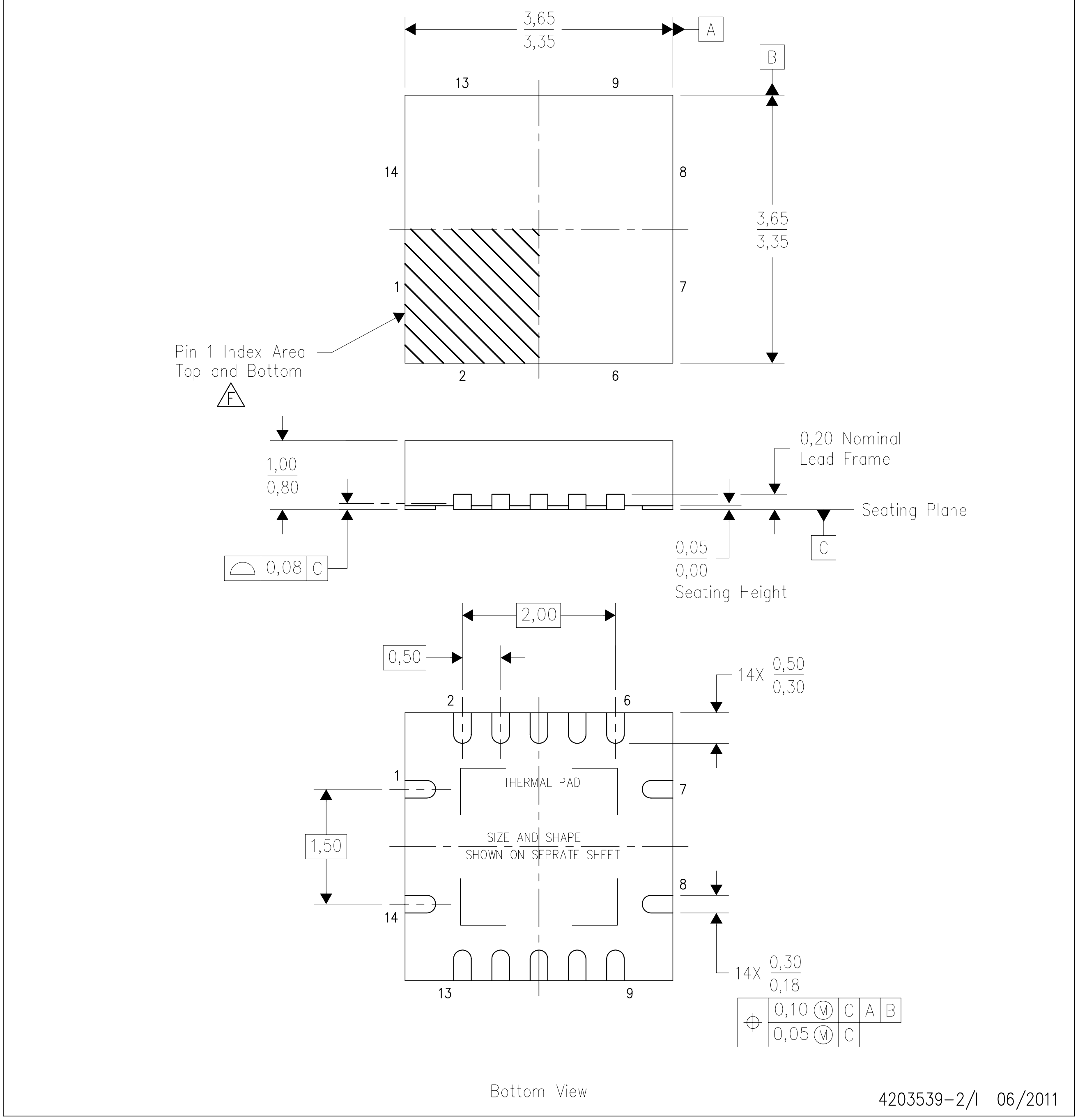
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBTLV3126DBQR	SSOP	DBQ	16	2500	340.5	338.1	20.6
SN74CBTLV3126DGVR	TVSOP	DGV	14	2000	367.0	367.0	35.0
SN74CBTLV3126DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74CBTLV3126PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74CBTLV3126RGYR	VQFN	RGY	14	3000	367.0	367.0	35.0

RGY (S-PVQFN-N14) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. QFN (Quad Flatpack No-Lead) package configuration.

D. The package thermal pad must be soldered to the board for thermal and mechanical performance.

E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

G. Package complies to JEDEC MO-241 variation BA.

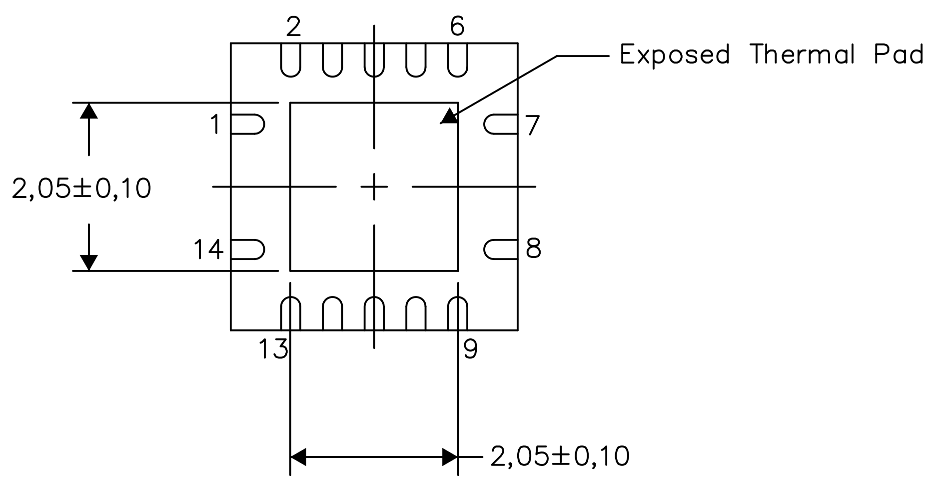
RGY (S-PVQFN-N14) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



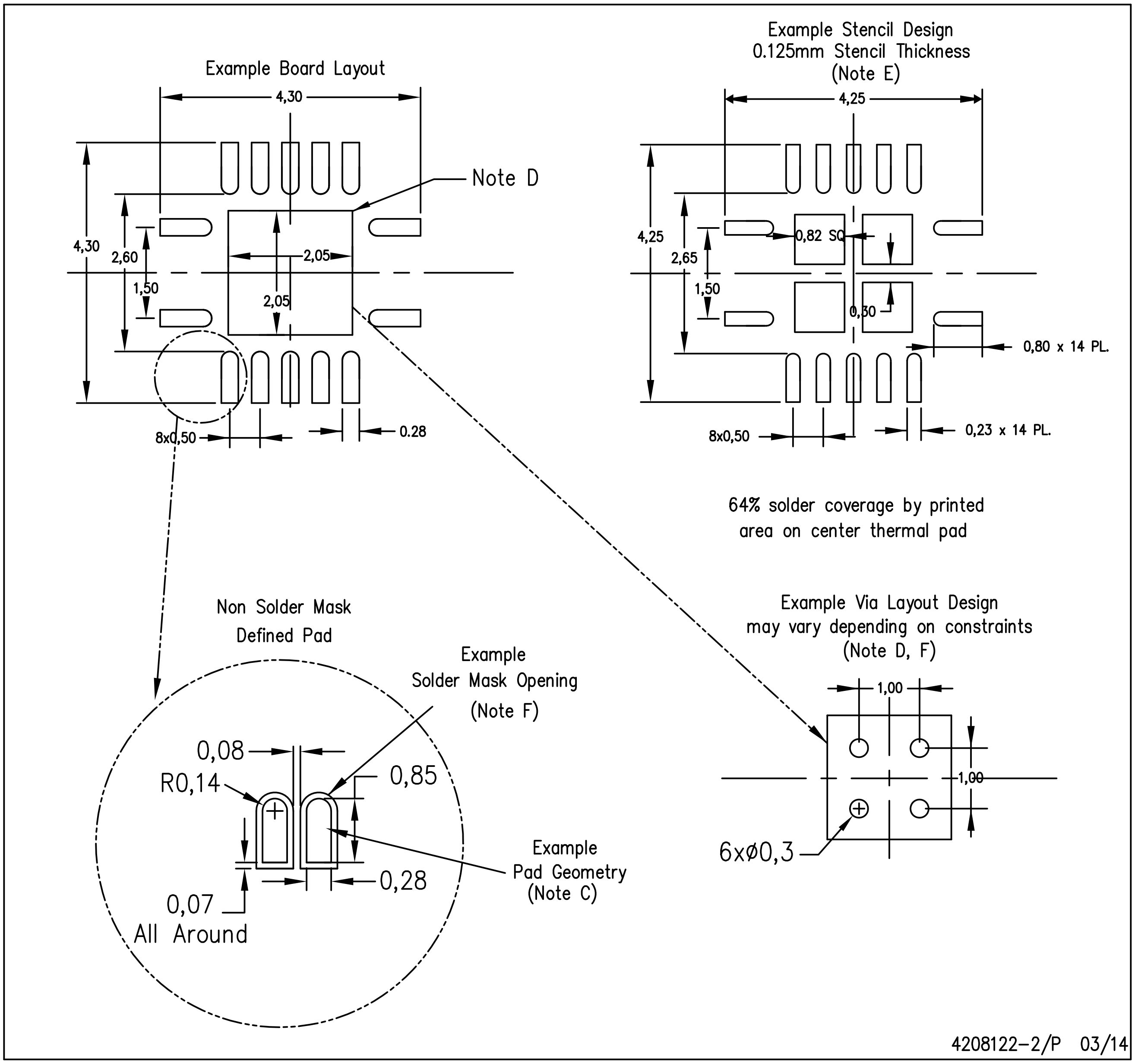
Bottom View

Exposed Thermal Pad Dimensions

4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters

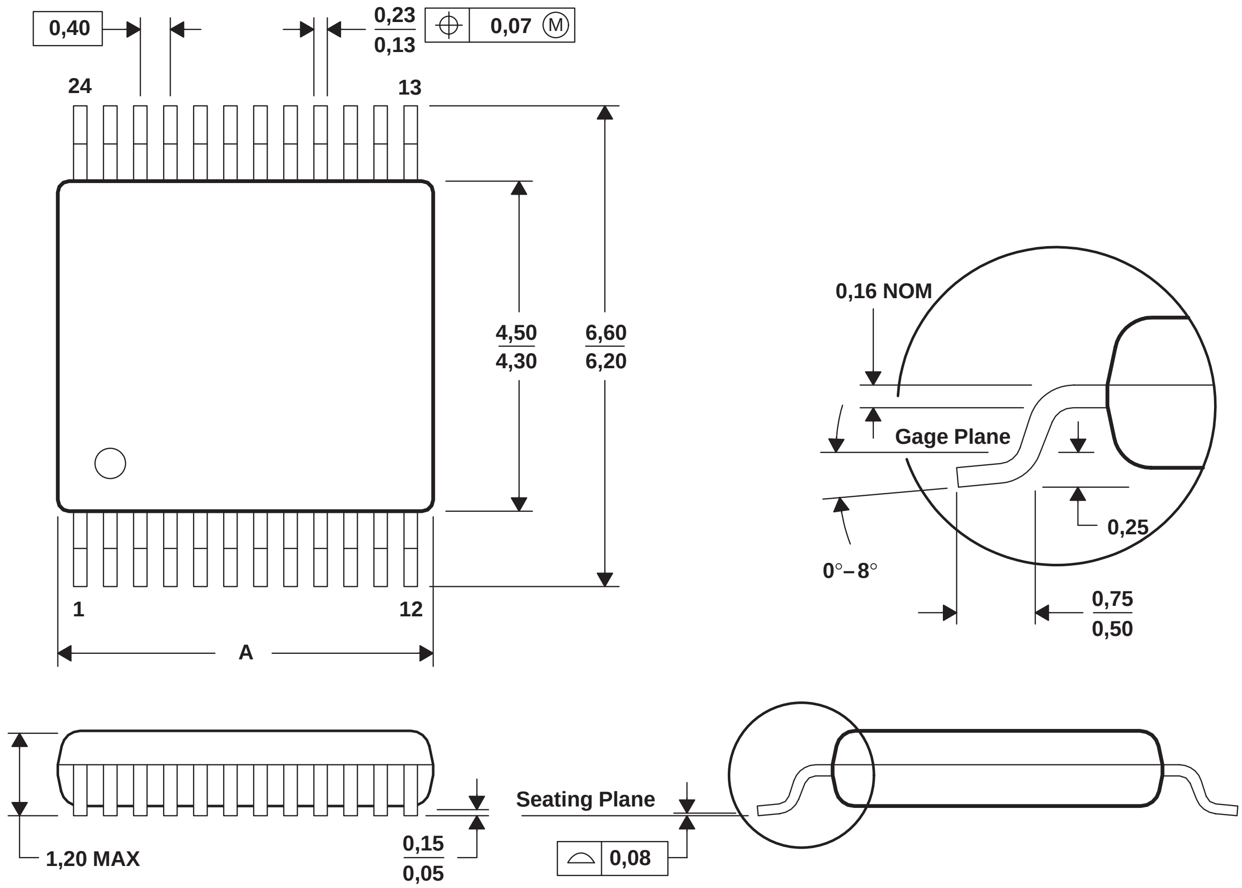
RGY (S-PVQFN-N14) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

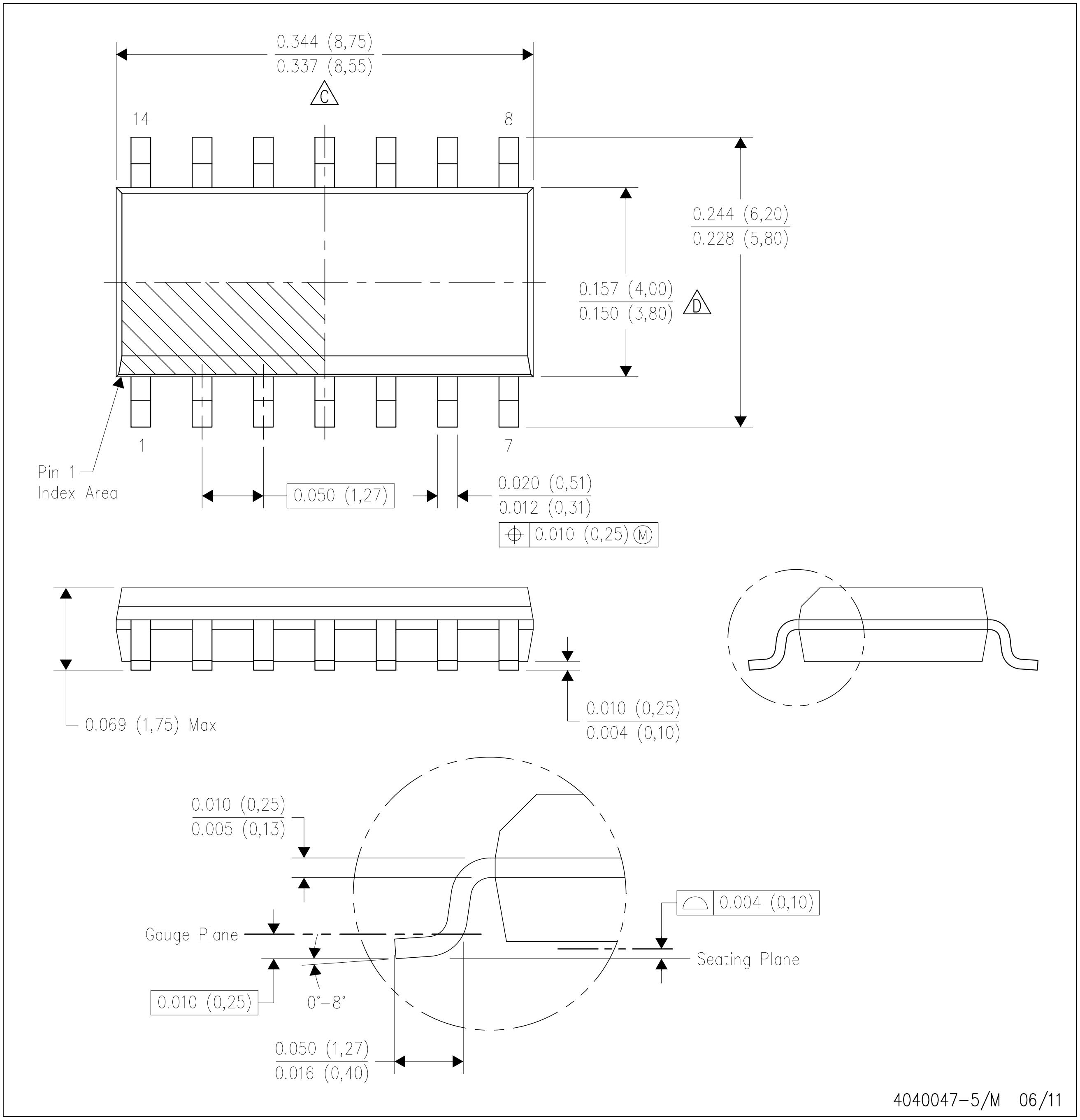


PINS ** / DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

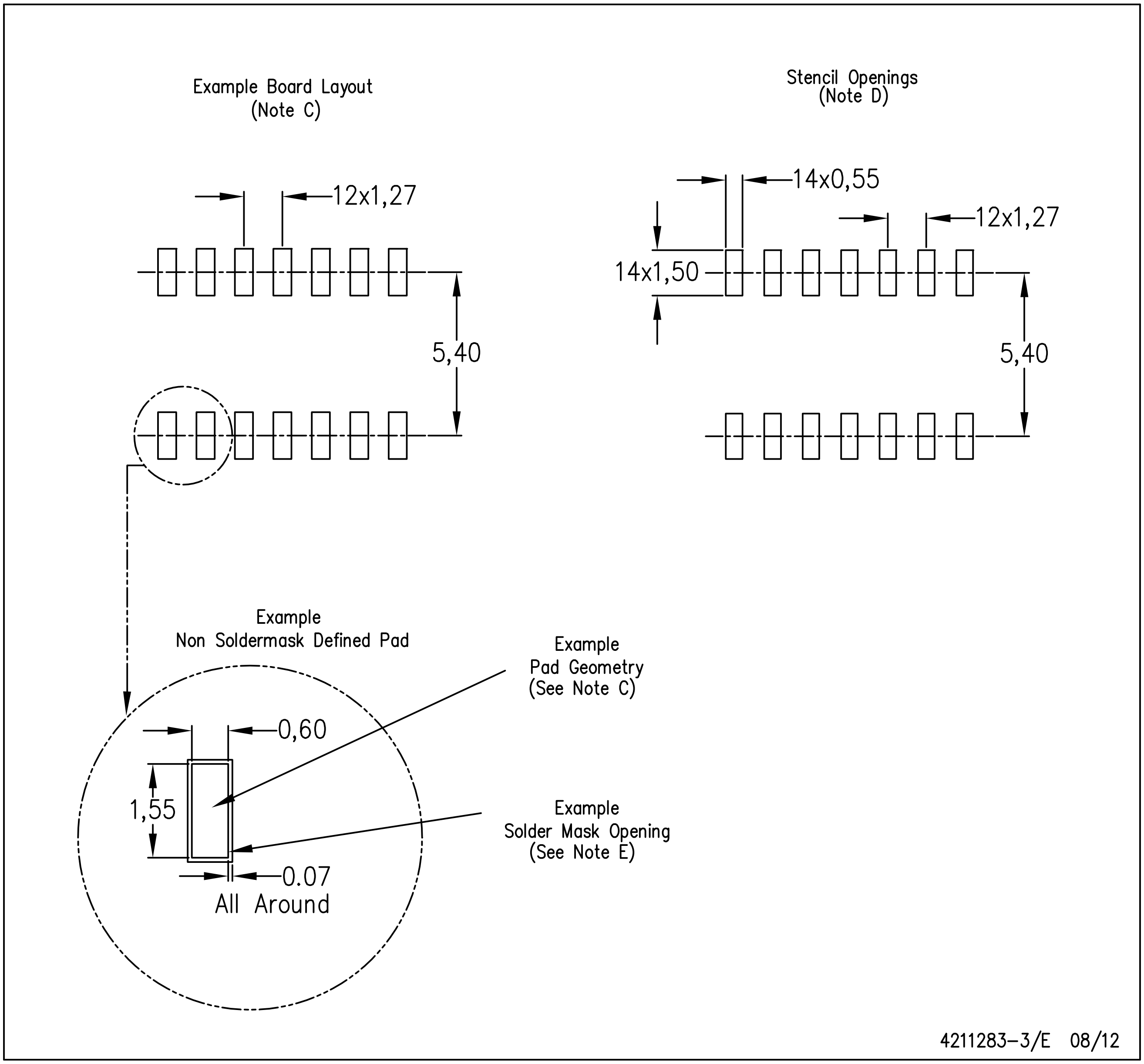
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

D (R-PDSO-G14) PLASTIC SMALL OUTLINE



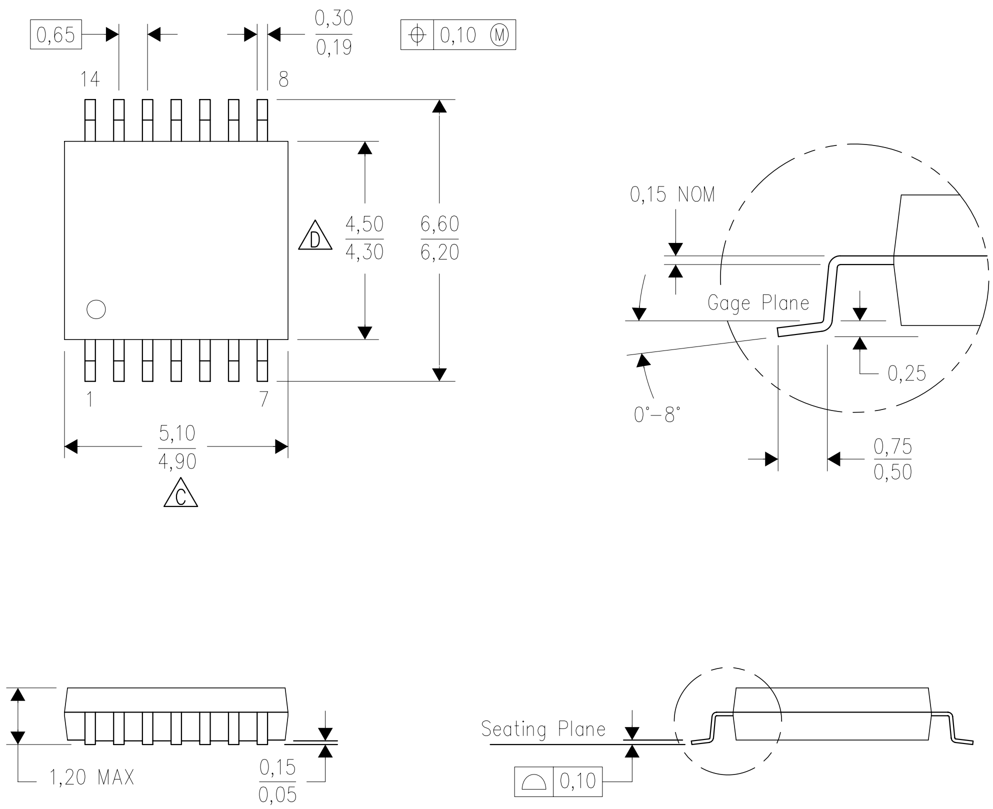
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

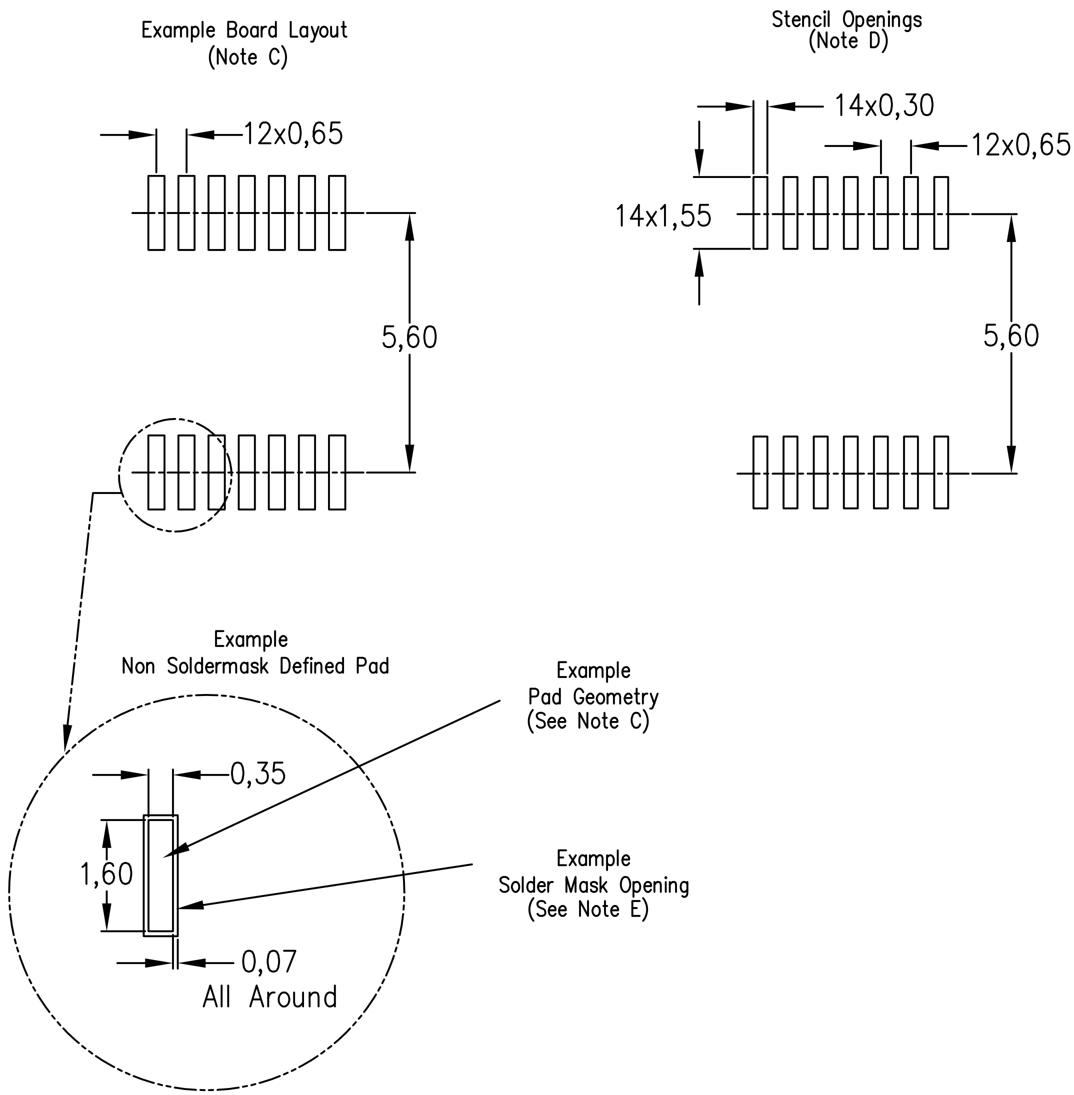
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

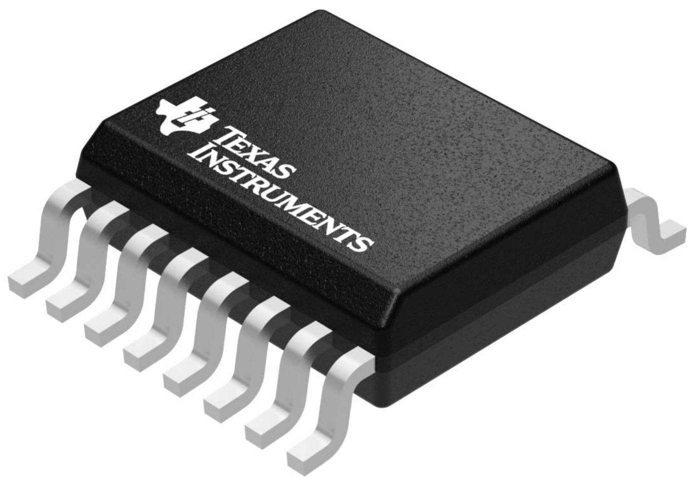
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



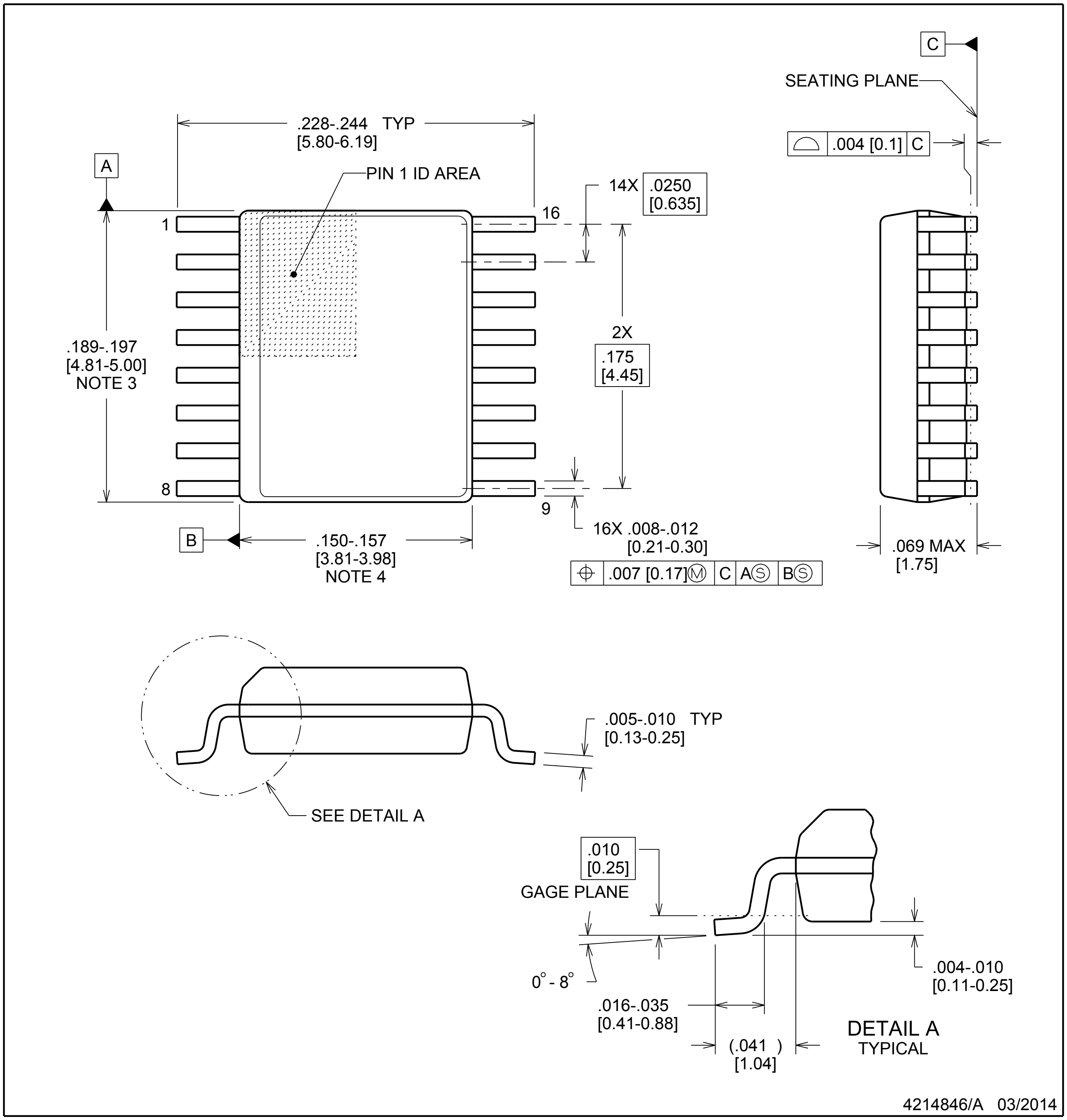
4211284–2/G 08/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



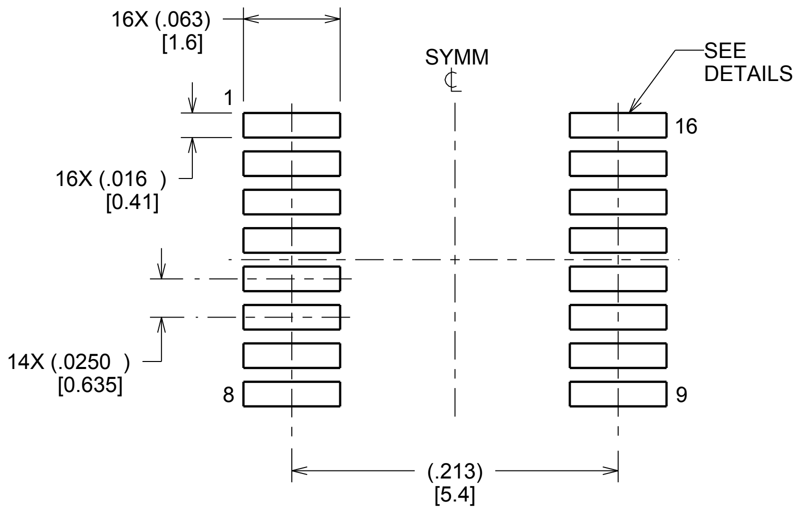
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4073301-2/I

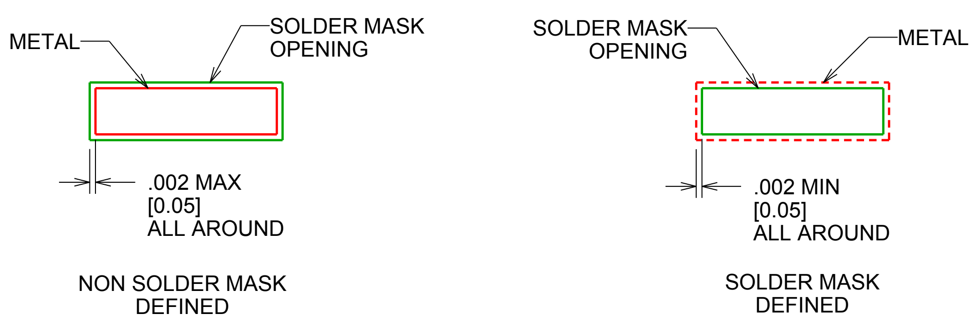


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

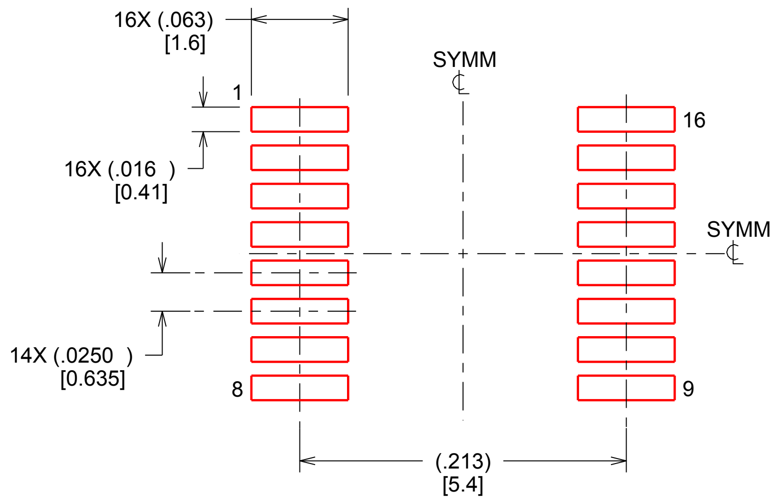


SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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