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FAIRCHILD SEMICONDUCTOR®

June 2013

FAN5903
Buck Converter with Bypass Mode for 3G / 3.5G / 4G PAs

Features

- 2.7 V to 5.5 V Input Voltage Range
- V_{OUT} Range from 0.4 V to 3.5 V (or V_{IN})
- Small Form Factor Inductor
  - 2012 470 nH or 540 nH for Minimal PCB Area
  - 2520 1.0 µH for Higher Efficiency
- Bypass Dropout at 500 mA, 60 mV Typical
- 100% Duty Cycle for Low Dropout Operation
- Input Under-Voltage Lockout / Thermal Shutdown
- 1.34 mm x 1.29 mm, 9-Bump, 0.4 mm-Pitch, Wafer-Level Chip-Scale Package (WLCSP)
- 3 MHz / 6 MHz Selectable Switching Frequency to Facilitate System Optimization
- High-Efficiency PFM Operation at Low Power
- Sleep Mode for Very Low I_Q Operation
- Up to 96% Efficient Synchronous Operation at High-Power Conditions
- 10 µs Output Voltage Step Response for Early Power Loop Settling

Applications

- Dynamic Supply Bias for 3G/3.5G and 4G PAs
- Power Supply for WCDMA/LTE PAs

Resources

For more information or a full copy of this datasheet, please contact a Fairchild representative.

Description

FAN5903 is a high-efficiency, low-noise, synchronous, step-down, DC-DC converter designed for powering 3G / 3.5G / 4G RF Power Amplifiers (PAs) in handsets and other mobile applications.

The output voltage may be dynamically varied from 0.40 V to 3.50 V, proportional to an analog input V_{CON}, ranging from 0.16 V to 1.40 V provided by an external DAC. This allows the PA to be supplied with the voltage that enables maximum power-added efficiency.

An integrated bypass FET automatically switches on when battery voltage drops close to the desired output voltage (V_{OUT} = V_{BAT} - 200 mV). The DC-DC switches back to Synchronous Mode when the voltage dropout exceeds 375 mV. The integrated bypass FET is also enabled when V_{CON} is nominally greater than to 1.5 V.

The FAN5903 offers fast transition times, enabling changes to the output voltage in less than 10 µs for power transitions. Moreover, a Current-Mode control loop with fast transient response ensures excellent line and load regulation.

Light-load efficiency is optimized by operating in PFM Mode for load currents typically less than 100 mA.

The switching frequency may be set to 3 MHz or 6 MHz, enabling further optimization of system performance. The FAN5903 typically uses a single, small-form-factor inductor of 470 nH or 540 nH. Efficiency may be further optimized using a 1.0 µH inductor when running at 3 MHz.

When output regulation is not required, the FAN5903 may be placed in Sleep Mode by setting V_{CON} nominally to 50 mV. This ensures a very low I_Q (<70 µA) while enabling a fast return to output regulation. The FAN5903 enables significant current reduction and increased talk time and is available in a 1.34 mm x 1.29 mm, 9-bump, 0.40 mm-pitch, WLCSP package.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN5903UCX	-40 to +85°C	1.34 mm x 1.29 mm, 9-bump, 0.4 mm Pitch, Wafer-Level Chip-Scale Package (WLCSP)	Tape and Reel

Application Diagrams

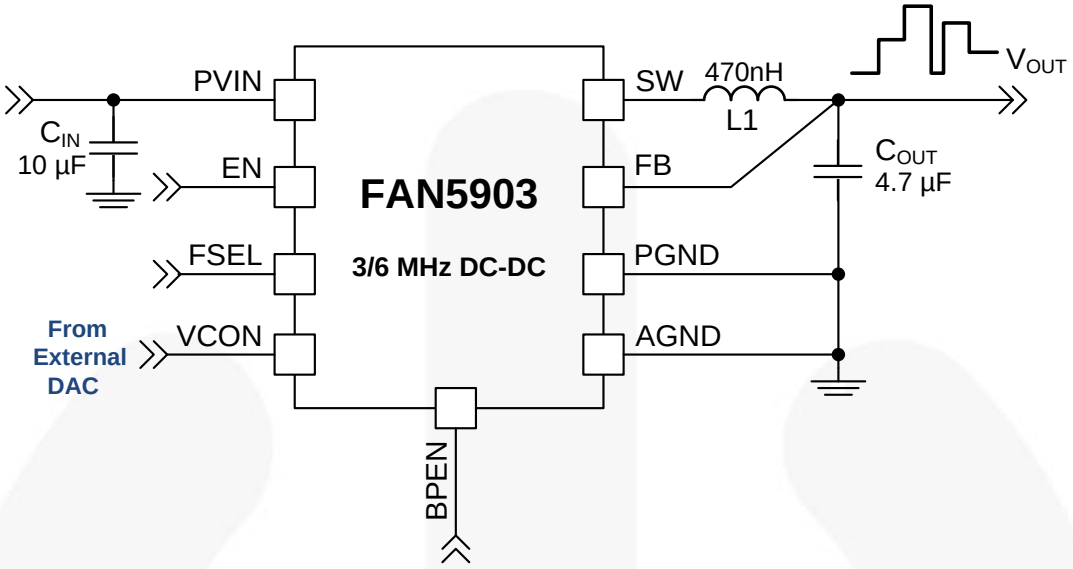


Figure 1. Application Circuit

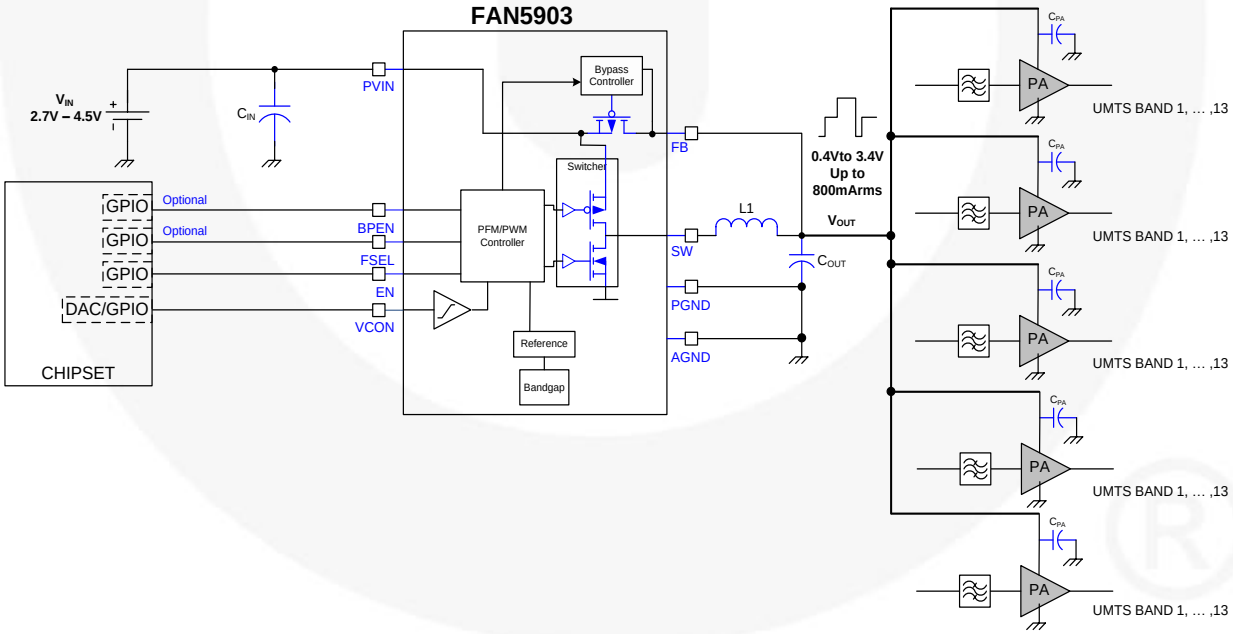


Figure 2. Typical Application with a 5-Band WCDMA / HSPA PA System

Pin Configuration

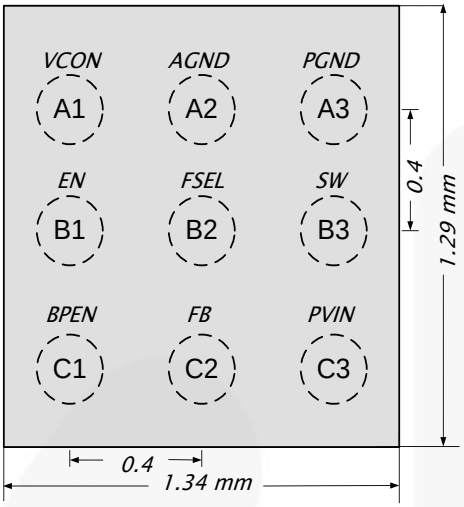


Figure 3. Top-Through View, Bumps Face Down

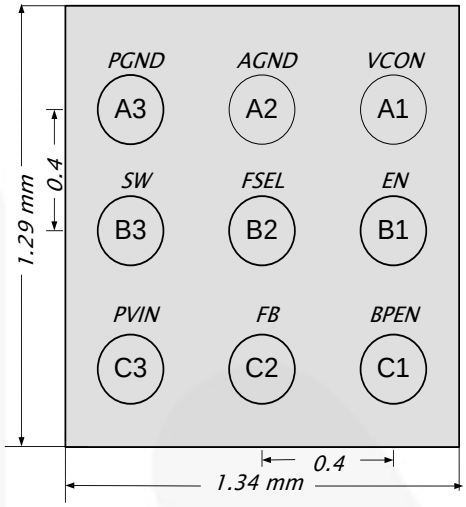


Figure 4. Top-Through View, Bumps Face Up

Pin Definitions

Pin #	Name	Description
A1	VCON	Analog control pin. Shield signal routing against noise.
A2	AGND	Analog ground, reference ground for the IC. Follow PCB routing notes for connecting this pin.
A3	PGND	Power ground of the internal MOSFET switches. Follow routing notes for connections between PGND and AGND.
B1	EN	Enables switching when HIGH, Shutdown Mode when LOW. This pin should not be left floating.
B2	FSEL	Switching frequency select. When FSEL is LOW, the DC-DC operates at 6 MHz. When FSEL is HIGH, the DC-DC operates at 3 MHz. This pin should not be left floating.
B3	SW	Switching node of the internal MOSFET switches. Connect to output inductor.
C1	BPEN	Force bypass transistor when HIGH; auto-bypass when LOW. This pin should not be left floating.
C2	FB	Output voltage-sense pin. Connect to VOUT to establish feedback path for regulation point.
C3	PVIN	Supply voltage input to the internal MOSFET switches; connect to input power source.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}	PVIN		-0.3	6.0	V
	Voltage On Any Other Pin		-0.3	PV_{IN} + 0.3	
T_J	Junction Temperature		-40	+125	°C
T_{STG}	Storage Temperature		-65	+150	°C
T_L	Lead Soldering Temperature (10 Seconds)			+260	°C
ESD	Electrostatic Discharge Protection	Human Body Model, JESD22-A114	2.0		kV
		Charged Device Model, JESD22-C101	1.5		

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{IN}	Supply Voltage Range		2.7		5.5	V
V_{OUT}	Output Voltage Range		0.35		$\leq V_{IN}$	V
I_{OUT_BYP}	Output Current (Bypass Mode)				2.4	A
I_{OUT_DCDC}	Output Current (DCDC Mode)				1.0	A
L1	Inductor	f_{SW} = 6 MHz		470		nH
				540		
		f_{SW} = 3 MHz		1.00		µH
C_{IN}	Input Capacitor[1]			10		µF
C_{OUT}	Output Capacitor		2.2	4.7		µF
T_A	Operating Ambient Temperature Range		-40		+85	°C
T_J	Operating Junction Temperature Range		-40		+125	°C

Note:

1. A large enough input capacitor value is required for limiting the input voltage drop during bursts, bypass transitions, or during large output voltage transitions. Ensure the input capacitor value is greater than the output capacitor's. *See the inrush current specifications below.*

Dissipation Ratings

Symbol	Parameter	Min.	Typ.	Max.	Unit
Θ_{JA}	Junction-to-Ambient Thermal Resistance[2]		110		°C/W

Note:

2. Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer 2s2p boards in accordance to JESD51- JEDEC standard. Special attention must be paid not to exceed junction temperature $T_{J(max)}$ at a given ambient temperate T_A.

Electrical Characteristics

V_{IN} = V_{OUT} + 0.6 V, I_{OUT} = 200 mA, EN = V_{IN}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{IN} = 3.7 V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Power Supplies						
V_{IN}	Input Voltage Range	I_{OUT} ≤ 800 mA	2.7		5.5	V
I_{SD}	Shutdown Supply Current	EN = 0 V		1	3	µA
I_Q	Quiescent Current	Sleep Enabled		70		µA
V_{UVLO}	Under Voltage Lockout Threshold	V_{IN} Rising	2.30	2.45	2.60	V
		Hysteresis		175		mV
V_{IH}	Logic Threshold Voltage: EN, FSEL and BPEN	Input HIGH Threshold	1.2			V
V_{IL}		Input LOW Threshold			0.5	V
I_{EN}	EN Input Bias Current	EN = V_{IN} or GND		0.01	1.00	µA
Oscillator						
f_{SW}	Average Oscillator Frequency	FSEL = 0	5.4	6.0	6.6	MHz
f_{SW}	Average Oscillator Frequency	FSEL = 1	2.7	3.0	3.3	MHz
DC-DC Mode						
R_{DSON}	PMOS On Resistance[3]	V_{IN} = V_{GS} = 3.7 V		230		mΩ
	NMOS On Resistance[3]	V_{IN} = V_{GS} = 3.7 V		150		mΩ
I_{LIMp}	P-Channel Current Limit		1.2	1.5	1.8	A
I_{LIMn}	N-Channel Current Limit		0.8	1.1	1.4	A
V_{OUT_MIN}	Minimum Output Voltage	V_{CON} = 0.16 V	0.35	0.40	0.45	V
V_{OUT_MAX}	Maximum Output Voltage	V_{CON} = 1.40 V	3.45	3.50	3.55	V
Gain	Gain in Control Range 0.16V to 1.40V			2.5		
V_{OUT_ACC}	V_{OUT} Accuracy	Ideal = 2.5 x V_{CON}	-50		+50	mV
Bypass Mode						
R_{FET}	Bypass FET Resistance[4]	V_{IN} = V_{GS} = 3.7 V		210		mΩ
ΔV_{OUT_BP}	Bypass Mode Output Voltage Drop	I_{OUT} = 500 mA		60		mV
Output Regulation						
V_{OUT_RLine}	V_{OUT} Line Regulation			±5		mV
V_{OUT_RL}	V_{OUT} Load Regulation	I_{OUT} ≤ 800 mA		±25		mV
$V_{CON\_SL\_EN}$	V_{CON} Sleep Mode Enter	V_{CON} Voltage that Forces Very Low I_Q Sleep Mode	50			mV
$V_{CON\_SL\_EX}$	V_{CON} Sleep Mode Exit	V_{CON} Voltage that Exits Sleep Mode			135	mV
$V_{CON\_BP\_EN}$	V_{CON} Forced Bypass Mode Enter	V_{CON} Voltage that Forces Bypass, V_{IN} = 2.70 V – 4.75 V	1.6			V
$V_{CON\_BP\_EX}$	V_{CON} Forced Bypass Mode Exit	V_{CON} Voltage that Exits Forced; Bypass, V_{IN} = 2.70 V – 4.75 V			1.4	V
V_{BP_ThH}	Voltage Threshold to Enter Bypass Mode	V_{IN} – V_{OUT}	160	200	240	mV
V_{BP_ThL}	Voltage Threshold to Exit Bypass Mode	V_{IN} – V_{OUT}	320	375	440	mV
T_{OTP}	Over-Temperature Protection	Rising Temperature		+150		°C
		Hysteresis		+20		

Electrical Characteristics

V_{IN} = V_{OUT} + 0.6 V, I_{OUT} = 200 mA, EN = V_{IN}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{IN} = 3.7 V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Timings						
t_{SS}	Startup Time	V_{IN} = 3.7 V, V_{OUT} from 0 V to 3.1 V, C_{OUT} = 4.7 µF, 10 V, X5R		30	40	µs
t_{SP_en}	Sleep Mode Enter Time	V_{CON} < 50 mV		40		µs
t_{SP_ex}	Sleep Mode Exit Time	V_{CON} ≥ 135 mV		11		µs
$t_{DC\text{-}DC\_TR}$	V_{OUT} Step Response Rise Time(3)	V_{OUT} from 5% to 95%, ΔV_{OUT} < 2 V (1.4 V – 3.4 V) , R_{LOAD} ≤ 7 Ω			10	µs
$t_{DC\text{-}DC\_TF}$	V_{OUT} Step Response Fall Time(3)	V_{OUT} from 95% to 5%, ΔV_{OUT} < 2 V (3.4 V – 1.4 V), R_{LOAD} ≤ 7 Ω			12	µs
$t_{DC\text{-}DC\_CL}$	Maximum Allowed Time for Consecutive Current Limits(5)			40		µs
t_{DCDC_CLR}	Consecutive Current Limit Recovery Time(3)			180		µs

Notes:

3. Guaranteed by design; not tested in production.
4. Bypass FET resistance does not include the PFET R_{DSON} and inductor DCR in parallel with the bypass FET in Bypass Mode.
5. Protects part under short circuit conditions. After 40 µs, operation halts and restarts after 180 µs. Under heavy capacitive loads, V_{CON} slew rate may be reduced to avoid consecutive current limits. Under typical conditions for a 3 V change at the output, a capacitive only load of up to 40 µF is supported, assuming a step at the V_{CON} input.

Typical Characteristics

Unless otherwise noted, V_{IN} = EN = 3.7 V, L1 = 1.0 µH, C_{LOAD} = 4.7 µF, and T_A = +25°C.

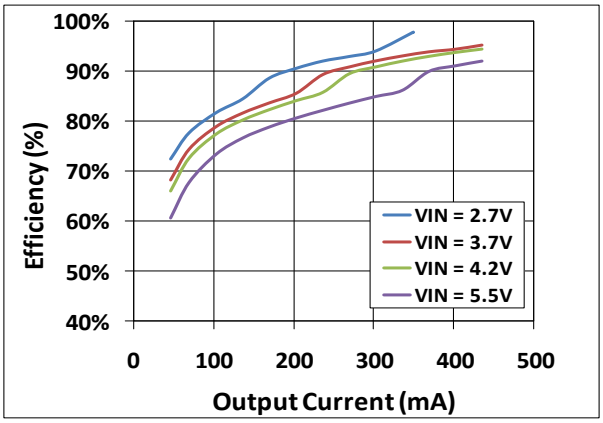


Figure 5. Efficiency vs. Output Current vs. Input Voltage, f_{SW} = 6 MHz, R_{PA} = 7 Ω

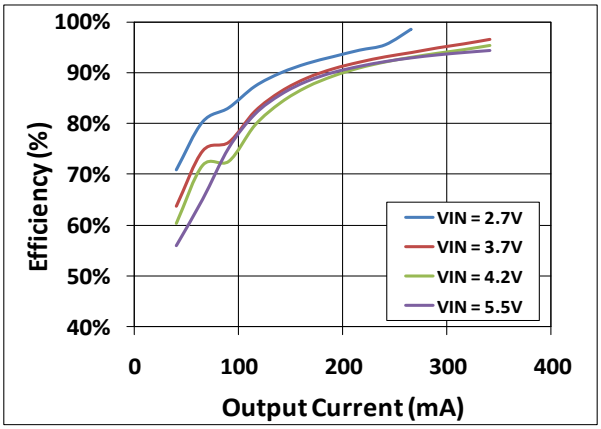


Figure 6. Efficiency vs. Output Current vs. Input Voltage, f_{SW} = 6 MHz, R_{PA} = 10 Ω

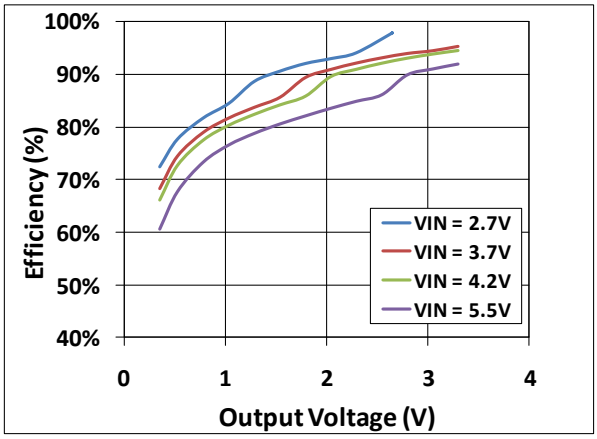


Figure 7. Efficiency vs. Output Voltage vs. Input Voltage, f_{SW} = 6 MHz, R_{PA} = 7 Ω

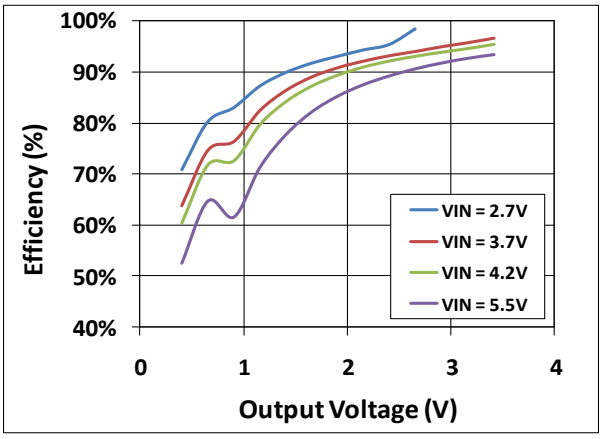


Figure 8. Efficiency vs. Output Voltage vs. Input Voltage, f_{SW} = 6 MHz, R_{PA} = 10 Ω

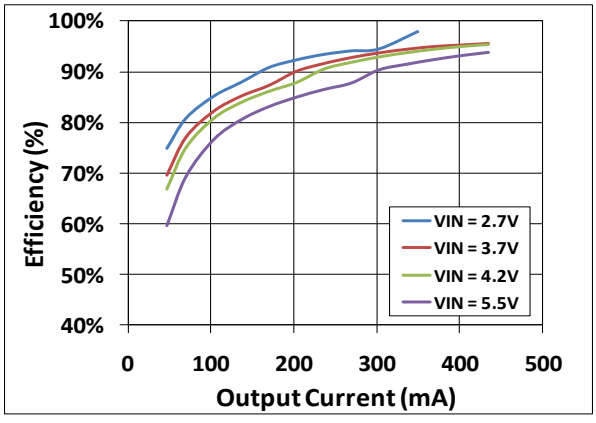


Figure 9. Efficiency vs. Output Current vs. Input Voltage, f_{SW} = 3 MHz, R_{PA} = 7 Ω

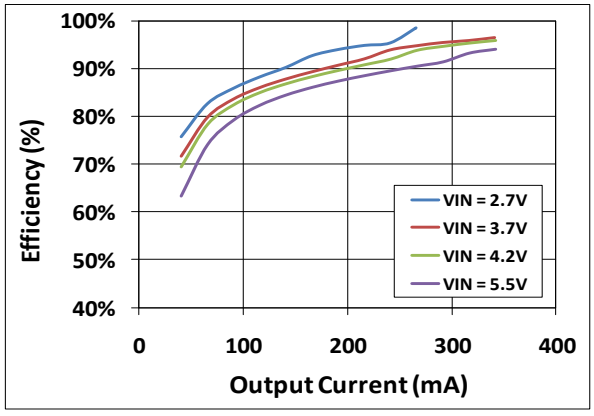


Figure 10. Efficiency vs. Output Current vs. Input Voltage, f_{SW} = 3 MHz, R_{PA} = 10 Ω

Typical Characteristics

Unless otherwise noted, V_{IN} = EN = 3.7 V, L1 = 1.0 µH, C_{LOAD} = 4.7 µF, and T_A = +25°C.

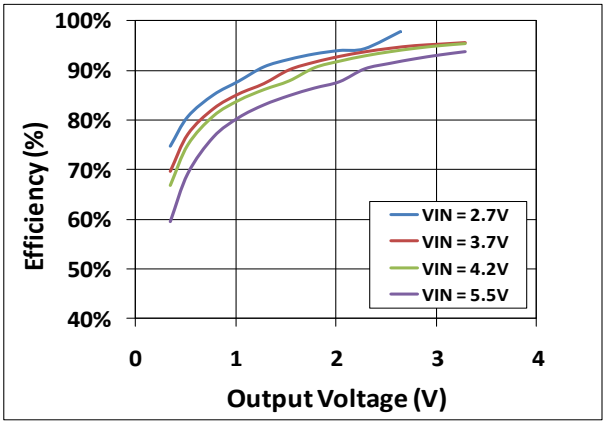


Figure 11. Efficiency vs. Output Voltage vs. Input Voltage, f_{SW} = 3 MHz, R_{PA} = 7 Ω

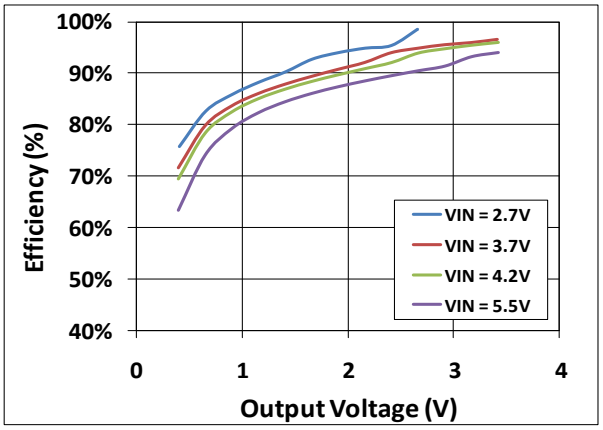


Figure 12. Efficiency vs. Output Voltage vs. Input Voltage, f_{SW} = 3 MHz, R_{PA} = 10 Ω

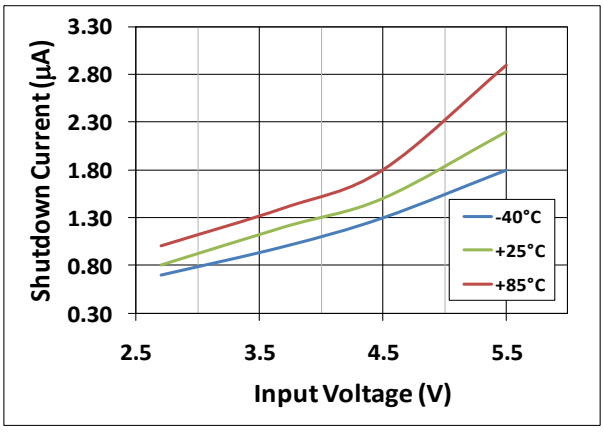


Figure 13. Shutdown Current vs. Input Voltage vs. Temperature

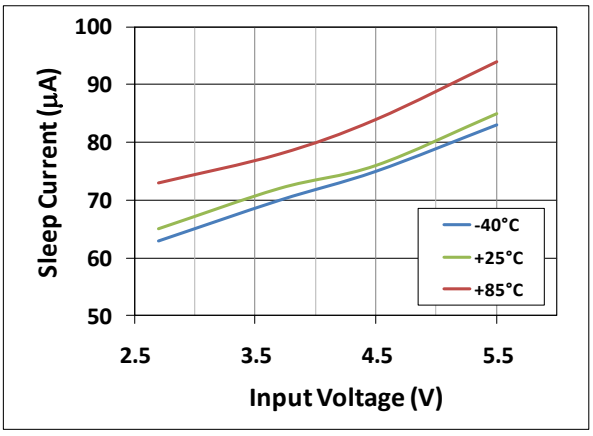


Figure 14. Sleep Mode Current vs. Input Voltage vs. Temperature

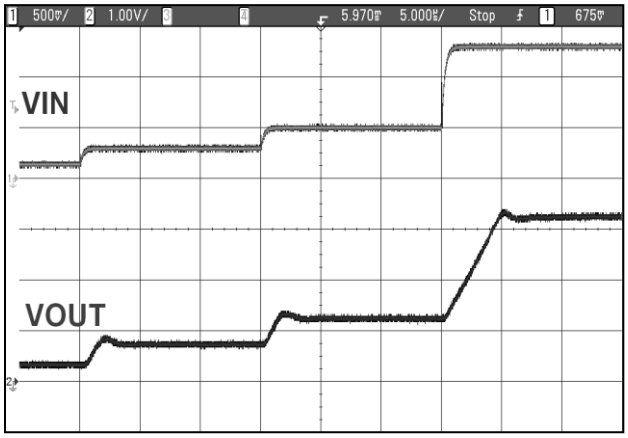


Figure 15. Rise Times for 300 mV, 500 mV, and 2 V ΔV_{OUT} (V_{IN} = 3.7 V)

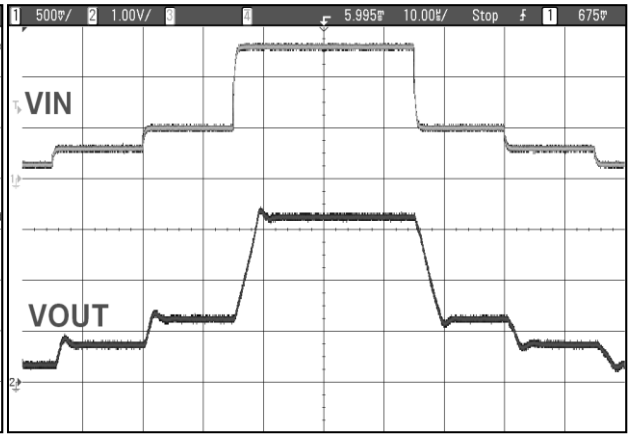


Figure 16. Rise Times for 300 mV, 500 mV, and 2 V ΔV_{OUT} (V_{IN} = 3.7 V)

Typical Characteristics

Unless otherwise noted, V_{IN} = EN = 3.7 V, L1 = 1.0 µH, C_{LOAD} = 4.7 µF, and T_A = +25°C.

Figure 17. Line Transient V_{IN} = 3.7 V to 4.2 V, V_{OUT} = 2.5 V, 10 Ω Load, 50 µs/div.

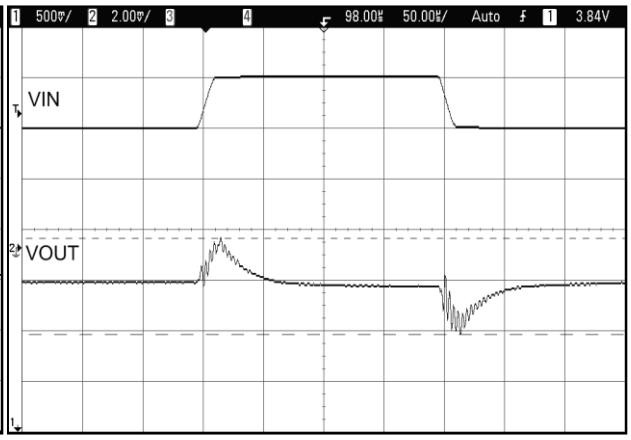


Figure 18. Line Transient V_{IN} = 3.7 V to 4.2 V, V_{OUT} = 1.0 V, 10 Ω Load, 50 µs/div.

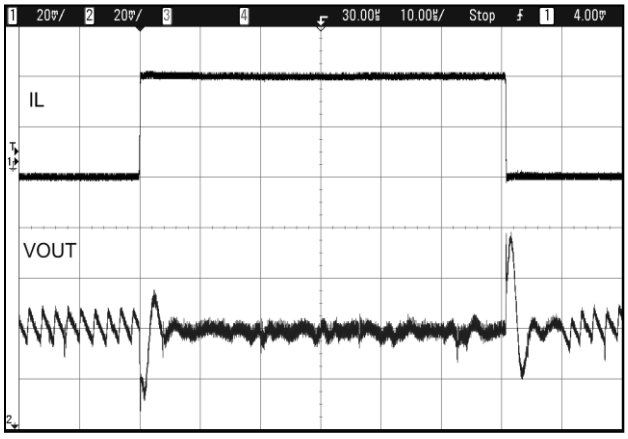


Figure 19. Load Transient, 0 mA to 400 mA, V_{OUT} = 1.0 V

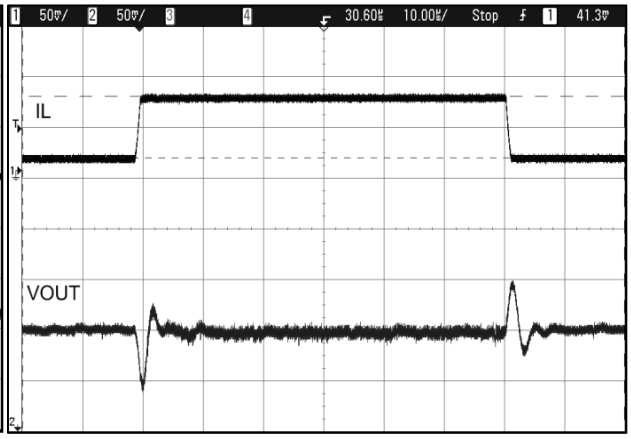


Figure 20. Load Transient, 200 mA to 800 mA, V_{OUT} = 1.0 V

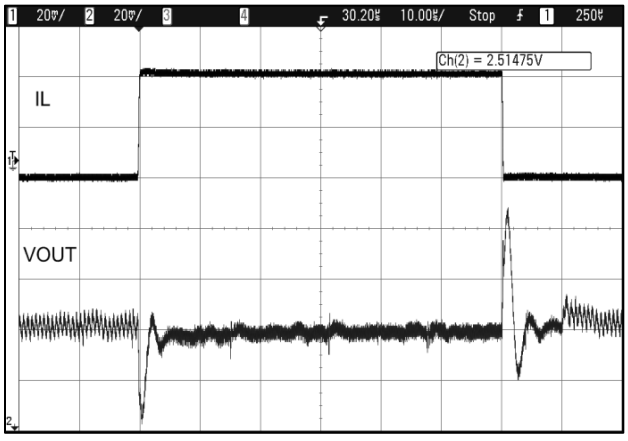


Figure 21. Load Transient, 0 mA to 400 mA, V_{OUT} = 2.5 V

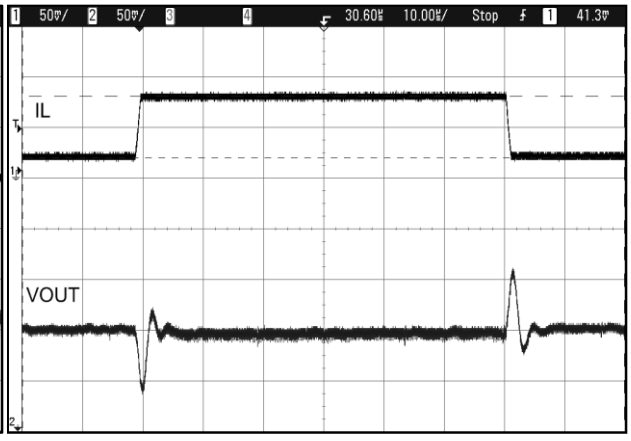


Figure 22. Load Transient, 200 mA to 800 mA, V_{OUT} = 2.5 V

Typical Characteristics

Unless otherwise noted, V_{IN} = EN = 3.7 V, L1 = 1.0 µH, C_{LOAD} = 4.7 µF, and T_A = +25°C.

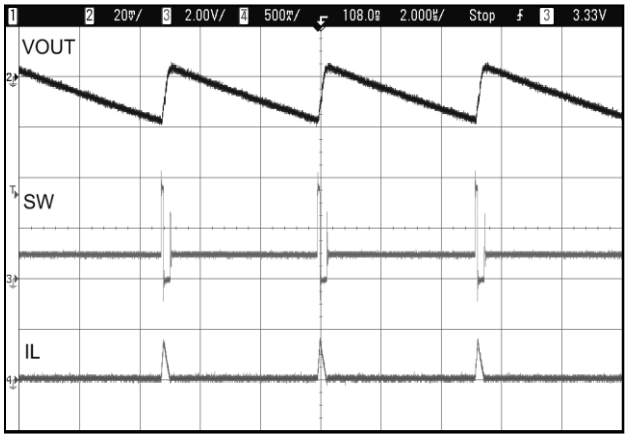


Figure 23. Switching Waveforms, PFM Mode, I_{LOAD} = 10 mA (Light Load)

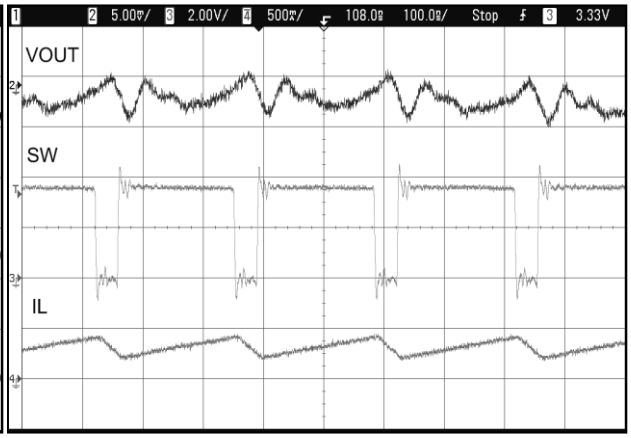


Figure 24. Switching Waveforms, PWM Mode, f_{SW} = 6 MHz, I_{LOAD} = 300 mA (Heavy Load)

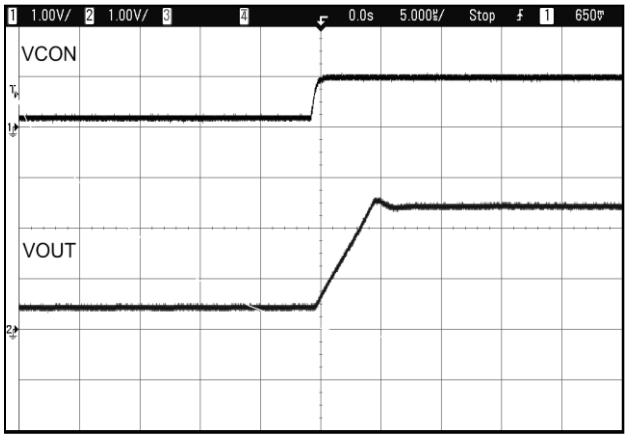


Figure 25. V_{OUT} Rising Transition 0.5 V to 2.5 V, V_{IN} = 3.7 V

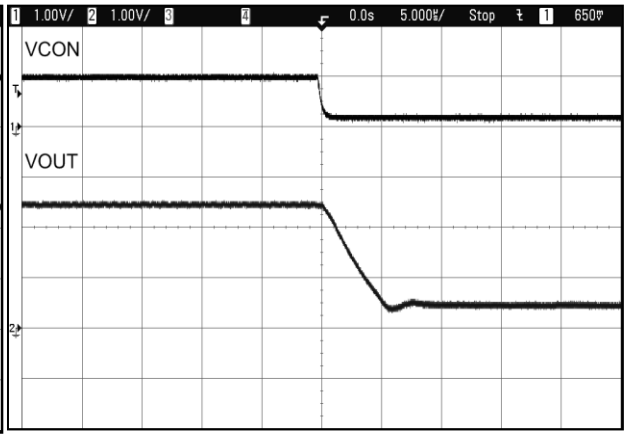


Figure 26. V_{OUT} Falling Transition 2.5 V to 0.5 V, V_{IN} = 3.7 V

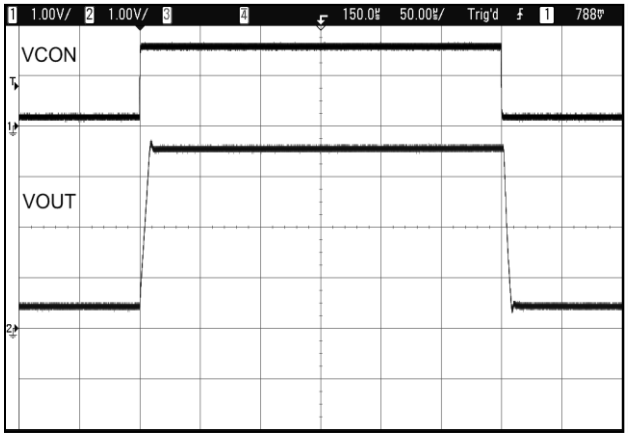


Figure 27. V_{OUT} Transient Response ΔV_{OUT} = 3 V

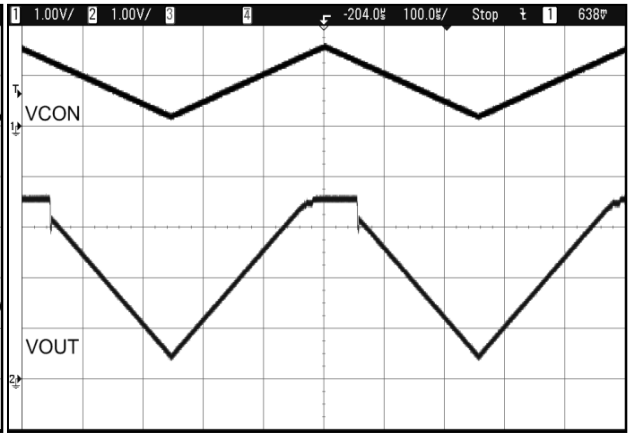


Figure 28. V_{OUT} Transient and Bypass Response ΔV_{OUT} > 3 V, V_{CON} Stepped Above 1.5 V

Typical Characteristics

Unless otherwise noted, V_{IN} = EN = 3.7 V, L1 = 1.0 µH, C_{LOAD} = 4.7 µF, and T_A = +25°C.

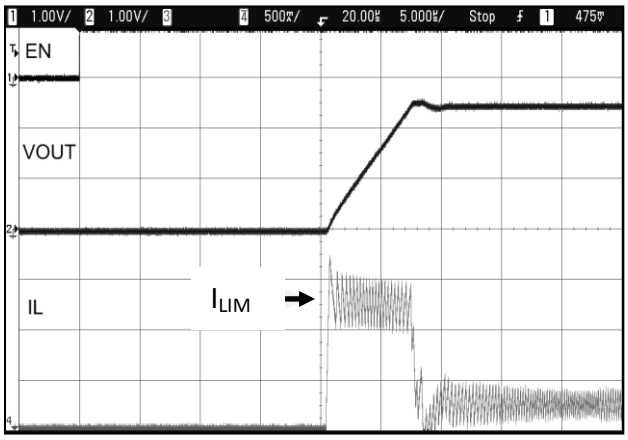


Figure 29. Soft-Start Transient Response from 0 mA to 100 mA

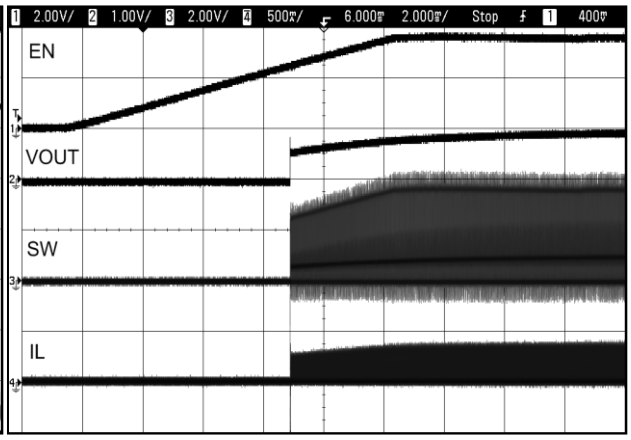


Figure 30. Cold-Start Transient Response from 0 mA to 100 mA

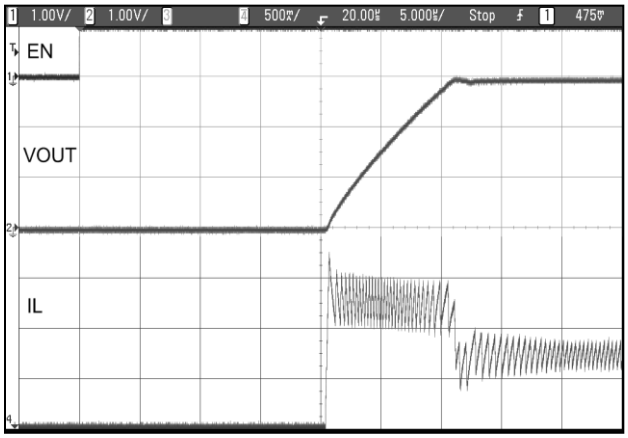


Figure 31. Soft-Start Transient Response from 0 mA to 800 mA

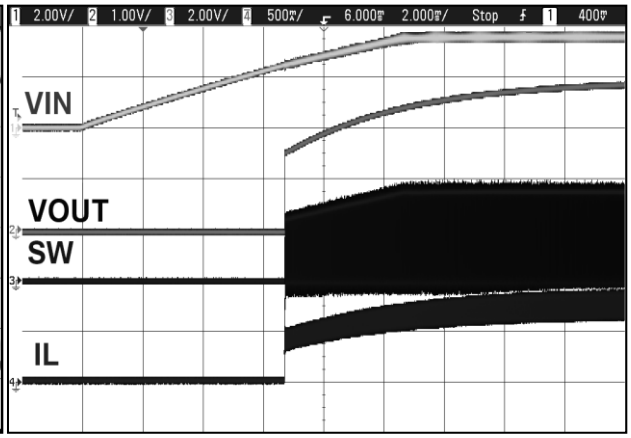


Figure 32. Cold-Start Transient Response from 0 mA to 800 mA

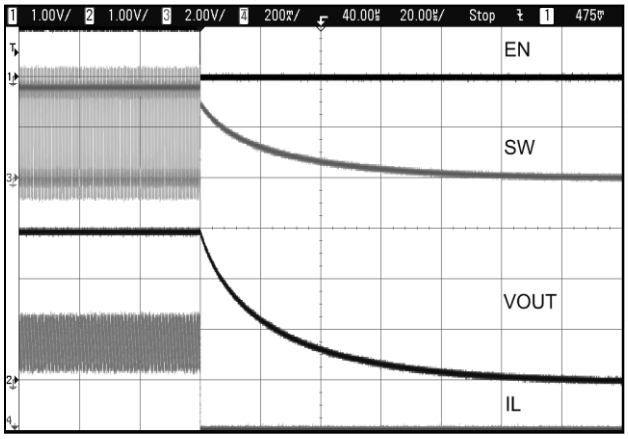


Figure 33. Shutdown Transient Response

Block Diagram

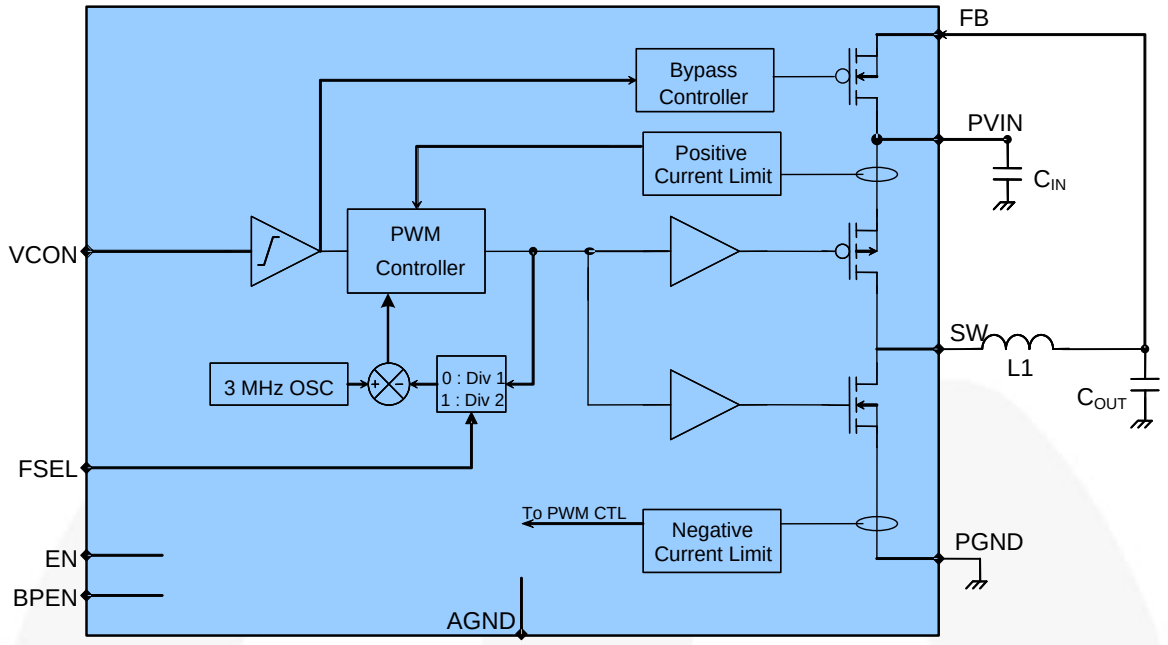


Figure 34. Block Diagram

Operating Mode Description

The FAN5903 is a high-efficiency synchronous step-down DC-DC converter operating with a Current-Mode control. It adjusts the output voltage, V_{OUT}, depending on the set voltage V_{CON} provided by an external DAC. Regulated V_{OUT} is set to 2.5 times input voltage V_{CON}.

The DC-DC operates in PWM Mode or PFM Mode, depending on the output voltage and load current. Bypass Mode is supported where the output voltage is shorted to the input voltage via a low on-state resistance bypass FET.

The FAN5903 supports a wide range of load currents. High-current applications, up to a DC output of 800 mA, mandated by 3G / 3.5G and 4G applications, for example, are supported. System performance may be optimized by enabling the DC-DC to run at either a 3 MHz or 6 MHz switching rate.

Auto Mode

In Pulse Width Modulation (PWM) Mode, regulation starts with an on-state where a P-channel transistor is turned on and the inductor current is ramped up until the off state begins. In the off state, the P-channel is switched off and an N-channel transistor is turned on. The inductor current decreases to maintain an average value equal to the DC load current. The inductor current is continuously monitored. A current sense flags when the P-channel transistor current exceeds the current limit and the switcher is turned off to decrease the inductor current and prevent magnetic saturation. Similarly, the current sense flags when the N-channel transistor current exceeds the current limit and re-directs discharging current through the inductor back to the battery.

In Pulse Frequency Modulation (PFM) Mode, at low output voltages and load currents, typically less than 100 mA; the DC-DC operates in a constant On-Time Mode. In the on-state, the P-channel is turned on during a well-defined on-time before switching to the off state, whereby the N-channel switch is turned on and the inductor current is decreased to 0 A. The switcher output is put into high-resistance state until the new regulation cycle starts.

PFM Mode realizes high efficiency while maintaining RF system performance down to low load currents.

Bypass Mode

In Bypass Mode, the FAN5903 operates at 100% duty cycle with the bypass FET turned on. This enables a very low voltage dropout with up to 2.4 A DC load current. In applications with 3G / 3.5G and 4G PAs, the Bypass Mode typically handles 800 mA.

Table 1. Mode Descriptions

#	Mode	Mode Description	Conditions			
			FSEL	BPEN	EN	VCON
1	Shutdown Mode	The whole IC is disabled.	X	X	0	0
2	Sleep Mode	The DC-DC is in Sleep Mode and consumes less than 70 µA of current.	X	X	1	0
3	6 MHz Auto Mode	The DC-DC is in Auto Mode and switches at 6 MHz.(6,7)	0	0	1	1
4	3 MHz Auto Mode	The DC-DC is in Auto Mode and switches at 3 MHz.	1	0	1	1
5	Bypass Mode	The bypass FET is forced ON. The DC-DC is set to 100% duty cycle.	X	1	1	1

Notes:

6. When V_{OUT} exceeds V_{IN} – 200 mV, the bypass FET is enabled and the DC-DC goes to 100% duty cycle. When $V_{OUT} \leqq V_{IN}$ – 375 mV, the bypass FET is disabled and the DC-DC goes to Auto Mode.
7. When the load current is smaller than PFM current threshold, the DC-DC changes to PFM Mode.

DC Output Voltage

The output voltage of the DC-DC is determined by V_{CON}, provided by an external DAC or voltage reference:

$$V_{OUT} = 2.5 \times V_{CON} \quad (1)$$

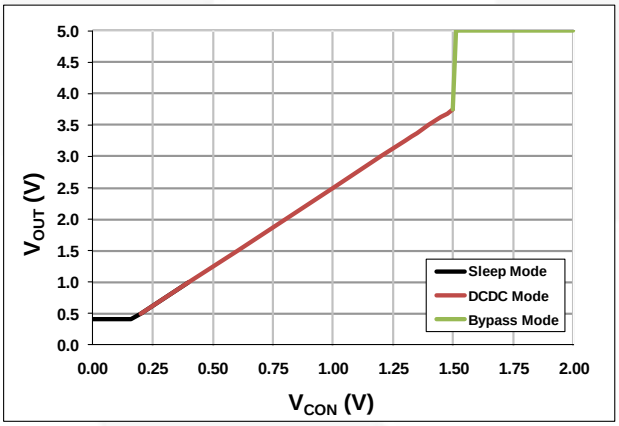


Figure 35. Output Voltage vs. Control Voltage

The DC-DC is able to provide a regulated V_{OUT} only if V_{CON} is between 0.16 V to 1.40 V. This allows V_{OUT} to be adjusted between 0.40 V and 3.50 V. If V_{CON} is below this range, V_{OUT} is clamped to 0.40 V as minimum and enters bypass for V_{CON} > 1.50 V. If V_{CON} is less than 50 mV, FAN5903 enters a non-regulated Sleep Mode. This reduces current consumption to less than 70 µA while allowing for a rapid return to regulation.

FAN5903 automatically switches between PFM, PWM, and Bypass Modes.

The DC-DC is able to provide a regulated V_{OUT} only if the battery voltage is 200 mV greater than V_{OUT}.

Bypass Mode

The trigger to enter Bypass Mode is based on the voltage difference between the battery voltage (sensed through the PVIN pin) and the internally generated reference voltage, V_{REF}, as depicted in Figure 36. The DC-DC enters Bypass Mode when $V_{IN} = V_{OUT} + 200$ mV. It then turns into 100% duty cycle and the low-R_{DSON} bypass FET is turned on. As V_{OUT} approaches V_{IN}; the DC-DC operates in a constant off-time mode, the frequency is decreased to achieve a high duty cycle, and the system continues to run in a regulated mode until the bypass condition is satisfied.

As noted above, Bypass Mode is also entered when V_{CON} exceeds 1.5 V.

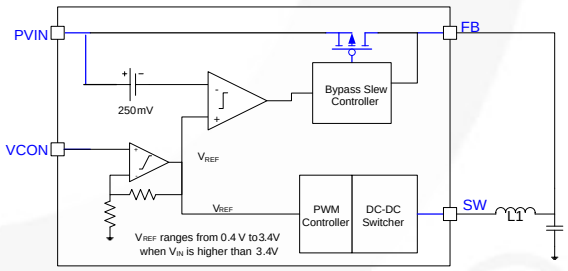


Figure 36. Enabling Bypass Transistor Circuit

The bypass FET is turned on progressively using a slew rate controller to limit the inrush current. The inrush current is expressed as a function of the specified slew rate as follows:

$$I_{INRUSH} \approx C_{OUT} \frac{\Delta V_{OUT}}{\Delta t} = C_{OUT} \bullet V_{BP\_SLEW} \quad (2)$$

The slew rate controller is not used when releasing the Bypass Mode.

Switching Frequency Selection (FSEL)

In some cases, it may be desirable to change the DC-DC's switching frequency from 6 MHz (FSEL = 0) to 3 MHz (FSEL = 1). At 3 MHz operation the DC-DC's efficiency is generally higher than that at 6 MHz. The primary tradeoff with this is increased voltage ripple at the lower frequency. A 1.0 µH inductor may be used in 3 MHz operation to optimize efficiency and ripple.

The FAN5903 is designed to have minimal impact on the RF output spectrum at either switching frequency.

Dynamic Output Voltage Transitions

The FAN5903 has a complex voltage transition controller that realizes less than 10 µs transition times with a large output capacitor and output voltage ranges.

The transition controller manages five transitions:

- ΔV_{OUT} positive step
- ΔV_{OUT} negative step
- ΔV_{OUT} transition to or from Bypass Mode
- ΔV_{OUT} transition at startup
- ΔV_{OUT} transition after BPEN

In most cases, sharp V_{CON} transitions and letting the transition controller optimize the output voltage slew rate are recommended.

ΔV_{OUT} Positive Step
After a V_{CON} positive step, the DC-DC enters a Current-Limit Mode, where V_{OUT} ramps with a constant slew rate dictated by the output capacitor and the current limit.

ΔV_{OUT} Negative Step
After a V_{CON} negative step, the DC-DC enters Current-Limit Mode, where V_{OUT} is reduced with a constant slew rate dictated by the output capacitor and the current limit.

V_{OUT} Transition to or from Bypass Mode
The transition to or from Bypass Mode requires the bypass conditions be met. The FAN5903 performs detection of the bypass conditions 2 µs after V_{CON} transition and enables the required charging / discharging circuit to realize a transition time of 10 µs.

V_{OUT} Transition at Startup
At startup, after EN rising edge is detected, the system requires 40 µs to enable all internal voltage references and amplifiers before enabling the DC-DC function.

V_{OUT} Transition After BPEN
When BPEN goes HIGH, the controller dismisses the internal bypass flags and sensors and enables Bypass Mode. However, the transition is managed with the same current limit and slew rate used during regular transitions.

Thermal Protection

If the junction temperature exceeds the maximum specified junction temperature, the FAN5903 enters Power-Down Mode (except the thermal detection circuit).

Sleep Mode

The FAN5903 offers a Sleep mode to minimize current, while also enabling a rapid return to regulation. Sleep Mode is entered when V_{CON} is held below 50 mV for at least 40 µs. In this mode, current consumption is reduced to under 70 µA. Sleep Mode is exited after approximately 12 µs when V_{CON} is set above 135 mV.

Typical Voltage Transitions

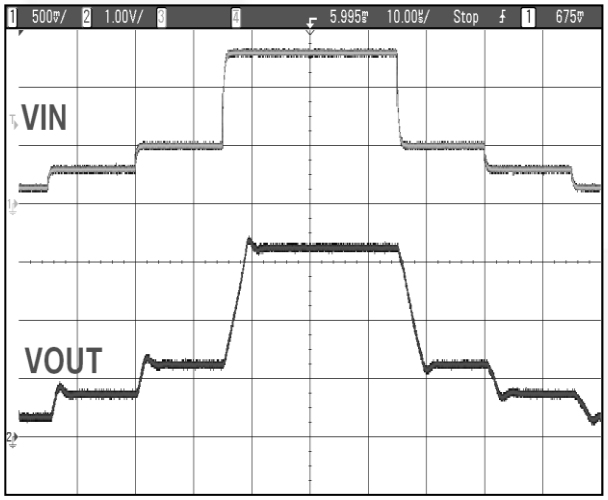


Figure 37. Rise and Fall Times for 300 mV, 500 mV, and 2 V ΔV_{OUT} (V_{IN} = 3.7 V)

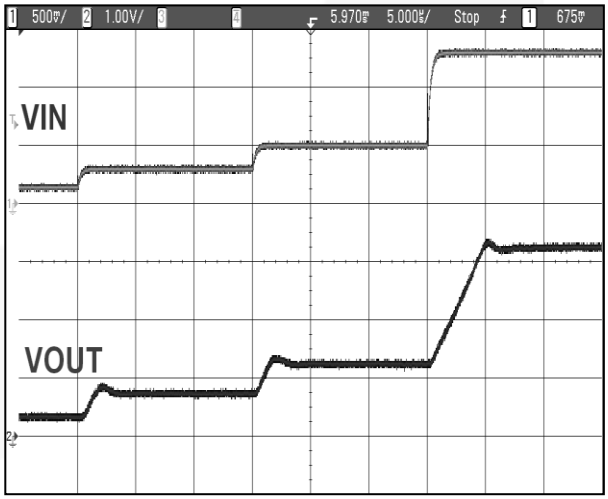


Figure 38. Rise Times for 300 mV, 500 mV, and 2 V ΔV_{OUT} (V_{IN} = 3.7 V)

Application Information

Figure 39 illustrates an application of the FAN5903 in a 3G / 4G transmitter. The FAN5903 is designed for driving multiple PAs. Figure 40 presents a timing diagram designed to meet WCDMA specifications. The FAN5903 supports voltage transients less than 10 µs.

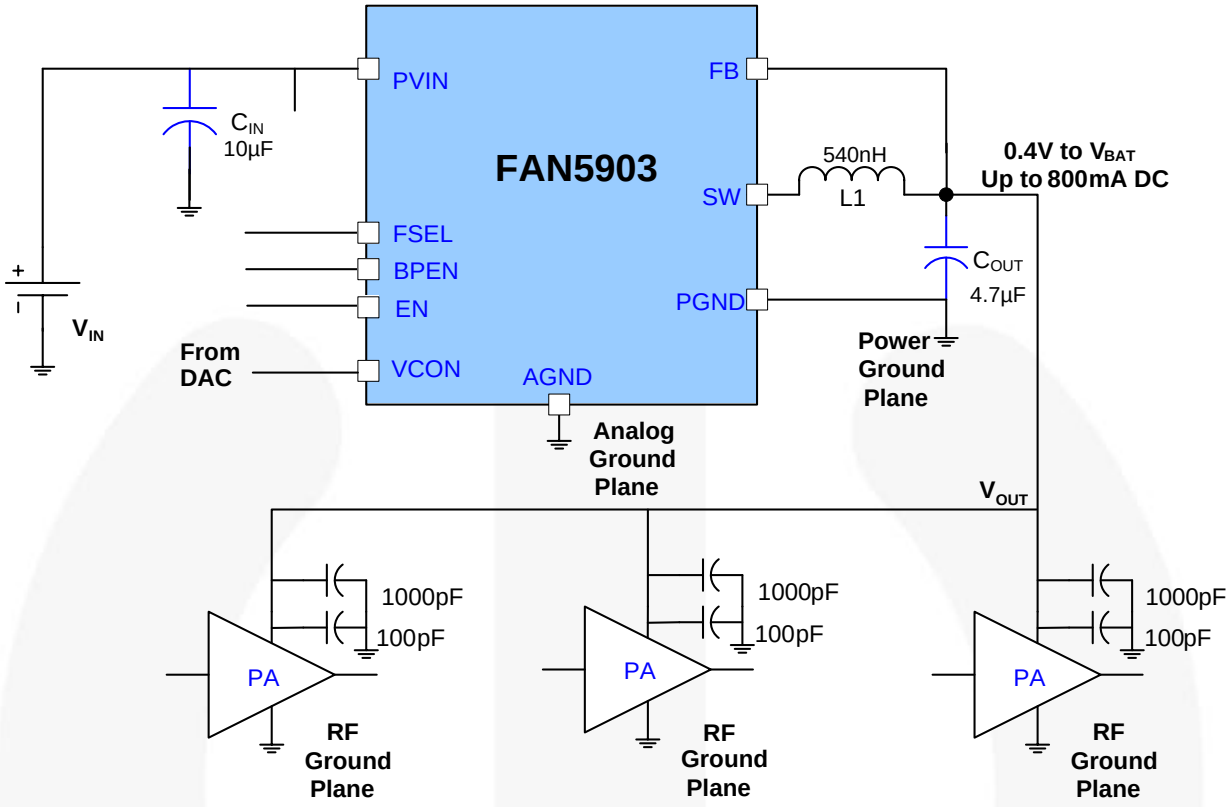


Figure 39. Typical Application Diagram of FAN5903 Supplying Power to Three 3G or 4G PAs

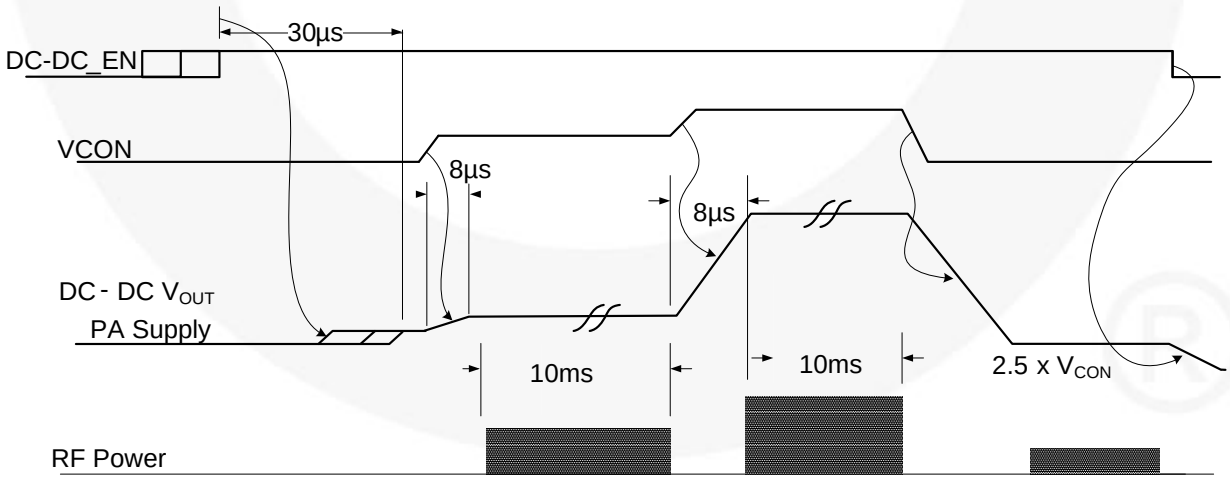


Figure 40. Timing Diagram for 3G/4G Transmitters

Application Information

Inductor Selection

The FAN5903 is able to operate at 3 MHz or 6 MHz switching frequency, so 470 nH (or 540 nH) or 1.0 µH inductors can be used, respectively. To achieve optimum efficiency, it is recommended that the FAN5903 switch at 3 MHz (FSEL = HIGH), using a 1.0 µH inductor. For applications that require the smallest possible PCB area, the FAN5903 should be configured for 6 MHz operation (FSEL = LOW) to allow use of a 470 nH or 540 nH 2012 inductor.

Table 2. Recommended Inductors

Inductor	f_{SW}	Description
L1	6 MHz	470 nH, ±20%, 1100 mA, 2012 (metric) Murata: LQM21PNR47MC0
		470 nH, ±30%, 1200 mA, 2012 (metric) Panasonic: ELGTEAR47NA
		540 nH, ±20%, 1300 mA, 2012 (metric) Murata: LQM21PNR54MG0
	3 MHz	1.0 µH, ±20%, 2500 mA, 3030 (metric) Coilcraft: XFL3010-102ME

Capacitor Selection

The minimum required output capacitor C_{OUT} is 4.7 µF, 6.3 V, X5R with an ESR of 10 mΩ or lower and an ESL of 0.3 nH or lower. Larger case sizes result in increased loop parasitic inductance and higher noise.

A 0.1 µF capacitor may be added in parallel with C_{OUT} to reduce the effect of the capacitor's parasitic inductance.

Table 3. Recommended Capacitor Values

Capacitor	Description
C_{IN}	10 µF, ±20%, X5R, 10 V
C_{OUT}	4.7 µF, ±20%, X5R, 6.3 V
C on V_{CON}	470 pF, ±20%, X5R

Filter VCON

VCON is the analog control pin of the DC-DC and should be connected to an external Digital-to-Analog Converter (DAC). It is recommended to place up to 470 pF decoupling capacitance between VCON and AGND to filter the DAC noise. This capacitor also helps protect the DAC from the DC-DC high-frequency switching noise coupled through the VCON pin.

Any noise on the V_{CON} input is transferred to V_{OUT} with a gain of two and a half (2.5). If the DAC output is noisy, a series resistor may be inserted between the DAC output and the capacitor to form an RC filter.

Follow these guidelines:

- Use a low noise source or a driver with good PSRR to generate V_{CON}.
- The V_{CON} driver must be referenced to AGND.
- V_{CON} routing must be protected against PVIN, SW, PGND signals, and other noisy signals. Use AGND shielding for better isolation.
- Be sure the DAC output can drive the 470 pF capacitor on VCON. It may be necessary to insert a low value resistor to ensure DAC stability without slowing V_{CON} fast transition times.

No Floating Inputs

The FAN5903 does not have internal pull-down resistors on its inputs. Therefore, unused inputs should not be left floating and should be pulled HIGH or LOW.

PCB Layout & Component Placement

- Make sure the FAN5903, C_{IN}, and C_{OUT} are all tied to the same power ground (PGND). This minimizes the parasitic inductance of the switching loop paths.
- Place PGND on the top layer and connect it to the AGND ground plane next to C_{OUT} using several vias.
- Ensure that the routing loop, PVIN – PGND – VOUT is the shortest possible.
- Place the inductor away from the FB connection to prevent unpredictable loop behavior.
- Use the application circuit layout in Figure 41 whenever possible. The performance of this layout has been verified.
- Review the layout guidelines for the IC package. This is especially important for the WLCSP package. Refer to "*Surface Mount Assembly of Amkor's Eutectic and Lead-Free CSPnl™ Wafer-Level Chip-Scale Package*" available from the Amkor website.
- PVIN and PGND must be routed with the widest and shortest traces possible. It is acceptable for the traces connecting the inductor to be long rather than having long PVIN or PGND traces. The SW node is a source of electrical switching noise. Do not route it near sensitive analog signals.
- Two small vias are used to connect the SW node to the inductor L1. Use solder-filled vias if available.
- The connection from C_{OUT} to FB should be wide to minimize the Bypass mode voltage drop and the series inductance. Even if the current in Bypass Mode is small, keep this trace short and at least 5mm wide.
- The ground plane should be not be broken into pieces. Ground currents must have a direct, wide path from input to output.

- Each capacitor should have at least two dedicated ground vias. Place vias within 0.1 mm of the capacitors.
- Ensure the traces are wide enough to handle the maximum current value, especially in Bypass Mode.
- Ensure the vias are able to handle the current density. Use metal-filled vias if available.

Assembly

- Use metal-filled or solder-filled vias if available.
- Poor soldering can cause low DC-DC conversion efficiency. If the efficiency is low, X-ray the solder connections to verify their integrity.

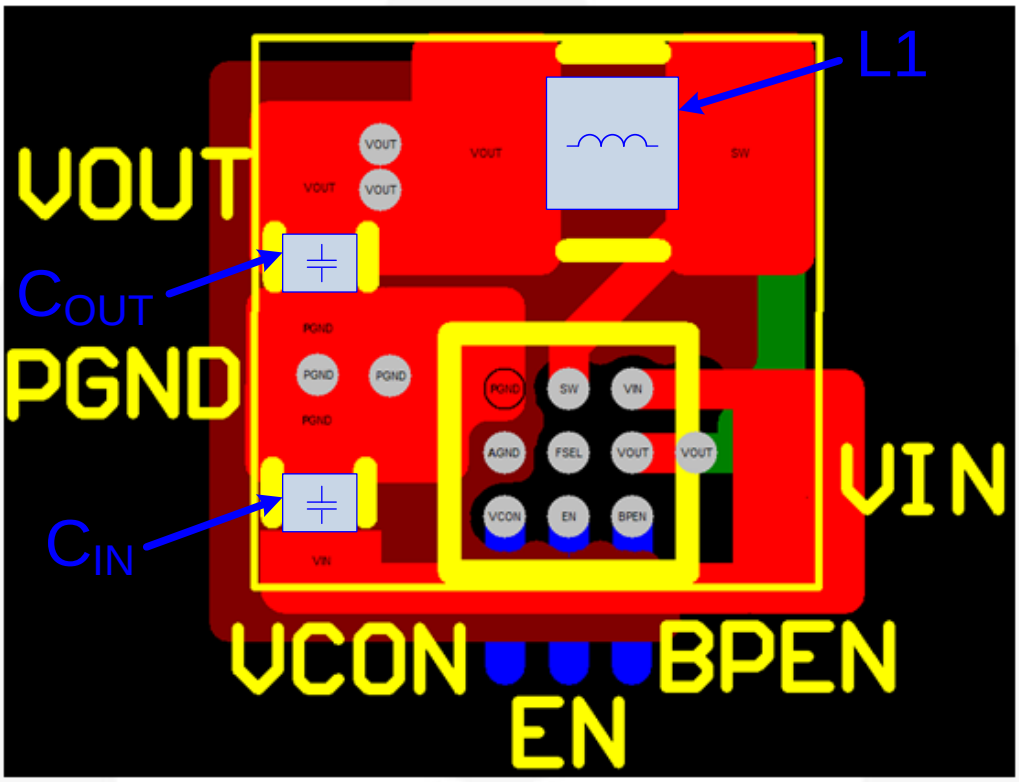
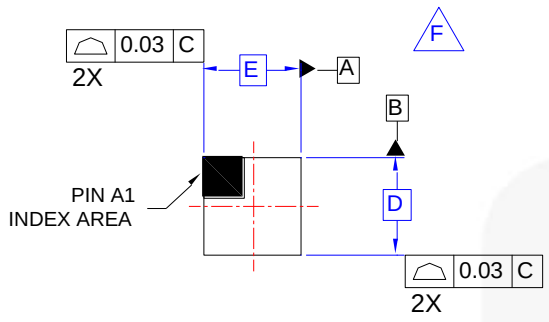
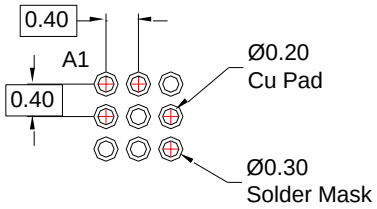


Figure 41. Recommended PCB Layout

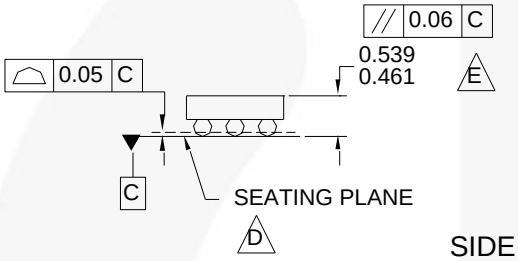
Physical Dimensions

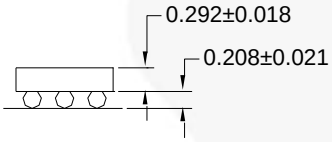


TOP VIEW

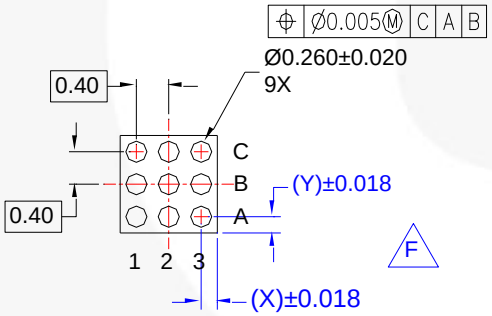


LAND PATTERN RECOMMENDATION
(NSMD PAD TYPE)





SIDE VIEWS



BOTTOM VIEW

NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 1994.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 500 MICRONS ±39 MICRONS (461-539 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILNAME: MKT-UC009AErev1

Product	D	E	X	Y	Unit
FAN5903UCX	1.292 ± 0.030	1.342 ± 0.030	0.271	0.246	mm

Figure 42. 1.34 x 1.29 mm, 9-Bump, 0.4 mm-Pitch WLCSP

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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MicroPak2™
MillerDrive™
MotionMax™
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SMART START™
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STEALTH™
SuperFET®
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
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SyncFET™
Sync-Lock™
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TinyBoost™
TinyBuck™
TinyCalc™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
TranSiC™
TriFault Detect™
TRUECURRENT®*
μSerDes™
SerDes™
UHC®
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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
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