12-V Input, 1.5-V Output, 40-A Two Phase Synchronous Buck Converter Using the TPS40130

The TPS40130EVM-001 evaluation module (EVM) is a high efficiency, two phase synchronous buck converter providing a fixed 1.5-V output at up to 40 A from a 12-V input bus. The EVM is designed to start up from a single supply, so no additional bias voltage is required for start-up. The module uses the TPS40130 high frequency two phase controller.

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1 Description

The TPS40130EVM-001 is designed to use a regulated 12-V (10-V to 14-V) bus to produce a high current, regulated 1.5-V output at up to 40 A of load current. The TPS40130EVM-001 uses a number of advanced technologies to improve its performance. Lossless DCR current sensing eliminates the need for a current sense resistor, reduces losses, and improves efficiency. A unity gain amplifier provides accurate, integrated remote sense capabilities for highly accurate, point of load regulated output voltages. Independent, programmable overvoltage protection (OVP) provides accurate overvoltage protection, even as the user adjusts the output voltage, or accidentally shorts the feedback pin to ground.

1.1 Applications

- Nonisolated High Current Point of Load and Low Voltage Bus Converters
- Video Graphic Adaptors
- Internet Servers
- Networking Equipment
- Telecommunications Equipment
- DC Power Distributed Systems

1.2 Features

- 91% Peak and 89% Full Load Efficiency at 10-V Input
- 10-V to 14-V Input Range
- 1.5-V Fixed Output, Adjustable with Single Resistor
- 40-Adc Steady State Output Current
- 330-kHz per Phase Operation (660-kHz Output Ripple)
- Single Main Switch MOSFET and Dual Synchronous Rectifier MOSFET for Each Phase
- Single Component Side, Surface Mount Design (4.5" $\times$ 4.0”)
- Current Mode Control with Forced Current Sharing
- Four Layer PCB with all Components on Top Side
- Convenient Test Points for Probing Critical Waveforms and Noninvasive Loop Response Testing
- 5-V LDO for Single Supply Operation
- Space for the TPS40120 Digitally Controlled Resistor Network for 6-Bit VID Control (Not Populated)

2 TPS40130EVM-001 Electrical Performance Specifications

Table 1. TPS40130EVM-001 Electrical and Performance Specifications

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
Input voltage range			10		14	V
Max input current	V_{IN} = 10 V, I_{OUT} = 40 A			6.9		A
No-load input current	V_{IN} = 14 V, I_{OUT} = 0 A			180		mA
OUTPUT CHARACTERISTICS						
Output voltage	R14 = 8.66 kΩ		1.45	1.50	1.55	V
Output voltage regulation	Line regulation (10 V < V_{IN} < 14 V, I_{OUT} = 20 A)				1%	
	Load regulation (0 A < I_{OUT} < 40 A, V_{IN} = 12 V)				1%	
Output voltage ripple	V_{IN} = 14 V, I_{OUT} = 40 A			30		mV_{pp}
Output load current			0		40	A
Output overcurrent	Limit source current to 8.5 A			none		—
	Limit load current to 40 A					
Output current limit	Limit source current to V_{IN} = 12 V			80		A
Switching frequency			300	330	360	kHz
Peak efficiency	V_{OUT} = 1.5 V, 20 A < I_{OUT} < 30 A	V_{12V_IN} = 10 V		91%		
		V_{12V_IN} = 12 V		90%		
		V_{12V_IN} = 14 V		89%		
Full load efficiency	V_{OUT} = 1.5 V, I_{OUT} = 40 A	V_{12V_IN} = 10 V		89%		
		V_{12V_IN} = 12 V		88%		
		V_{12V_IN} = 14 V		87%		

3 Schematics

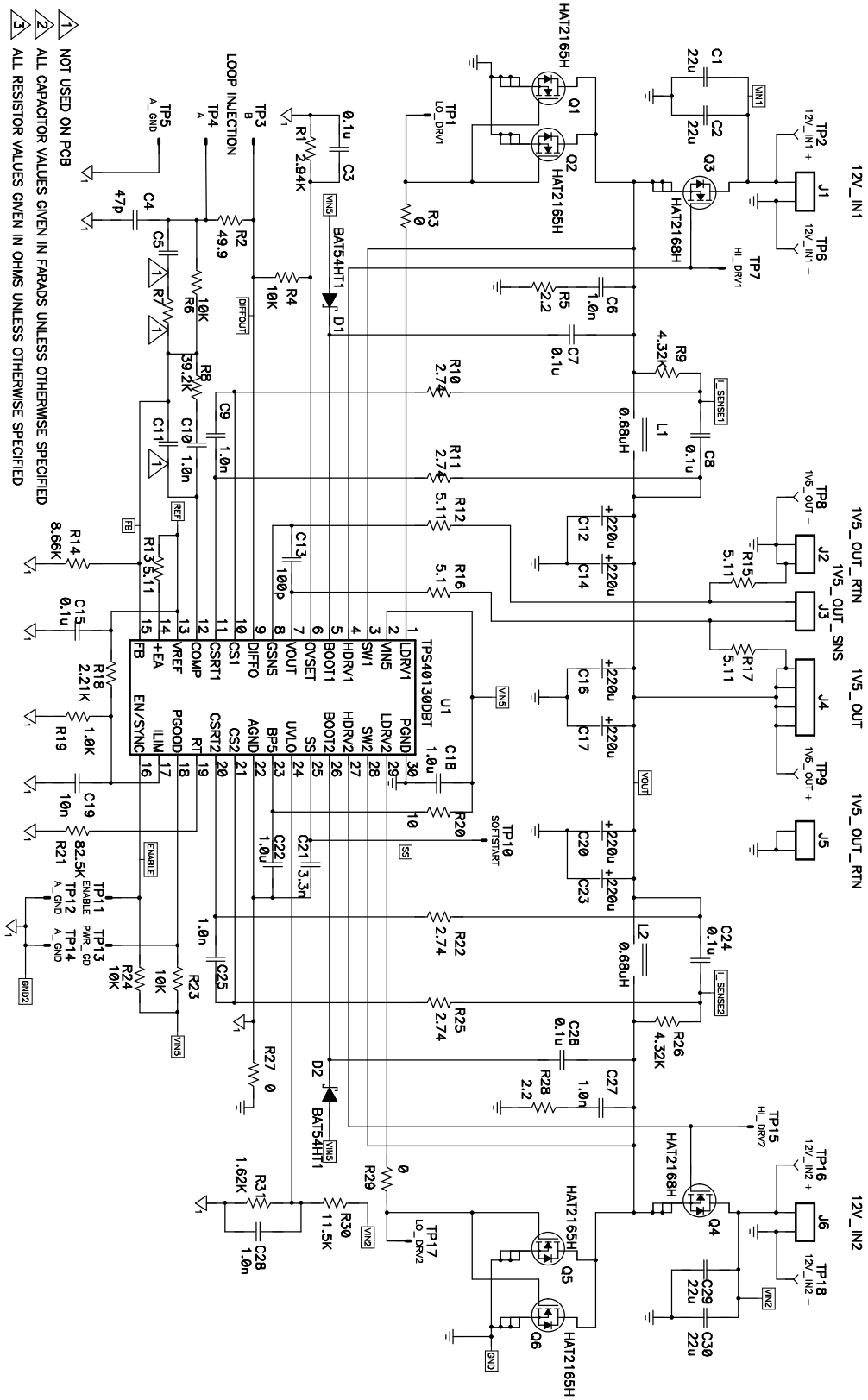

Figure 1. TPS40130EVM-001 Power Stage/Control Schematic

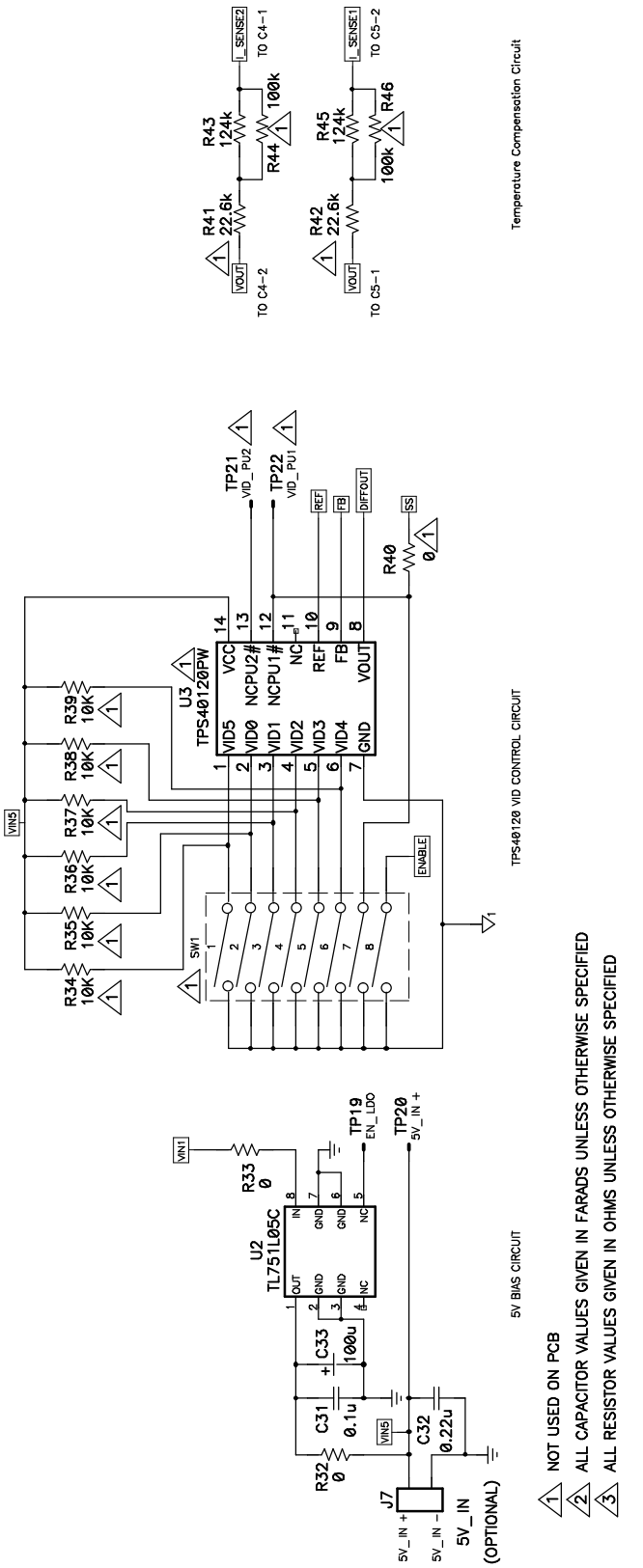

Figure 2. TPS40130EVM-001 Support Circuitry Schematic

3.1 Adjusting Output Voltage (R14)

The regulated output voltage can be adjusted within a limited range by changing the ground resistor in the feedback resistor divider (R14). The output voltage is given by Equation 1, where V_{VREF} = 0.7 V and R6 = 10.0 kΩ.

$$V_{VOUT} = V_{VREF} \times \frac{R14 + R6}{R14} \quad (1)$$

Table 2 contains common values for R14 to generate popular output voltages. The TPS40130EVM-001 is stable through these output voltages but the efficiency may suffer as the power stage is optimized for the 1.5-V output.

Table 2. Adjusting V_{1V5_OUT} With R14

V_{OUT}	R14
3.3 V	2.67 kΩ
2.5 V	3.83 kΩ
2.2 V	4.64 kΩ
2.0 V	5.36 kΩ
1.8 V	6.34 kΩ
1.5 V	8.66 kΩ
1.2 V	14.0 kΩ

3.2 Adjusting Overvoltage Protection (R1)

The output voltage is protected through an overvoltage protection circuit separate from the feedback loop, to prevent damaging the 4-V output capacitors. Initially set for 3.5 V to allow the user to adjust the output voltage from 1.2 V to 3.3 V, the OVP set point can be adjusted to be closer to the output voltage by changing R1. The output overvoltage set point is given by Equation 2, where V_{OVSET} = 0.816 V and R4 = 10.0 kΩ.

$$V_{OVP} = V_{OVSET} \times \frac{R1 + R4}{R1} \quad (2)$$

Setting R1 = R14 provides 14% to 18% margin between the voltage set value and the OVP set point. Narrower overvoltage margins can be obtained, however the tolerance on the OVP reference voltage must be closely observed.

3.3 Adjusting Overcurrent Protection (I_{lim})

The TPS40130EVM-001 is preconfigured with the overcurrent protection (OVP) set very high to allow the converter to deliver high-current, short duration loads, operate under higher loads with sufficient air flow, but still provide output short-circuit protection. To set the current limit to a lower value, change R19 according to Table 3.

Table 3. Adjusting Overcurrent Protection with R19

I_{OUT} MAX	CURRENT LIMIT	R18	R19
30 A	40 A	2.21 kΩ	464 Ω
40 A	50 A	2.21 kΩ	590 Ω
50 A	60 A	2.21 kΩ	715 Ω
60 A	70 A	2.21 kΩ	845 Ω
70 A	80 A	2.21 kΩ	1 kΩ

For more details on setting V_{Ilim} for specific overcurrent protection levels, see the overcurrent protection equations in the Functional Descriptions section of the TPS40130 data sheet.

3.4 Using an External 5-V Supply (R32 and R33)

The TPS40130EVM-001 is designed to be run from a single 12-V supply by incorporating a TL751 5-V LDO, however an external supply can be used if a separate 5-V bus is available in the target system. To use an external 5-V supply, connect it through 5V_IN (J7) and remove R32 and R33 to disconnect the LDO from the circuit. The TPS40130EVM-001 requires approximately 50 mA of current from the 5-V supply.

4 Test Setup

4.1 Equipment

4.1.1 Voltage Source

V_{12V_IN}: The input voltage source (V_{12V_IN}) should be a 0-V to 15-V variable dc source capable of 8.5 Adc. Connect V_{12V_IN} to J1 and J6 as shown in Figure 1.

4.1.2 Meters

A1: 0 Adc to 10 Adc ammeter

V1: V_{12V_IN}, 0 V to 15 V voltmeter

V2: V_{1V5_OUT} VOUT, 0 V to 5 V voltmeter

4.1.3 Loads

LOAD1: The output load (LOAD1) should be an electronic constant current mode load capable of 0 Adc to 40 Adc at 1.5 V.

4.1.4 Recommended Wire Gauge

V_{12V_IN} to J1 and J6: The connection between the source voltage, V_{12V_IN} and J1 and J6 of HPA087 can carry as much as 7 Adc. The minimum recommended wire size is AWG #16 with the total length of wire less than 4 feet (2 feet input, 2 feet return).

J4 to LOAD1: The connection between J4 of HPA087 and LOAD1 can carry as much as 40 Adc. The minimum recommended wire size is 4 x AWG #16, with the total length of wire less than 1 foot.

J2 and J5 to LOAD1: The connection between J2 and J5 of HPA087 and LOAD1 can carry as much as 40 Adc. The minimum recommended wire size is 2 x AWG #16 (two wires per connector), with the total length of wire less than 1 foot.

4.1.5 Other

FAN: The TPS40130EVM-001 includes components that can get hot to the touch. Because this EVM is not enclosed to allow probing of circuit nodes, a small fan capable of 200 to 400 lfm is required to reduce component surface temperatures to prevent user injury. The EVM should not be left unattended while powered or probed while the fan is not running.

OSCILLOSCOPE: A 60-MHz or faster oscilloscope can be used to determine the ripple voltage on 1V5_OUT. The oscilloscope should be set for 1 MΩ impedance, ac coupling, 1 µs/division horizontal resolution, 20 mV/division vertical resolution for taking output ripple measurements.

4.2 Equipment Setup

Shown in Figure 3 is the basic test setup recommended to evaluate the TPS40130EVM-001. Note that although the return for J1, J2, J5, and J6 are all the same, the connections should remain separate as shown in Figure 3.

4.2.1 Procedure

1. Working at an ESD workstation, make sure that any wrist straps, bootstraps, or mats are connected referencing the user to earth ground before power is applied to the EVM. Electrostatic smock and safety glasses should also be worn.
2. Prior to connecting the dc input source, V_{12V_IN}, it is advisable to limit the source current from V_{12V_IN} to 7.0 A maximum. Make sure V_{12V_IN} is initially set to 0 V and connected as shown in Figure 3.
3. Connect the ammeter A1 (0-A to 7-A range) between V_{12V_IN} and J1 and J2 as shown in Figure 3.
4. Connect voltmeter V1 to 12V_IN + and 12V_IN– as shown in Figure 3.
5. Connect LOAD1 to J2 as shown in Figure 1. Set LOAD1 to constant current mode to sink 0 Adc before V_{12V_IN} is applied.
6. Connect voltmeter, V2 across 1V5_OUT + and 1V5_OUT - as shown in Figure 3.
7. Place fan as shown in Figure 3 and turn on, making sure air is flowing across the EVM.

4.2.2 Diagram

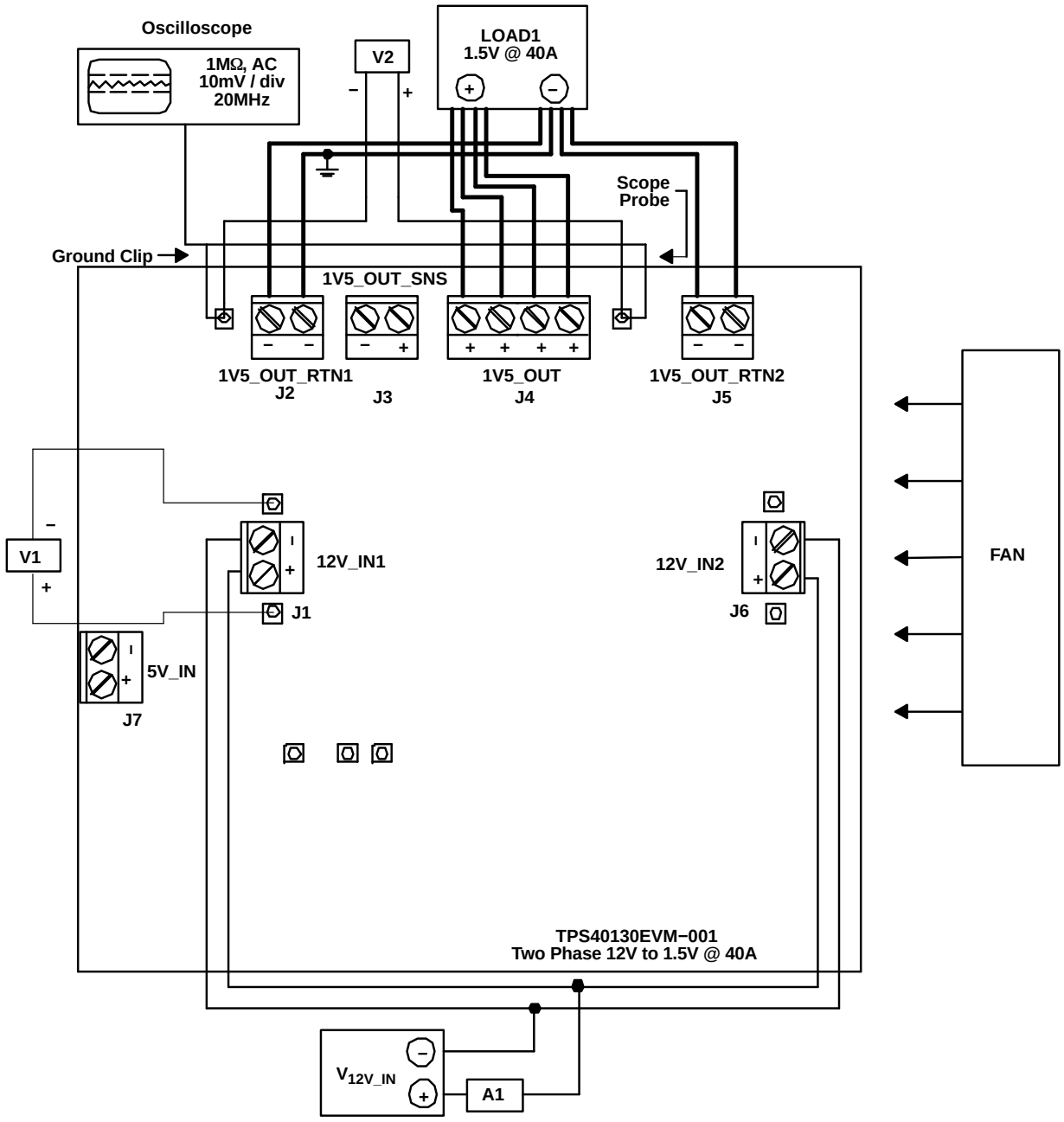

Figure 3. TPS40130EVM-001 Recommended Test Setup

4.3 Startup/Shutdown Procedure

1. Increase V_{12V_IN} (V1) from 0 Vdc to 10 Vdc
2. Vary LOAD1 from 0 Adc to 40 Adc
3. Vary V_{12V_IN} (V1) from 10 Vdc to 14 Vdc
4. Decrease LOAD1 to 0 A
5. Decrease V_{12V_IN} to 0 V

4.4 Equipment Shutdown

1. Shut down oscilloscope
2. Shut down LOAD1
3. Shut down V_{12V_IN}
4. Shut down fan

5 TPS40130EVM-001 Typical Performance Data and Characteristic Curves

Figure 4, Figure 5, Figure 6, and Figure 7 present typical performance curves for the TPS40130EVM-001. Since actual performance data can be affected by measurement techniques and environment variables, these curves are presented for reference and may differ from actual field measurements.

5.1 Efficiency

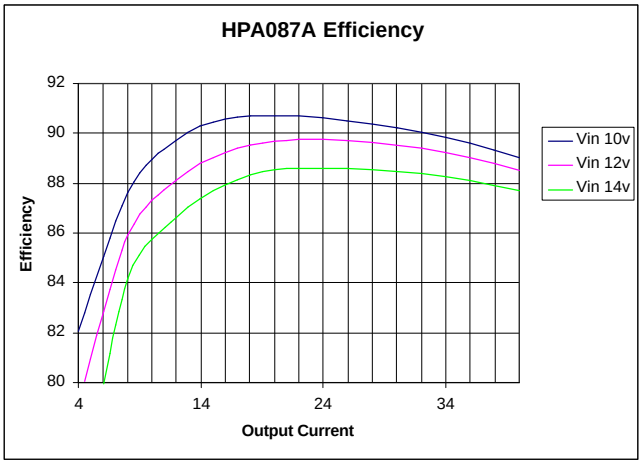

Figure 4. TPS40130EVM-001 Efficiency, V_{12V_IN} = 10 V to 14 V, V_{1V5_OUT} = 1.5 V, I_{1V5_OUT} = 4 A to 40 A

5.2 Line Regulation

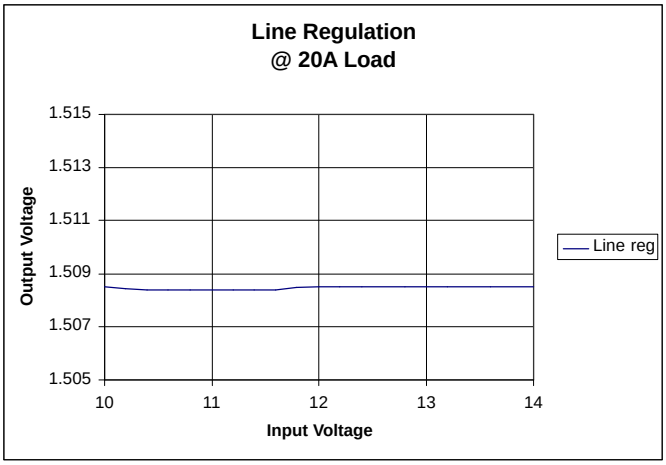

Figure 5. TPS40130EVM-001 Line Regulation, I_{1V5_OUT} = 20 A

5.3 Load Regulation

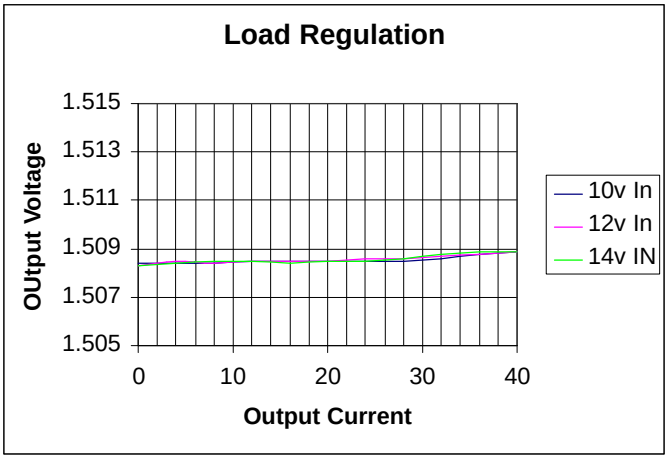

Figure 6. TPS40130EVM-001 Load Regulation

5.4 Transient Response

5.4.1 Positive Transient

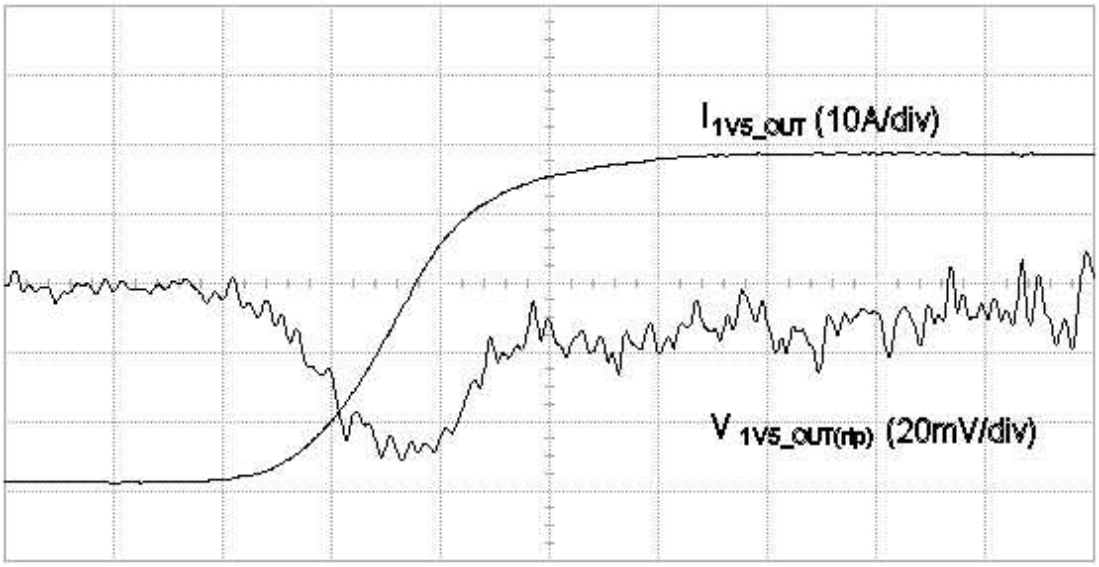

Figure 7. TPS40130EVM-001 5 A to 55 A Transient Response, 5 A to 55 A at 3 A/µs, $I_{1V5\_OUT\ (10A/div)}$, $V_{1V5\_OUT(rip)}$ (20 mv/div), Time 10 µs/div

5.4.2 Negative Transient

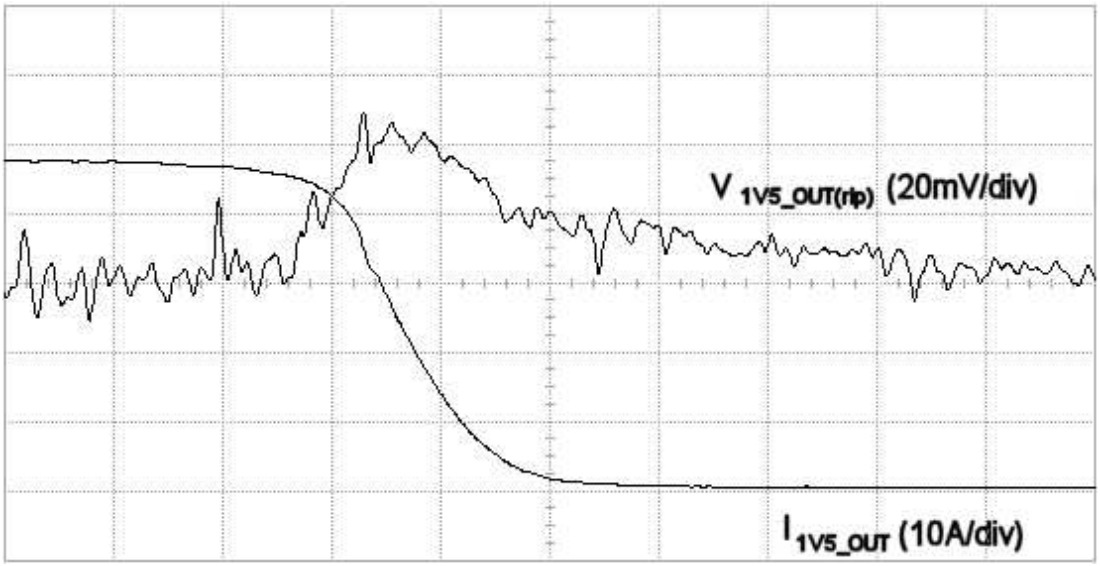

Figure 8. TPS40130EVM-001 55 A to 5 A Transient Response, 55 A to 5 A at 3 A/µs, $I_{1V5\_OUT\ (10A/div)}$, $V_{1V5\_OUT(rip)}$ (20 mV/div), Time 10 µs/div

6 EVM Assembly Drawings and Layout

Figure 9 through Figure 14 show the design of the TPS40130EVM-001 printed circuit board. The EVM has been designed using a 4-layer, 2-oz copper-clad circuit board 4.5" × 4.0" with all components on the top side to allow the user to easily view, probe, and evaluate the TPS40130 control IC in a practical application. Moving components to both sides of the PCB or using additional internal layers can offer additional size reduction for space constrained systems.

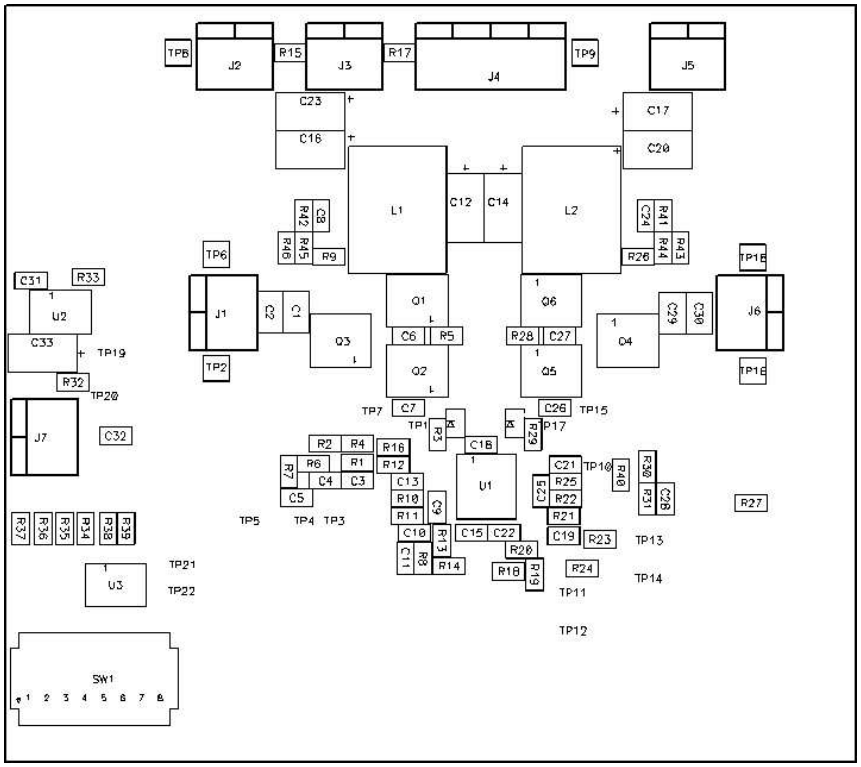

Figure 9. TPS40130EVM-001 Component Placement (Top View)

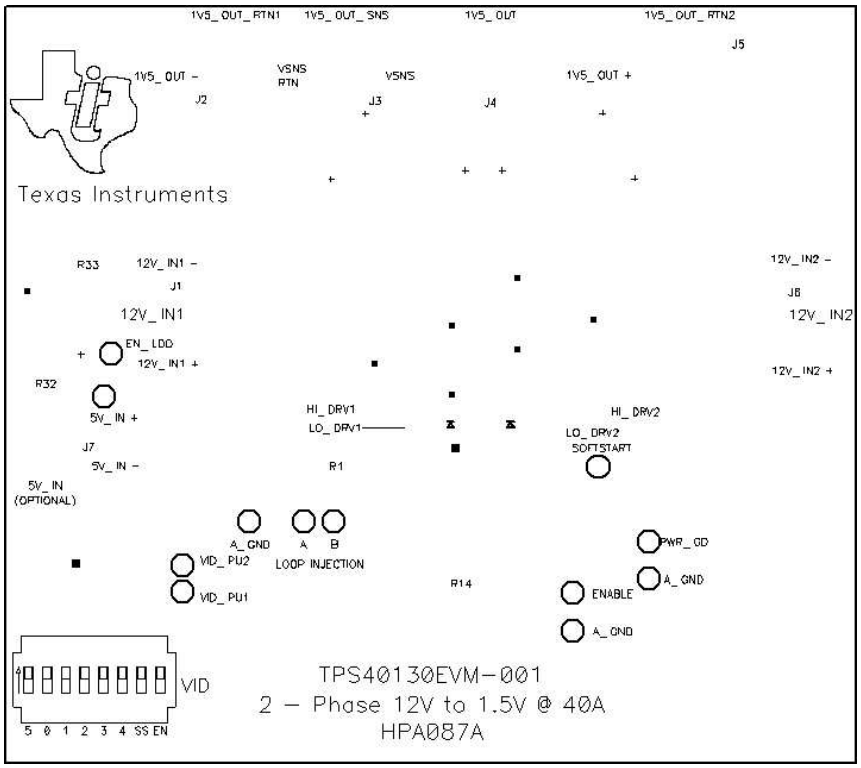

Figure 10. TPS40130EVM-001 Silkscreen (Top View)

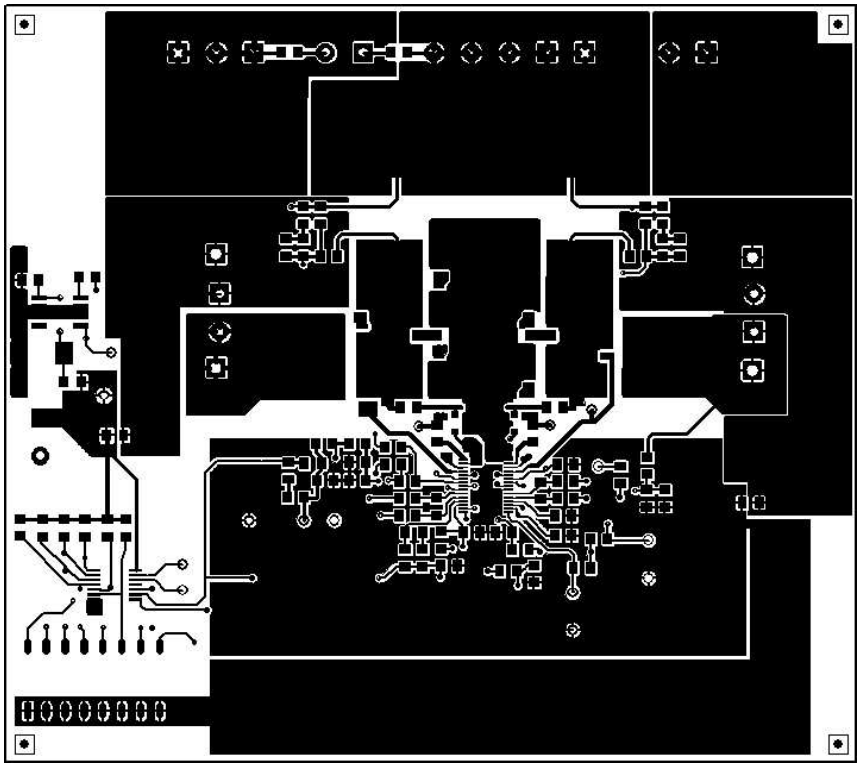

Figure 11. TPS40130EVM-001 Top Copper (Top View)

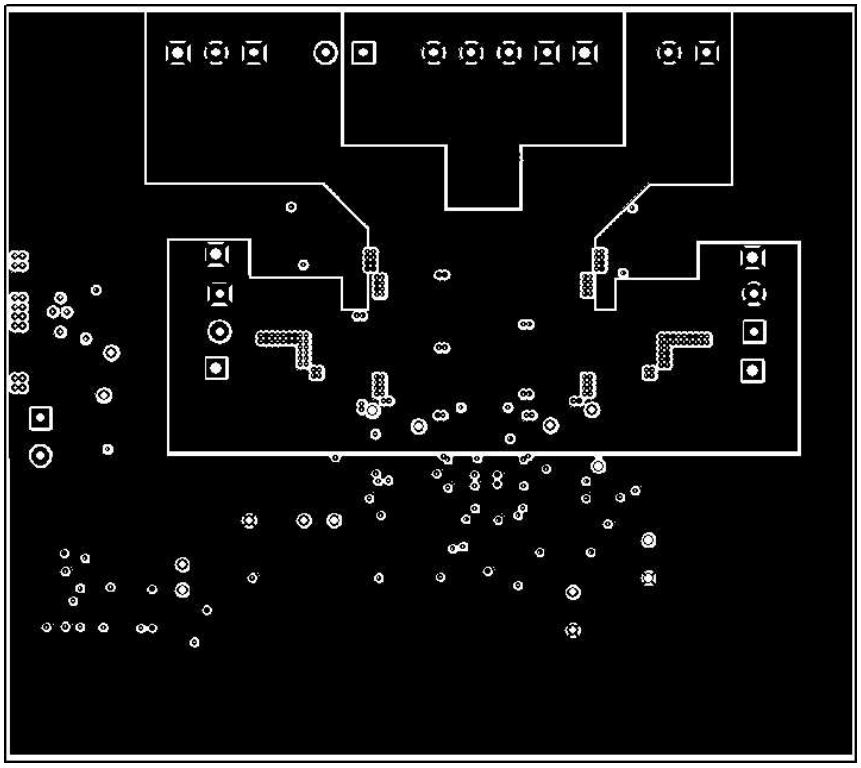

Figure 12. TPS40130EVM-001 Layer 2 (X-Ray Top View)

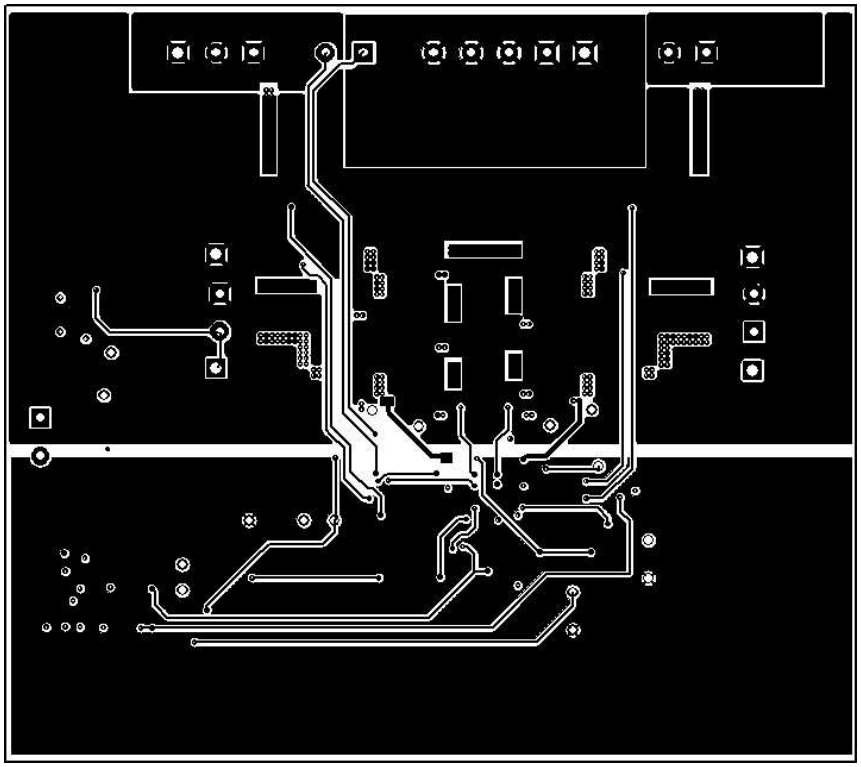

Figure 13. TPS40130EVM-001 Layer 3 (X-Ray Top View)

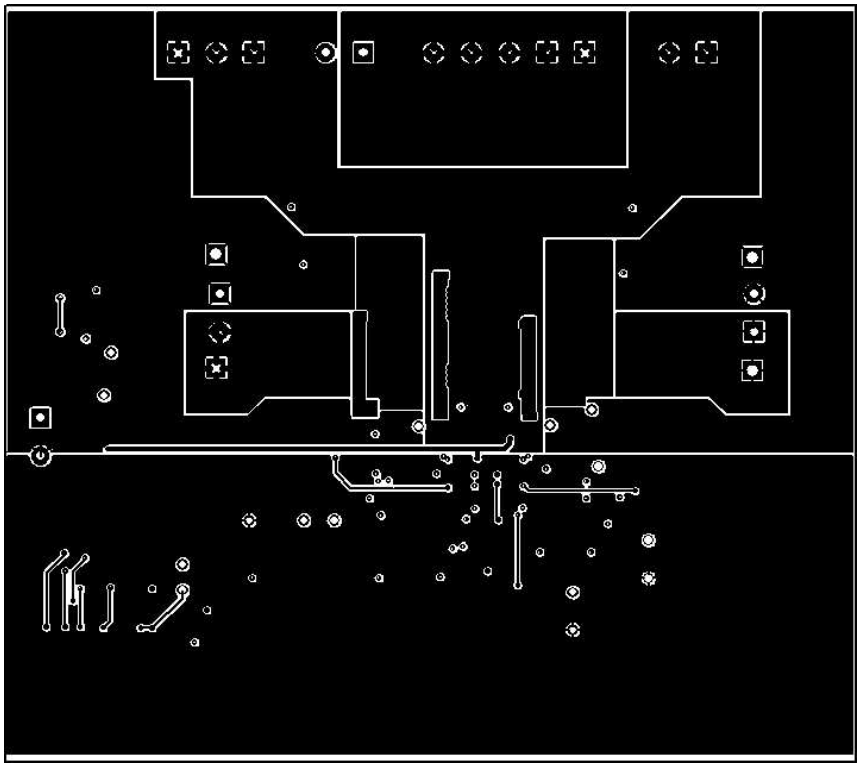

Figure 14. TPS40130EVM-001 Bottom Copper (X-Ray Bottom View)

7 List of Materials

Table 4 lists the EVM components as configured according to the schematic shown in Figure 1 and Figure 2.

Table 4. TPS40130EVM-001 Bill of Materials(1)(2)(3)(4)

Count	RefDes	Description	Size	MFR	Part Number
4	C1, C2, C29, C30	Capacitor, ceramic, 22-µF, 16-V, X7R, 15%	1210	TDK	C3225X7R1C226M
7	C3, C7, C8, C15, C24, C26, C31	Capacitor, ceramic, 0.1-µF, 25-V, X7R, 10%	805	Std	Std
1	C4	Capacitor, ceramic, 47-pF, 50-V, NPO, 10%	805	Std	Std
0	C5, C11	Capacitor, ceramic, pF, 50-V, X7R, 10%	805	Std	Std
7	C6, C9, C10, C19, C25, C27, C28	Capacitor, ceramic, 1000-pF, 50-V, X7R, 10%	805	Std	Std
6	C12, C14, C16, C17, C20, C23	Capacitor, aluminum, 220-µF, 5-mΩ, 4-V, 20% (UE Series)	7343	Panasonic	EEF-UEOG221R
1	C13	Capacitor, ceramic, 100-pF, 50-V, NPO, 10%	805	Std	Std
2	C18, C22	Capacitor, ceramic, 1-µF, 16-V, X5R, 10%	805	Std	Std
1	C21	Capacitor, ceramic, 3300-pF, 50-V, X7R, 10%	805	Std	Std
1	C32	Capacitor, ceramic, 0.22-µF, 16-V, X7R, 10%	805	Panasonic	ECJ-2VB1C224K
1	C33	Capacitor, POSCAP, 100-µF, 10-V, 40-mΩ, 20%	7343(D)	Sanyo	10TPB100ML
2	D1, D2	Diode, Schottky, 200-mA, 30-V	SOD323	On Semi	BAT54HT1
6	J1, J2, J3, J5, J6, J7	Terminal block, 2-pin, 15-A, 5,1-mm	0.40 x 0.35	OST	ED1609
1	J4	Terminal block, 4-pin, 15-A, 5,1-mm	0.80 x 0.35	OST	ED2227
2	L1, L2	Inductor, SMT, 0.68-µH, 30-A, 0.9-mΩ	0.524 x 0.492	Wurth	S0410124A
4	Q1, Q2, Q5, Q6	MOSFET, N-channel, 30-V, 55-A, 2.5-mΩ	LFPAK	Renesas	HAT2165H
2	Q3, Q4	MOSFET, N-channel, 30-V, 20-A, 6-mΩ	LFPAK	Renesas	HAT2168H
1	R1	Resistor, chip, 2.94-kΩ, 1/10-W, 1%	805	Std	Std
4	R10, R11, R22, R25	Resistor, chip, 2.74-Ω, 1/10-W, 1%	805	Std	Std
5	R12, R13, R15, R16, R17	Resistor, chip, 5.11-Ω, 1/10-W, 1%	805	Std	Std
1	R14	Resistor, chip, 8.66-kΩ, 1/10-W, 1%	805	Std	Std
1	R18	Resistor, chip, 2.21-kΩ, 1/10-W, 1%	805	Std	Std
1	R19	Resistor, chip, 1.0-kΩ, 1/10-W, 1%	805	Std	Std
1	R2	Resistor, chip, 49.9-Ω, 1/10-W, 1%	805	Std	Std
1	R20	Resistor, chip, 10-Ω, 1/10-W, 1%	805	Std	Std
1	R21	Resistor, chip, 82.5-kΩ, 1/10-W, 1%	805	Std	Std
5	R3, R27, R29, R32, R33	Resistor, chip, 0-Ω jumper, 1/10-W, 5%	805	Std	Std
1	R30	Resistor, chip, 11.5-kΩ, 1/10-W, 1%	805	Std	Std
1	R31	Resistor, chip, 1.62-kΩ, 1/10-W, 1%	805	Std	Std
4	R4, R6, R23, R24	Resistor, chip, 10-kΩ, 1/10-W, 1%	805	Std	Std

(1) These assemblies are ESD sensitive, ESD precautions shall be observed.
(2) These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
(3) These assemblies must comply with workmanship standards IPC-A-610 Class 2.
(4) Ref designators marked with an asterik " * " cannot be substituted. All other components can be substituted with equivalent manufacturers components.

Table 4. TPS40130EVM-001 Bill of Materials (continued)

Count	RefDes	Description	Size	MFR	Part Number
0	R34, R35, R36, R37, R38, R39	Resistor, chip, 10-kΩ, 1/10-W, 1%	805	Std	Std
0	R40	Resistor, chip, 0-Ω Jumper, 1/10-W, 5%	805	Std	Std
0	R41, R42	Resistor, chip, 22.6-kΩ, 1/10-W, 1%	805	Std	Std
2	R43, R45	Resistor, chip, 124-kΩ, 1/10-W, 1%	805	Std	Std
0	R44, R46	Thermister, chip, NTC, 100-kΩ, -4250 ppm/°C 3%	805	Murata	NCP21WF104J03RA
2	R5, R28	Resistor, chip, 2.2-Ω, 1/10-W, 1%	805	Std	Std
0	R7	Resistor, chip, Ω, 1/10-W, 1%	805	Std	Std
1	R8	Resistor, chip, 39.2-kΩ, 1/10-W, 1%	805	Std	Std
2	R9, R26	Resistor, chip, 4.32-kΩ, 1/10-W, 1%	805	Std	Std
0	SW1	Switch, 8-pos, SPST, low profile, SMT			SD08H0SK
11	TP1, TP3, TP4, TP7, TP10, TP11, TP13, TP15, TP17, TP19, TP20	Test point, white, 0.40 hole, 0.050 loop	0.100	Keystone	5002
0	TP21, TP22	Test point, white, 0.40 hole, 0.050 loop	0.100	Keystone	5002
3	TP2, TP9, TP16	Test point, red, thru hole	0.125	Keystone	5010
3	TP5, TP12, TP14	Test point, black, 0.40 hole, 0.050 loop	0.100	Keystone	5001
3	TP6, TP8, TP18	Test point, black, thru hole	0.125	Keystone	5011
1	U1	IC, High-speed 2-phase synchronous BUCK controller	TSSOP-30	TI	TPS40130DBT
1	U2	IC, Low drop-out regulator, 5-V to 12-V options	SOIC8	TI	TL751L05C
0	U3	IC, 6-Bit VID controller	SO14	TI	TPS40120PW
1	—	PCB, 4-Layer FR4, 4.0" x 4.5" x 0.062"	2.4" x 2.1"	Any	HPA087A
4	—	Bumpon(5), transparent	0.44" x 0.2"	3M	SJ5303

(5) Install Bumpons on back side (unpopulated side) of PCB. Install one in each corner after cleaning.

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Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

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