74HCU04

Hex unbuffered inverter

Rev. 8 — 16 July 2020 **Product data sheet**

1. General description

The 74HCU04 is a hex unbuffered inverter. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- Balanced propagation delays
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HCU04D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HCU04DB	-40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74HCU04PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HCU04BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

nexperia

4. Functional diagram

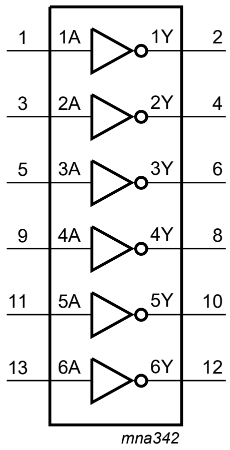


Fig. 1. Logic symbol

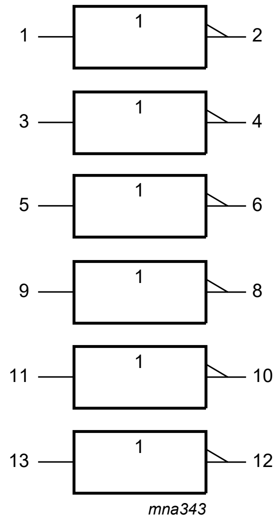


Fig. 2. IEC logic symbol

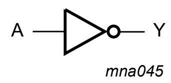


Fig. 3. Logic diagram (one inverter)

5. Pinning information

5.1. Pinning

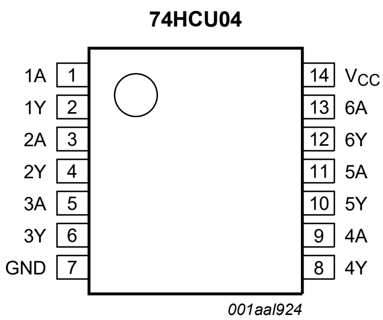
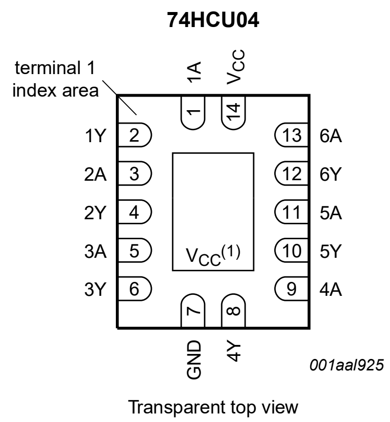


Fig. 4. Pin configuration SOT108-1 (SO14), SOT337-1 (SSOP14) and SOT402-1 (TSSOP14)



(1) This is not a supply pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to V_{CC}.

Fig. 5. Pin configuration SOT762-1 (DHVQFN14)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V_{CC}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level

Input	Output
nA	**nY**
L	H
H	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V [1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V [1]	-	±50	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V	-	±25	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.
For SOT337-1 (SSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.
For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.
For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	°C

9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.7	1.4	-	1.7	-	1.7	-	V
		V_{CC} = 4.5 V	3.6	2.6	-	3.6	-	3.6	-	V
		V_{CC} = 5.5 V	4.8	3.4	-	4.8	-	4.8	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.6	0.3	-	0.3	-	0.3	V
		V_{CC} = 4.5 V	-	1.9	0.9	-	0.9	-	0.9	V
		V_{CC} = 5.5 V	-	2.6	1.2	-	1.2	-	1.2	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = -20 μA; V_{CC} = 2.0 V	1.8	2.0	-	1.8	-	1.8	-	V
		I_O = -20 μA; V_{CC} = 4.5 V	4.0	4.5	-	4.0	-	4.0	-	V
		I_O = -4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = -20 μA; V_{CC} = 6.0 V	5.5	6.0	-	5.5	-	5.5	-	V
		I_O = -5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.2	-	0.2	-	0.2	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.5	-	0.5	-	0.5	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.5	-	0.5	-	0.5	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	2	-	20	-	20	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); For test circuit see Fig. 7.

Symbol	Parameter	Conditions		25 °C		-40 °C to +85 °C	-40 °C to +125 °C	Unit
				Typ	Max	Max	Max	
t_{pd}	propagation delay	nA to nY; see Fig. 6	[1]					
		V_{CC} = 2.0 V; C_L = 50 pF		19	70	90	105	ns
		V_{CC} = 4.5 V; C_L = 50 pF		7	14	18	21	ns
		V_{CC} = 5.0 V; C_L = 15 pF		5	-	-	-	ns
		V_{CC} = 6.0 V; C_L = 50 pF		6	12	15	18	ns
t_t	transition time	see Fig. 6	[2]					
		V_{CC} = 2.0 V; C_L = 50 pF		19	75	95	110	ns
		V_{CC} = 4.5 V; C_L = 50 pF		7	15	19	22	ns
		V_{CC} = 6.0 V; C_L = 50 pF		6	13	16	19	ns
C_{PD}	power dissipation capacitance	per inverter; V_I = GND to V_{CC}	[3]	10	-	-	-	pF

[1] t_{pd} is the same as t_{PHL}, t_{PLH}.

[2] t_t is the same as t_{THL}, t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

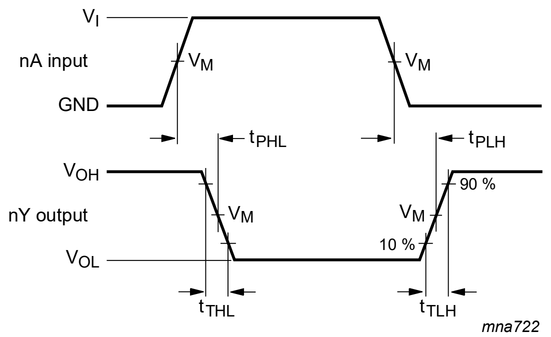
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

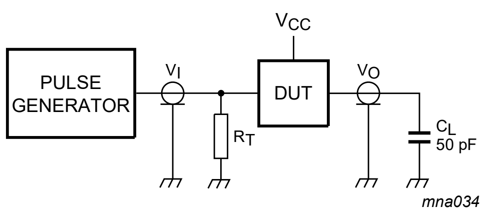
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveform and test circuit



$V_M = 0.5 \times V_{CC}$; V_I = GND to V_{CC}.

Fig. 6. The input (nA) to output (nY) propagation delay times



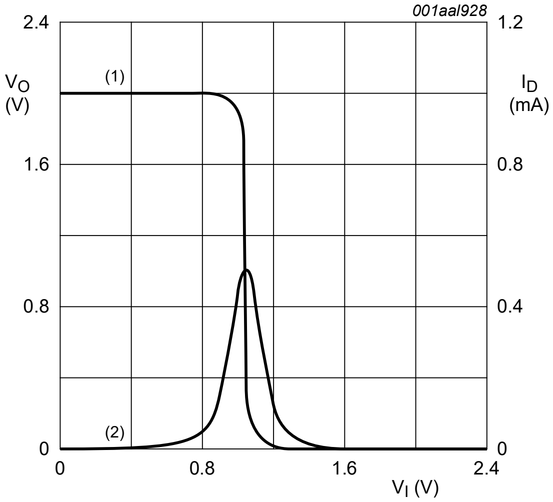
Definitions for test circuit:

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

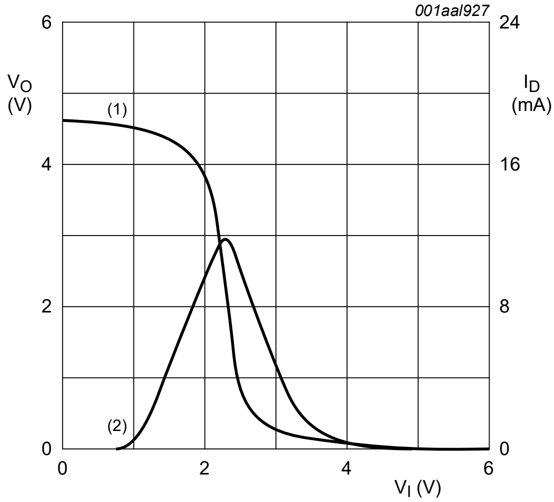
Fig. 7. Test circuit for measuring switching times

11. Typical transfer characteristics



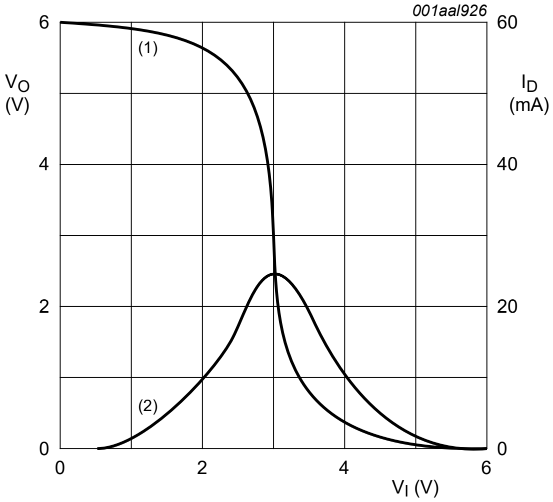
T_{amb} = 25 °C.

Fig. 8. V_{CC} = 2.0 V; I_O = 0 A



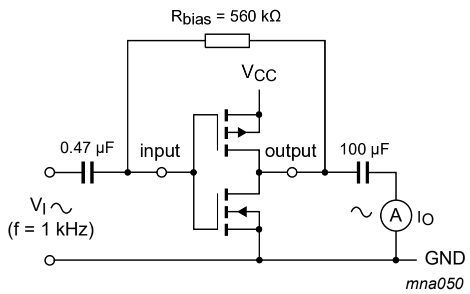
T_{amb} = 25 °C.

Fig. 9. V_{CC} = 4.5 V; I_O = 0 A



T_{amb} = 25 °C.

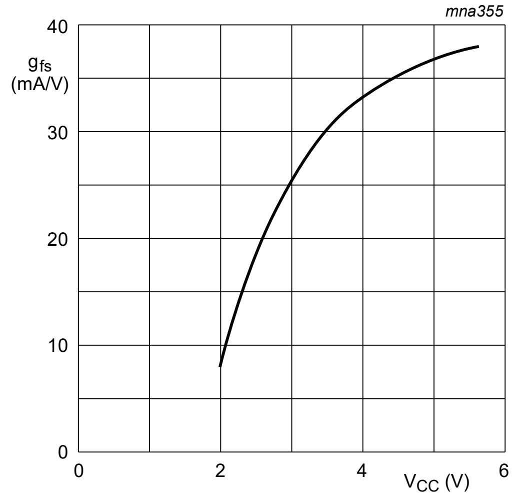
Fig. 10. V_{CC} = 6.0 V; I_O = 0 A



$$g_{fs} = \frac{\Delta I_O}{\Delta V_I}$$

f_i = 1 kHz at V_O is constant

Fig. 11. Test set-up for measuring forward transconductance



T_{amb} = 25 °C.

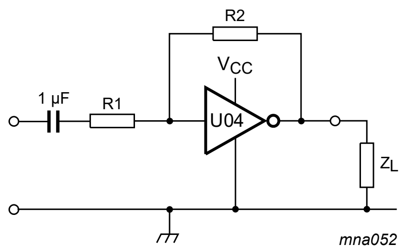
Fig. 12. Typical forward transconductance as a function of the supply voltage

12. Application information

Some applications are:

- Linear amplifier (see Fig. 13)
- Crystal oscillator design (see Fig. 14)
- Astable multivibrator (see Fig. 15)

Remark: All values given are typical unless otherwise specified.

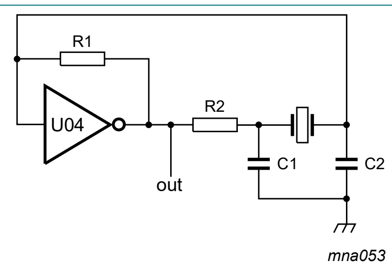


Maximum $V_{o(p-p)}$ = V_{CC} - 2.0 V centered at $0.5V_{CC}$.

$$G_v = -\frac{G_{ol}}{1 + \frac{R1}{R2}(1 + G_{ol})}$$

G_{ol} = open loop gain
G_v = voltage gain
R1 ≥ 3 kΩ, R2 ≤ 1 MΩ
Z_L > 10 kΩ; G_{ol} = 20 (typical)
V_{CC} = 6.0 V
Typical unity gain bandwidth product is 5 MHz.

Fig. 13. Linear amplifier



C1 = 47 pF (typical)
C2 = 33 pF (typical)
R1 = 1 MΩ to 10 MΩ (typical
R2 optimum value depends on the frequency and required stability against changes in V_{CC} or average minimum I_{CC}.
I_{CC} is typically 5 mA at V_{CC} = 5 V and f_i = 10 MHz.

Fig. 14. Crystal oscillator

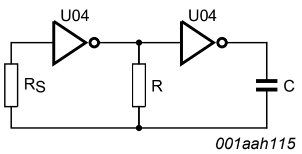
Table 8. External components for resonator (f < 1 MHz)

All values given are typical and must be used as an initial set-up.

Frequency	R1	R2	C1	C2
10 kHz to 15.9 kHz	22 MΩ	220 kΩ	56 pF	20 pF
16 kHz to 24.9 kHz	22 MΩ	220 kΩ	56 pF	10 pF
25 kHz to 54.9 kHz	22 MΩ	100 kΩ	56 pF	10 pF
55 kHz to 129.9 kHz	22 MΩ	100 kΩ	47 pF	5 pF
130 kHz to 199.9 kHz	22 MΩ	47 kΩ	47 pF	5 pF
200 kHz to 349.9 kHz	10 MΩ	47 kΩ	47 pF	5 pF
350 kHz to 600 kHz	10 MΩ	47 kΩ	47 pF	5 pF

Table 9. Optimum value for R2

Frequency	R2	Optimum for
3 kHz	2.0 kΩ	minimum required I_{CC}
	8.0 kΩ	minimum influence due to change in V_{CC}
6 kHz	1.0 kΩ	minimum required I_{CC}
	4.7 kΩ	minimum influence by V_{CC}
10 kHz	0.5 kΩ	minimum required I_{CC}
	2.0 kΩ	minimum influence by V_{CC}
14 kHz	0.5 kΩ	minimum required I_{CC}
	1.0 kΩ	minimum influence by V_{CC}
>14 kHz	-	replace R2 by C3 with a typical value of 35 pF

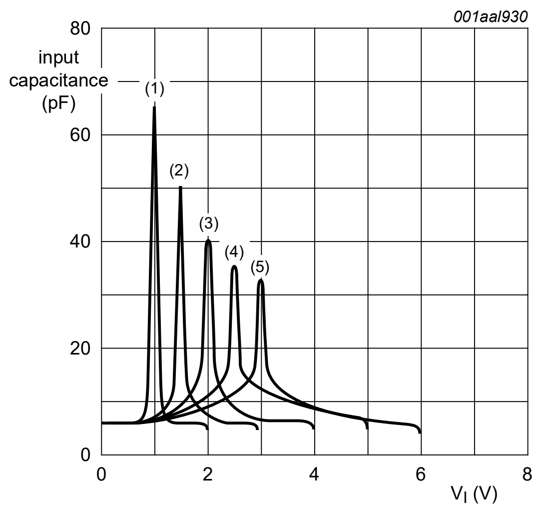


$$f = \frac{1}{T} \approx \frac{1}{2.2RC}$$

$$R_S \approx 2 \times R$$

The average I_{CC} (mA) is approximately 3.5 + 0.05 × f (MHz) × C (pF) at V_{CC} = 5.0 V.

Fig. 15. Astable multivibrator

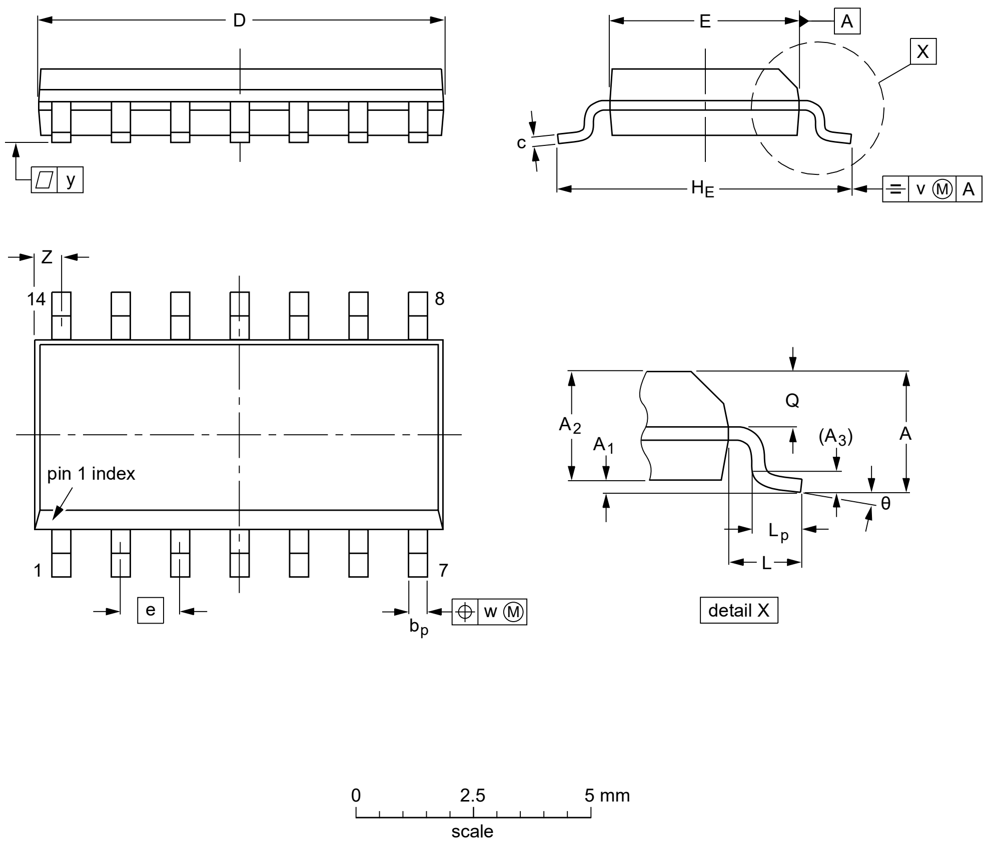


(1) V_{CC} = 2.0 V
(2) V_{CC} = 3.0 V
(3) V_{CC} = 4.0 V
(4) V_{CC} = 5.0 V
(5) V_{CC} = 6.0 V
T_{amb} = 25 °C.

Fig. 16. Input capacitance as function of input voltage

13. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

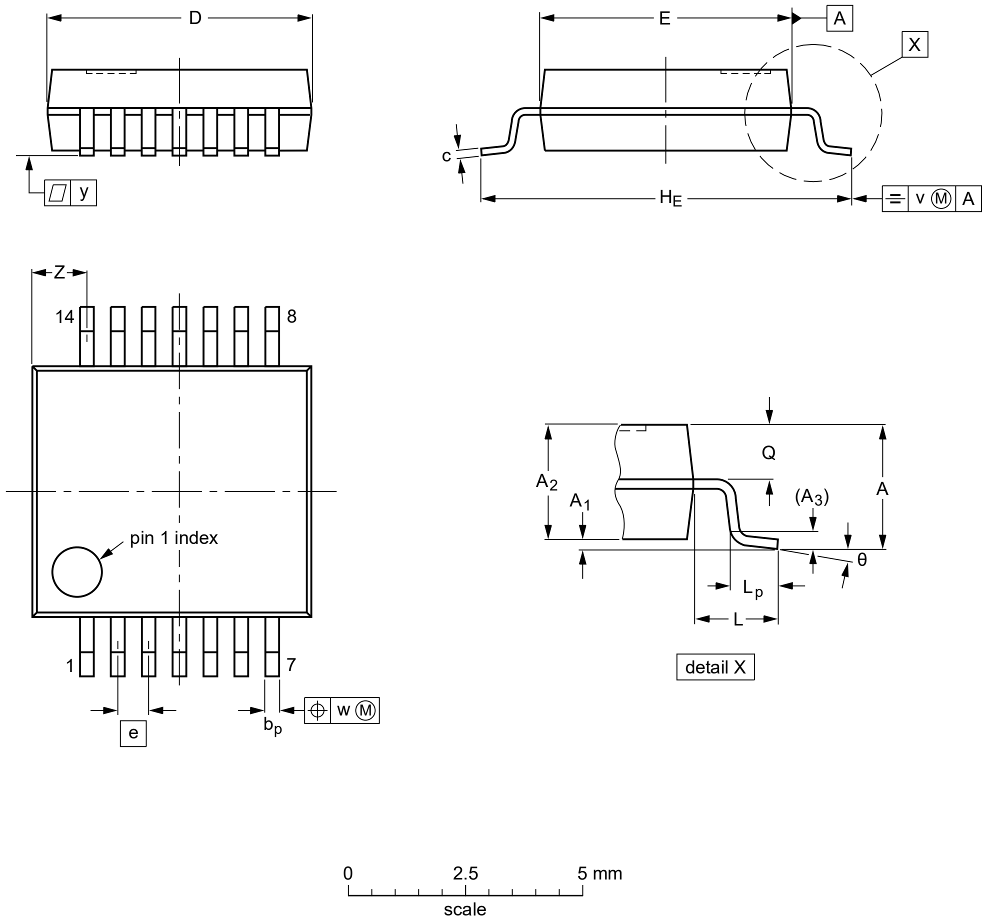
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig. 17. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

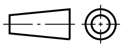
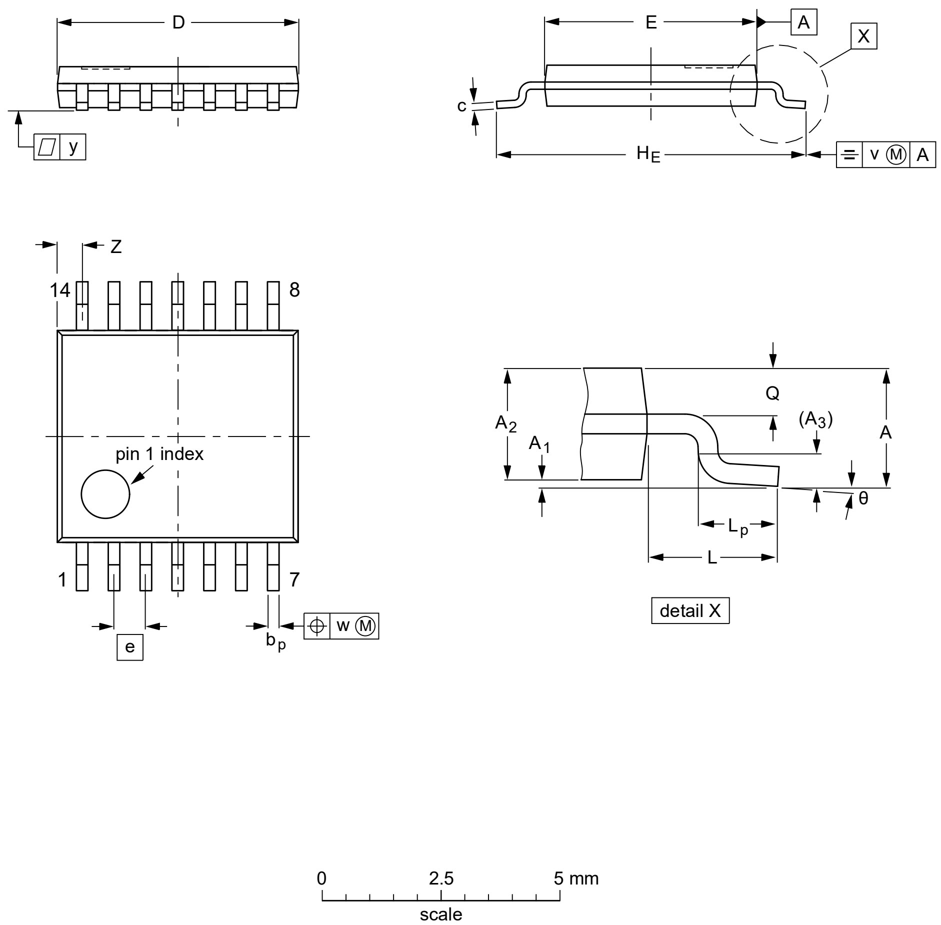
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				~~99-12-27~~ 03-02-19

Fig. 18. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

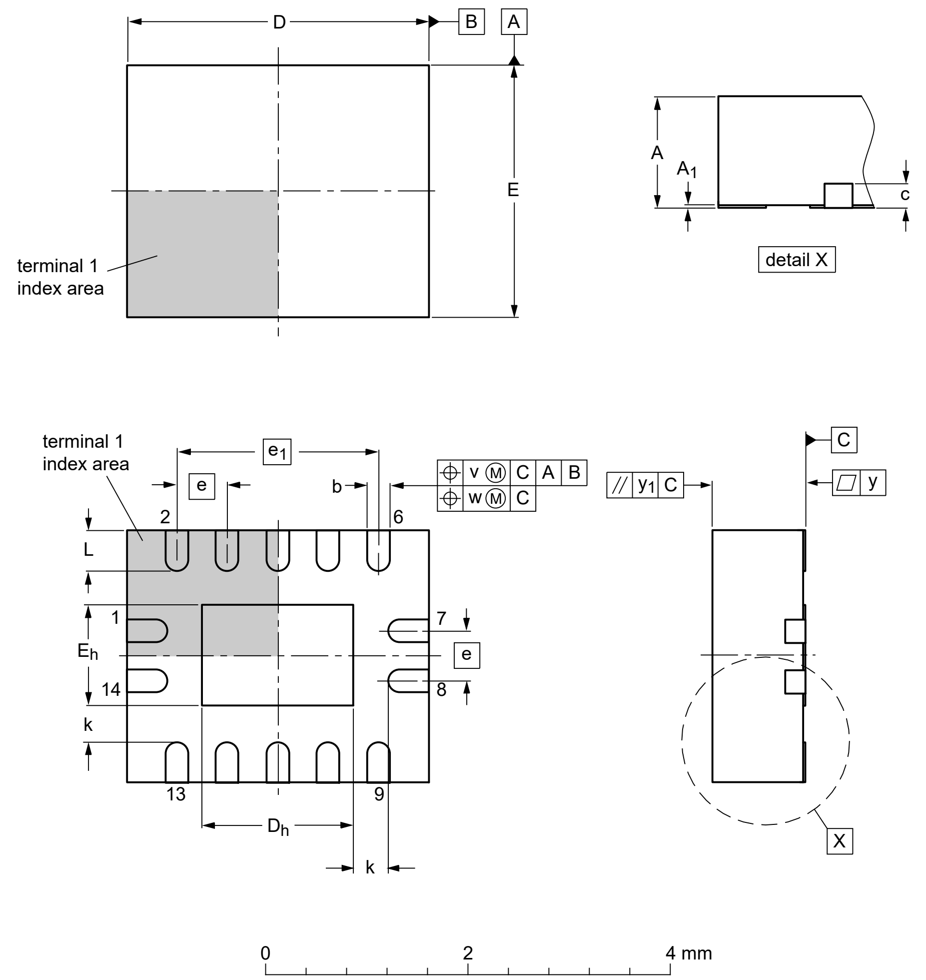
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig. 19. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



Dimensions (mm are the original dimensions)

Unit		A(1)	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	k	L	v	w	y	y_1
	max	1	0.05	0.30		3.1	1.65	2.6	1.15				0.5				
mm	nom		0.02	0.25	0.2	3.0	1.50	2.5	1.00	0.5	2		0.4	0.1	0.05	0.05	0.1
	min		0.00	0.18		2.9	1.35	2.4	0.85			0.2	0.3				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot762-1_po

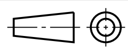
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT762-1		MO-241				~~15-04-10~~ 15-05-05

Fig. 20. Package outline SOT762-1 (DHVQFN14)

14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HCU04 v.8	20200716	Product data sheet	-	74HCU04 v.7
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 2 updated. • Section 7: Derating values for P_{tot} total power dissipation have been updated.			
74HCU04 v.7	20151208	Product data sheet	-	74HCU04 v.6
Modifications:	• Type number 74HCU04N (SOT27-1) removed. • Conditions V_{IL} and V_{IH} corrected (errata).			
74HCU04 v.6	20121227	Product data sheet	-	74HCU04 v.5
Modifications:	• New general description.			
74HCU04 v.5	20120806	Product data sheet	-	74HCU04 v.4
Modifications:	• Measurement points added to figure 6 (errata).			
74HCU04 v.4	20111212	Product data sheet	-	74HCU04 v.3
Modifications:	• Legal pages updated.			
74HCU04 v.3	20100916	Product data sheet	-	74HCU04_CNV v.2
74HCU04_CNV v.2	19970826	Product specification	-	-

16. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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