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**SN74AVCBH324245**
**32-BIT DUAL-SUPPLY BUS TRANSCEIVER**
**WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS**
SCES550B−FEBRUARY 2004−REVISED JUNE 2005

## FEATURES

- **Member of the Texas Instruments Widebus+™ Family**
- **DOC™ Circuitry Dynamically Changes Output Impedance, Resulting in Noise Reduction Without Speed Degradation**
- **Dynamic Drive Capability Is Equivalent to Standard Outputs With $I_{OH}$ and $I_{OL}$ of**
  - **±24 mA at 3-V $V_{CC}$**
  - **±15 mA at 2.3-V $V_{CC}$**
  - **±9 mA at 1.65-V $V_{CC}$**
  - **±6 mA at 1.4-V $V_{CC}$**
- **Control Inputs $V_{IH}/V_{IL}$ Levels Are Referenced to $V_{CCB}$ Voltage**
- **If Either $V_{CC}$ Input Is at GND, Both Ports Are in the High-Impedance State**

- **Inputs/Outputs Can Tolerate up to 4.6 V, Which Allows Mixed-Voltage-Mode Data Communications**
- **$I_{off}$ Supports Partial-Power-Down Mode Operation**
- **Fully Configurable Dual-Rail Design Allows Each Port to Operate Over Full 1.4-V to 3.6-V Power-Supply Range**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

## DESCRIPTION/ORDERING INFORMATION

This 32-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track $V_{CCA}$. $V_{CCA}$ accepts any supply voltage from 1.4 V to 3.6 V. The B port is designed to track $V_{CCB}$. $V_{CCB}$ accepts any supply voltage from 1.4 V to 3.6 V. This allows for universal low-voltage bidirectional translation between any of the 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

The SN74AVCBH324245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input is used to disable the outputs, so the buses effectively are isolated.

The SN74AVCBH324245 is designed so that the control pins (1DIR, 2DIR, 1$\overline{OE}$, and 2$\overline{OE}$) are supplied by $V_{CCB}$.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CCB}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. If either $V_{CC}$ input is at GND, both ports are in the high-impedance state.

### ORDERING INFORMATION

| $T_A$ | PACKAGE[1] | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| −40°C to 85°C | LFBGA – GKE | Tape and reel | SN74AVCBH324245KR | WN4245 |
| | LFBGA – ZKE | Tape and reel | 74AVCBH324245ZKER | |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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SCES550B−FEBRUARY 2004−REVISED JUNE 2005

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**GKE PACKAGE**
**(TOP VIEW)**
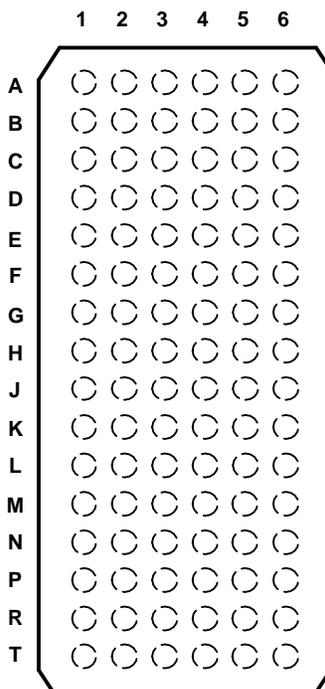


## TERMINAL ASSIGNMENTS

|   | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| **A** | 1B2 | 1B1 | 1DIR | 1$\overline{\text{OE}}$ | 1A1 | 1A2 |
| **B** | 1B4 | 1B3 | GND | GND | 1A3 | 1A4 |
| **C** | 1B6 | 1B5 | $V_{CCB}$ | $V_{CCA}$ | 1A5 | 1A6 |
| **D** | 1B8 | 1B7 | GND | GND | 1A7 | 1A8 |
| **E** | 2B2 | 2B1 | GND | GND | 2A1 | 2A2 |
| **F** | 2B4 | 2B3 | $V_{CCB}$ | $V_{CCA}$ | 2A3 | 2A4 |
| **G** | 2B6 | 2B5 | GND | GND | 2A5 | 2A6 |
| **H** | 2B7 | 2B8 | 2DIR | 2$\overline{\text{OE}}$ | 2A8 | 2A7 |
| **J** | 3B2 | 3B1 | 3DIR | 3$\overline{\text{OE}}$ | 3A1 | 3A2 |
| **K** | 3B4 | 3B3 | GND | GND | 3A3 | 3A4 |
| **L** | 3B6 | 3B5 | $V_{CCB}$ | $V_{CCA}$ | 3A5 | 3A6 |
| **M** | 3B8 | 3B7 | GND | GND | 3A7 | 3A8 |
| **N** | 4B2 | 4B1 | GND | GND | 4A1 | 4A2 |
| **P** | 4B4 | 4B3 | $V_{CCB}$ | $V_{CCA}$ | 4A3 | 4A4 |
| **R** | 4B6 | 4B5 | GND | GND | 4A5 | 4A6 |
| **T** | 4B7 | 4B8 | 4DIR | 4$\overline{\text{OE}}$ | 4A8 | 4A7 |

**FUNCTION TABLE**
**(EACH 8-BIT SECTION)**

| INPUTS | | OPERATION |
|---|---|---|
| $\overline{OE}$ | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

**LOGIC DIAGRAM (POSITIVE LOGIC)**
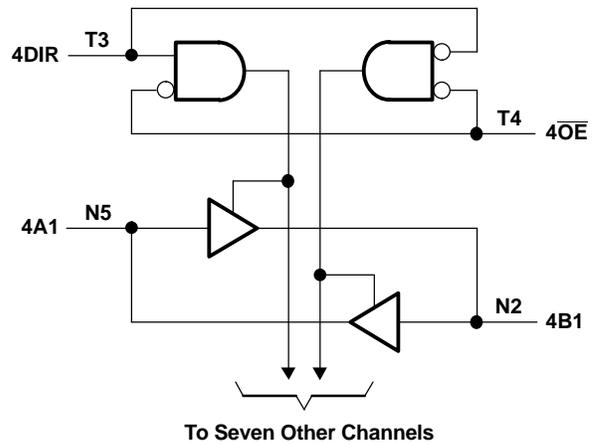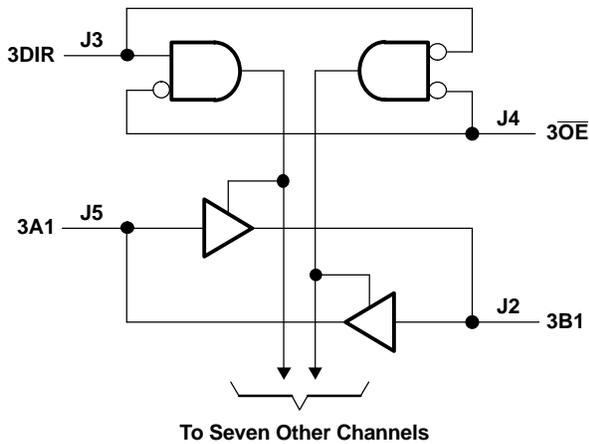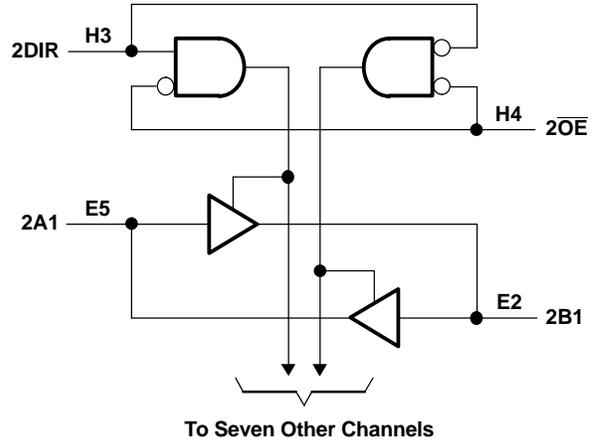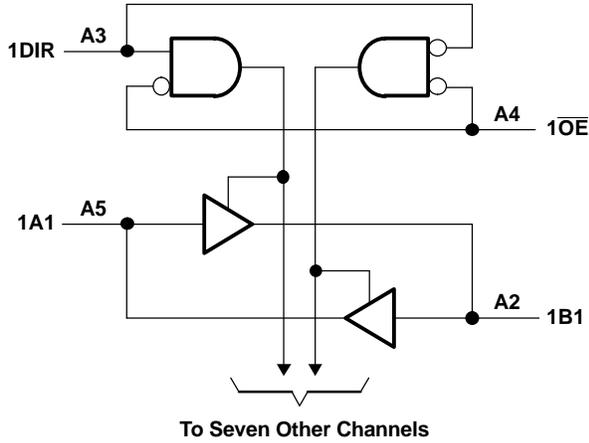


To Seven Other Channels

To Seven Other Channels

To Seven Other Channels

To Seven Other Channels

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## Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CCA}$ $V_{CCB}$ | Supply voltage range | | −0.5 | 4.6 | V |
| $V_I$ | Input voltage range[2] | I/O port (A port) | −0.5 | 4.6 | V |
| | | I/O port (B port) | −0.5 | 4.6 | |
| | | Control inputs | −0.5 | 4.6 | |
| $V_O$ | Voltage range applied to any output in the high-impedance or power-off state[2] | A port | −0.5 | 4.6 | V |
| | | B port | −0.5 | 4.6 | |
| $V_O$ | Voltage range applied to any output in the high or low state[2][3] | A port | −0.5 | $V_{CCA}$ + 0.5 | V |
| | | B port | −0.5 | $V_{CCB}$ + 0.5 | |
| $I_{IK}$ | Input clamp current | $V_I < 0$ | | −50 | mA |
| $I_{OK}$ | Output clamp current | $V_O < 0$ | | −50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| | Continuous current through each $V_{CCA}$, $V_{CCB}$, or GND | | | ±100 | mA |
| $\theta_{JA}$ | Package thermal impedance[4] | GKE/ZKE package | | 40 | °C/W |
| $T_{stg}$ | Storage temperature range | | −65 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

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## Recommended Operating Conditions[(1)(2)(3)]

| | | | $V_{CCI}$ | $V_{CCO}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CCA}$ | Supply voltage | | | | 1.4 | 3.6 | V |
| $V_{CCB}$ | Supply voltage | | | | 1.4 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | Data inputs | 1.4 V to 1.95 V | | $V_{CCI} \times 0.65$ | 3.6 | V |
| | | | 1.95 V to 2.7 V | | 1.7 | 3.6 | |
| | | | 2.7 V to 3.6 V | | 2 | 3.6 | |
| $V_{IL}$ | Low-level input voltage | Data inputs | 1.4 V to 1.95 V | | 0 | $V_{CCI} \times 0.35$ | V |
| | | | 1.95 V to 2.7 V | | 0 | 0.7 | |
| | | | 2.7 V to 3.6 V | | 0 | 0.8 | |
| $V_{IH}$ | High-level input voltage | Control inputs (referenced to $V_{CCB}$) | 1.4 V to 1.95 V | | $V_{CCB} \times 0.65$ | $V_{CCB}$ | V |
| | | | 1.95 V to 2.7 V | | 1.7 | $V_{CCB}$ | |
| | | | 2.7 V to 3.6 V | | 2 | $V_{CCB}$ | |
| $V_{IL}$ | Low-level input voltage | Control inputs (referenced to $V_{CCB}$) | 1.4 V to 1.95 V | | 0 | $V_{CCB} \times 0.35$ | V |
| | | | 1.95 V to 2.7 V | | 0 | 0.7 | |
| | | | 2.7 V to 3.6 V | | 0 | 0.8 | |
| $V_O$ | Output voltage | | | | 0 | $V_{CCO}$ | V |
| $I_{OH}$ | High-level output current | | | 1.4 V to 1.6 V | | −2 | mA |
| | | | | 1.65 V to 1.95 V | | −4 | |
| | | | | 2.3 V to 2.7 V | | −8 | |
| | | | | 3 V to 3.6 V | | −12 | |
| $I_{OL}$ | Low-level output current | | | 1.4 V to 1.6 V | | 2 | mA |
| | | | | 1.65 V to 1.95 V | | 4 | |
| | | | | 2.3 V to 2.7 V | | 8 | |
| | | | | 3 V to 3.6 V | | 12 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | | | | 5 | ns/V |
| $T_A$ | Operating free-air temperature | | | | −40 | 85 | °C |

(1)  $V_{CCI}$ is the $V_{CC}$ associated with the data input port.
(2)  $V_{CCO}$ is the $V_{CC}$ associated with the output port.
(3)  All unused data inputs of the device must be held at $V_{CCI}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# 32-BIT DUAL-SUPPLY BUS TRANSCEIVER
# WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

SCES550B−FEBRUARY 2004−REVISED JUNE 2005

## Electrical Characteristics[1]

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CCA}$ | $V_{CCB}$ | MIN | TYP[2] | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $I_{OH}$ = −100 µA, | $V_I = V_{IH}$ | 1.4 V to 3.6 V | 1.4 V to 3.6 V | $V_{CCO}$ − 0.2 | | | V |
| | | $I_{OH}$ = −2 mA, | $V_I = V_{IH}$ | 1.4 V | 1.4 V | 1.05 | | | |
| | | $I_{OH}$ = −4 mA, | $V_I = V_{IH}$ | 1.65 V | 1.65 V | 1.2 | | | |
| | | $I_{OH}$ = −8 mA, | $V_I = V_{IH}$ | 2.3 V | 2.3 V | 1.75 | | | |
| | | $I_{OH}$ = −12 mA, | $V_I = V_{IH}$ | 3 V | 3 V | 2.3 | | | |
| $V_{OL}$ | | $I_{OH}$ = 100 µA, | $V_I = V_{IL}$ | 1.4 V to 3.6 V | 1.4 V to 3.6 V | | | 0.2 | V |
| | | $I_{OH}$ = 2 mA, | $V_I = V_{IL}$ | 1.4 V | 1.4 V | | | 0.35 | |
| | | $I_{OH}$ = 4 mA, | $V_I = V_{IL}$ | 1.65 V | 1.65 V | | | 0.45 | |
| | | $I_{OH}$ = 8 mA, | $V_I = V_{IL}$ | 2.3 V | 2.3 V | | | 0.55 | |
| | | $I_{OH}$ = 12 mA, | $V_I = V_{IL}$ | 3 V | 3 V | | | 0.7 | |
| $V_{OH}$ | | $I_{OHD}$ = −6 mA, | $V_I = V_{IH}$ | 1.4 V | 1.4 V | 1.05 | | | V |
| | | $I_{OHD}$ = −9 mA, | $V_I = V_{IH}$ | 1.65 V | 1.65 V | 1.2 | | | |
| | | $I_{OHD}$ = −15 mA, | $V_I = V_{IH}$ | 2.3 V | 2.3 V | 1.75 | | | |
| | | $I_{OHD}$ = −24 mA, | $V_I = V_{IH}$ | 3 V | 3 V | 2.3 | | | |
| $V_{OL}$ | | $I_{OHD}$ = 6 mA, | $V_I = V_{IL}$ | 1.4 V | 1.4 V | | | 0.35 | V |
| | | $I_{OHD}$ = 9 mA, | $V_I = V_{IL}$ | 1.65 V | 1.65 V | | | 0.45 | |
| | | $I_{OHD}$ = 15 mA, | $V_I = V_{IL}$ | 2.3 V | 2.3 V | | | 0.55 | |
| | | $I_{OHD}$ = 24 mA, | $V_I = V_{IL}$ | 3 V | 3 V | | | 0.7 | |
| $I_I$ | Control inputs | $V_I = V_{CCB}$ or GND | | 1.4 V to 3.6 V | 3.6 V | | | ±2.5 | µA |
| $I_{BHL}$[3] | | $V_I$ = 0.49 V | | 1.4 V | 1.4 V | 11 | | | µA |
| | | $V_I$ = 0.57 V | | 1.65 V | 1.65 V | 25 | | | |
| | | $V_I$ = 0.7 V | | 2.3 V | 2.3 V | 45 | | | |
| | | $V_I$ = 0.8 V | | 3 V | 3 V | 75 | | | |
| $I_{BHH}$[4] | | $V_I$ = 0.49 V | | 1.4 V | 1.4 V | −11 | | | µA |
| | | $V_I$ = 1.07 V | | 1.65 V | 1.65 V | −25 | | | |
| | | $V_I$ = 1.7 V | | 2.3 V | 2.3 V | −45 | | | |
| | | $V_I$ = 2 V | | 3 V | 3 V | −75 | | | |
| $I_{BHLO}$[5] | | $V_I$ = 0 to $V_{CC}$ | | 1.6 V | 1.6 V | 100 | | | µA |
| | | | | 1.95 V | 1.95 V | 200 | | | |
| | | | | 2.7 V | 2.7 V | 300 | | | |
| | | | | 3.6 V | 3.6 V | 525 | | | |
| $I_{BHHO}$[6] | | $V_I$ = 0 to $V_{CC}$ | | 1.6 V | 1.6 V | −100 | | | µA |
| | | | | 1.95 V | 1.95 V | −200 | | | |
| | | | | 2.7 V | 2.7 V | −300 | | | |
| | | | | 3.6 V | 3.6 V | −525 | | | |

(1)  $V_{CCO}$ is the $V_{CC}$ associated with the output port.
(2)  All typical values are at $T_A$ = 25°C.
(3)  The bus-hold circuit can sink at least the minimum low sustaining current at $V_{IL}$ max. $I_{BHL}$ should be measured after lowering $V_{IN}$ to GND and then raising it to $V_{IL}$ max.
(4)  The bus-hold circuit can source at least the minimum high sustaining current at $V_{IH}$ min. $I_{BHH}$ should be measured after raising $V_{IN}$ to $V_{CC}$ and then lowering it to $V_{IH}$ min.
(5)  An external driver must source at least $I_{BHLO}$ to switch this node from low to high.
(6)  An external driver must sink at least $I_{BHHO}$ to switch this node from high to low.

## Electrical Characteristics[1][2] (continued)

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CCA}$ | $V_{CCB}$ | MIN | TYP[3] | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $I_{off}$ | A port | $V_I$ or $V_O$ = 0 to 3.6 V | | 0 V | 0 to 3.6 V | | | ±10 | μA |
| | B port | | | 0 to 3.6 V | 0 V | | | ±10 | |
| $I_{OZ}$[4] | A or B port | $V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND | $\overline{OE} = V_{IH}$ | 3.6 V | 3.6 V | | | ±12.5 | μA |
| | B port | | $\overline{OE}$ = don't care | 0 V | 3.6 V | | | ±12.5 | |
| | A port | | | 3.6 V | 0 V | | | ±12.5 | |
| $I_{CCA}$ | | $V_I = V_{CCI}$ or GND,     $I_O$ = 0 | | 1.6 V | 1.6 V | | | 40 | μA |
| | | | | 1.95 V | 1.95 V | | | 40 | |
| | | | | 2.7 V | 2.7 V | | | 60 | |
| | | | | 0 V | 3.6 V | | | −80 | |
| | | | | 3.6 V | 0 V | | | 80 | |
| | | | | 3.6 V | 3.6 V | | | 80 | |
| $I_{CCB}$ | | $V_I = V_{CCI}$ or GND,     $I_O$ = 0 | | 1.6 V | 1.6 V | | | 40 | μA |
| | | | | 1.95 V | 1.95 V | | | 40 | |
| | | | | 2.7 V | 2.7 V | | | 60 | |
| | | | | 0 V | 3.6 V | | | 80 | |
| | | | | 3.6 V | 0 V | | | −80 | |
| | | | | 3.6 V | 3.6 V | | | 80 | |
| $C_i$ | Control inputs | $V_I$ = 3.3 V or GND | | 3.3 V | 3.3 V | | 4 | | pF |
| $C_{io}$ | A or B ports | $V_O$ = 3.3 V or GND | | 3.3 V | 3.3 V | | 5 | | pF |

(1)  $V_{CCO}$ is the $V_{CC}$ associated with the output port.
(2)  $V_{CCI}$ is the $V_{CC}$ associated with the input port.
(3)  All typical values are at $T_A$ = 25°C.
(4)  For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.

## Switching Characteristics

over recommended operating free-air temperature range, $V_{CCA}$ = 1.5 V ± 0.1 V (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCB}$ = 1.5 V ± 0.1 V | | $V_{CCB}$ = 1.8 V ± 0.15 V | | $V_{CCB}$ = 2.5 V ± 0.2 V | | $V_{CCB}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A | B | 1.7 | 6.7 | 1.9 | 6.4 | 1.8 | 5.5 | 1.5 | 5.8 | ns |
| | B | A | 1.8 | 6.8 | 1.7 | 6.2 | 1.6 | 5.9 | 1.5 | 5.9 | |
| $t_{en}$ | $\overline{OE}$ | A | 2.1 | 9 | 2.9 | 9.8 | 3.2 | 10 | 3 | 9.8 | ns |
| | | B | 2.5 | 8.4 | 2.4 | 8 | 2.3 | 7.6 | 2.2 | 7.5 | |
| $t_{dis}$ | $\overline{OE}$ | A | 2.1 | 7.1 | 2.3 | 6.4 | 1.7 | 5.1 | 1.6 | 4.8 | ns |
| | | B | 2.2 | 6.9 | 1.8 | 6.4 | 1.1 | 5.8 | 1.8 | 5.7 | |

## Switching Characteristics

over recommended operating free-air temperature range, $V_{CCA}$ = 1.8 V ± 0.15 V (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCB}$ = 1.5 V ± 0.1 V | | $V_{CCB}$ = 1.8 V ± 0.15 V | | $V_{CCB}$ = 2.5 V ± 0.2 V | | $V_{CCB}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A | B | 1.7 | 6.4 | 1.8 | 6 | 1.7 | 4.7 | 1.6 | 4.3 | ns |
| | B | A | 2 | 6.6 | 1.8 | 6 | 1.8 | 5.6 | 1.8 | 5.5 | |
| $t_{en}$ | $\overline{OE}$ | A | 1.8 | 7.6 | 2.6 | 7.7 | 2.6 | 7.6 | 2.6 | 7.4 | ns |
| | | B | 2.5 | 8.2 | 2.5 | 7.5 | 2.4 | 7.4 | 2.3 | 7.2 | |
| $t_{dis}$ | $\overline{OE}$ | A | 1.8 | 7 | 2.5 | 6.3 | 1.8 | 4.7 | 1.7 | 4.4 | ns |
| | | B | 2.5 | 6.7 | 2.3 | 6.1 | 2.2 | 5.5 | 1.3 | 5.3 | |

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SCES550B – FEBRUARY 2004 – REVISED JUNE 2005

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## Switching Characteristics

over recommended operating free-air temperature range, $V_{CCA}$ = 2.5 V ± 0.2 V (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCB}$ = 1.5 V ± 0.1 V | | $V_{CCB}$ = 1.8 V ± 0.15 V | | $V_{CCB}$ = 2.5 V ± 0.2 V | | $V_{CCB}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A | B | 1.6 | 6 | 1.8 | 5.6 | 1.5 | 4 | 1.5 | 3.4 | ns |
| | B | A | 1.7 | 5.4 | 1.7 | 4.6 | 1.5 | 4 | 1.5 | 3.7 | |
| $t_{en}$ | $\overline{OE}$ | A | 1.7 | 5.7 | 2.2 | 5.5 | 2.2 | 5.3 | 2.2 | 5.1 | ns |
| | | B | 3.1 | 6.1 | 2.5 | 5.6 | 2.2 | 5.3 | 1.9 | 4.2 | |
| $t_{dis}$ | $\overline{OE}$ | A | 1.2 | 5.8 | 1.9 | 5 | 1.4 | 3.6 | 1.3 | 3.3 | ns |
| | | B | 2.4 | 6 | 3 | 5.2 | 1.4 | 3.6 | 1.2 | 3 | |

## Switching Characteristics

over recommended operating free-air temperature range, $V_{CCA}$ = 3.3 V ± 0.3 V (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCB}$ = 1.5 V ± 0.1 V | | $V_{CCB}$ = 1.8 V ± 0.15 V | | $V_{CCB}$ = 2.5 V ± 0.2 V | | $V_{CCB}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A | B | 1.5 | 5.9 | 1.7 | 5.4 | 1.5 | 3.7 | 1.4 | 3.1 | ns |
| | B | A | 1.5 | 5.8 | 1.5 | 4.2 | 1.5 | 3.3 | 1.4 | 3.1 | |
| $t_{en}$ | $\overline{OE}$ | A | 1.6 | 4.9 | 2 | 4.5 | 2 | 4.3 | 1.9 | 4.1 | ns |
| | | B | 2 | 5.1 | 2 | 4.6 | 2.2 | 5.2 | 1.9 | 4.1 | |
| $t_{dis}$ | $\overline{OE}$ | A | 1.3 | 6.9 | 2.1 | 5.5 | 1.6 | 3.8 | 1.5 | 3.5 | ns |
| | | B | 2.3 | 5.5 | 1.9 | 4.5 | 1.3 | 3.5 | 1.2 | 3.5 | |

## Operating Characteristics

$V_{CCA}$ and $V_{CCB}$ = 3.3 V, $T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pdA}$ ($V_{CCA}$) | Power-dissipation capacitance per transceiver, A-port input, B-port output | Outputs enabled | $C_L$ = 0,    f = 10 MHz | 14 | pF |
| | | Outputs disabled | | 7 | |
| | Power-dissipation capacitance per transceiver, B-port input, A-port output | Outputs enabled | | 20 | |
| | | Outputs disabled | | 7 | |
| $C_{pdB}$ ($V_{CCB}$) | Power-dissipation capacitance per transceiver, A-port input, B-port output | Outputs enabled | $C_L$ = 0,    f = 10 MHz | 20 | pF |
| | | Outputs disabled | | 7 | |
| | Power-dissipation capacitance per transceiver, B-port input, A-port output | Outputs enabled | | 14 | |
| | | Outputs disabled | | 7 | |

TEXAS INSTRUMENTS
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**SN74AVCBH324245**
**32-BIT DUAL-SUPPLY BUS TRANSCEIVER**
**WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS**
SCES550B−FEBRUARY 2004−REVISED JUNE 2005

## Output Description

The DOC™ circuitry is implemented, which, during the transition, initially lowers the output impedance to effectively drive the load and, subsequently, raises the impedance to reduce noise. Figure 1 shows typical $V_{OL}$ vs $I_{OL}$ and $V_{OH}$ vs $I_{OH}$ curves to illustrate the output impedance and drive capability of the circuit. At the beginning of the signal transition, the DOC circuit provides a maximum dynamic drive that is equivalent to a high-drive standard-output device. For more information, refer to the TI application reports, *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.
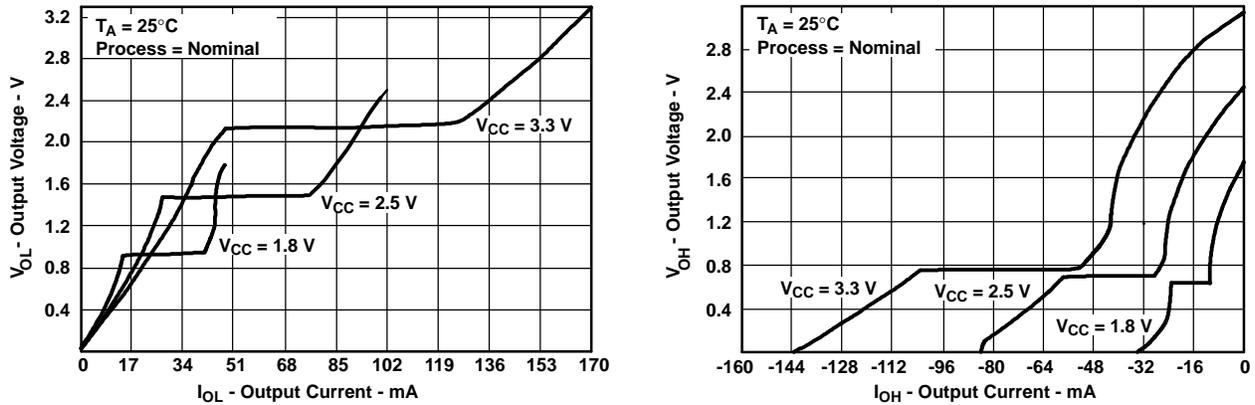


Figure 1. Typical Output Voltage vs Output Current

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## PARAMETER MEASUREMENT INFORMATION
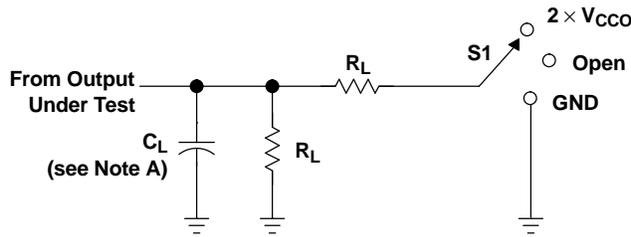
| TEST | S1 |
|------|-----|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $2 \times V_{CCO}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

**LOAD CIRCUIT**

| $V_{CCO}$ | $C_L$ | $R_L$ | $V_{TP}$ |
|-----------|-------|-------|----------|
| $1.5\ V \pm 0.1\ V$ | 15 pF | 2 kΩ | 0.1 V |
| $1.8\ V \pm 0.15\ V$ | 30 pF | 1 kΩ | 0.15 V |
| $2.5\ V \pm 0.2\ V$ | 30 pF | 500 Ω | 0.15 V |
| $3.3\ V \pm 0.3\ V$ | 30 pF | 500 Ω | 0.3 V |

**VOLTAGE WAVEFORMS**
**PULSE DURATION**

**VOLTAGE WAVEFORMS**
**PROPAGATION DELAY TIMES**

**VOLTAGE WAVEFORMS**
**ENABLE AND DISABLE TIMES**
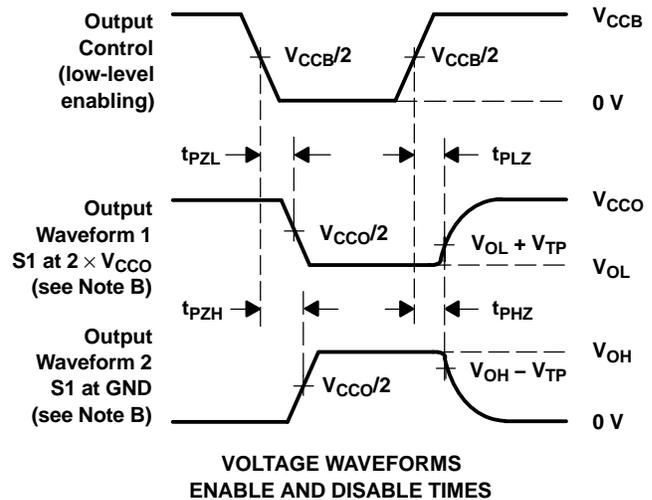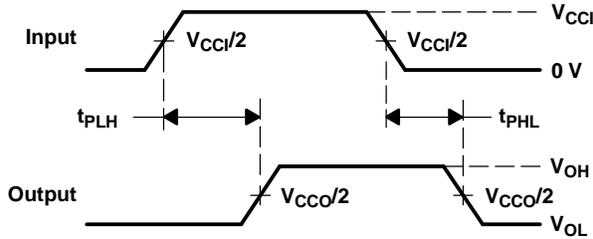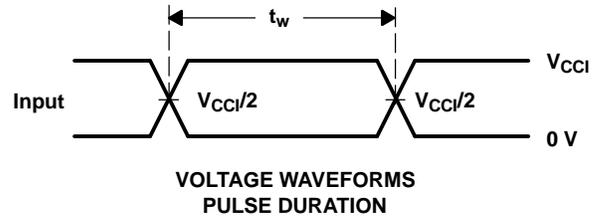
NOTES: A. $C_L$ includes probe and jig capacitance.
     B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
     C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50\ Ω$, dv/dt ≥ 1 V/ns.
     D. The outputs are measured one at a time, with one transition per measurement.
     E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
     F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
     G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
     H. $V_{CCI}$ is the $V_{CC}$ associated with the input port.
     I. $V_{CCO}$ is the $V_{CC}$ associated with the output port.

**Figure 2. Load Circuit and Voltage Waveforms**

# PACKAGE OPTION ADDENDUM

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 74AVCBH324245ZKER | NRND | LFBGA | ZKE | 96 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 85 | WN4245 | |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 74AVCBH324245ZKER | LFBGA | ZKE | 96 | 1000 | 330.0 | 24.4 | 5.7 | 13.7 | 2.0 | 8.0 | 24.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| 74AVCBH324245ZKER | LFBGA | ZKE | 96 | 1000 | 336.6 | 336.6 | 41.3 |

ZKE (R−PBGA−N96)                    PLASTIC BALL GRID ARRAY



A1 Corner

Bottom View

1 2 3 4 5 6

4,00

0,80

0,40

0,80

0,40

12,00

5,60
5,40

13,60
13,40

0,95
0,85

1,40 Max

Seating Plane

0,12

96X Ø 0,55
0,45

0,45
0,35

⊕ Ø 0,08 Ⓜ

4204493/C  06/04
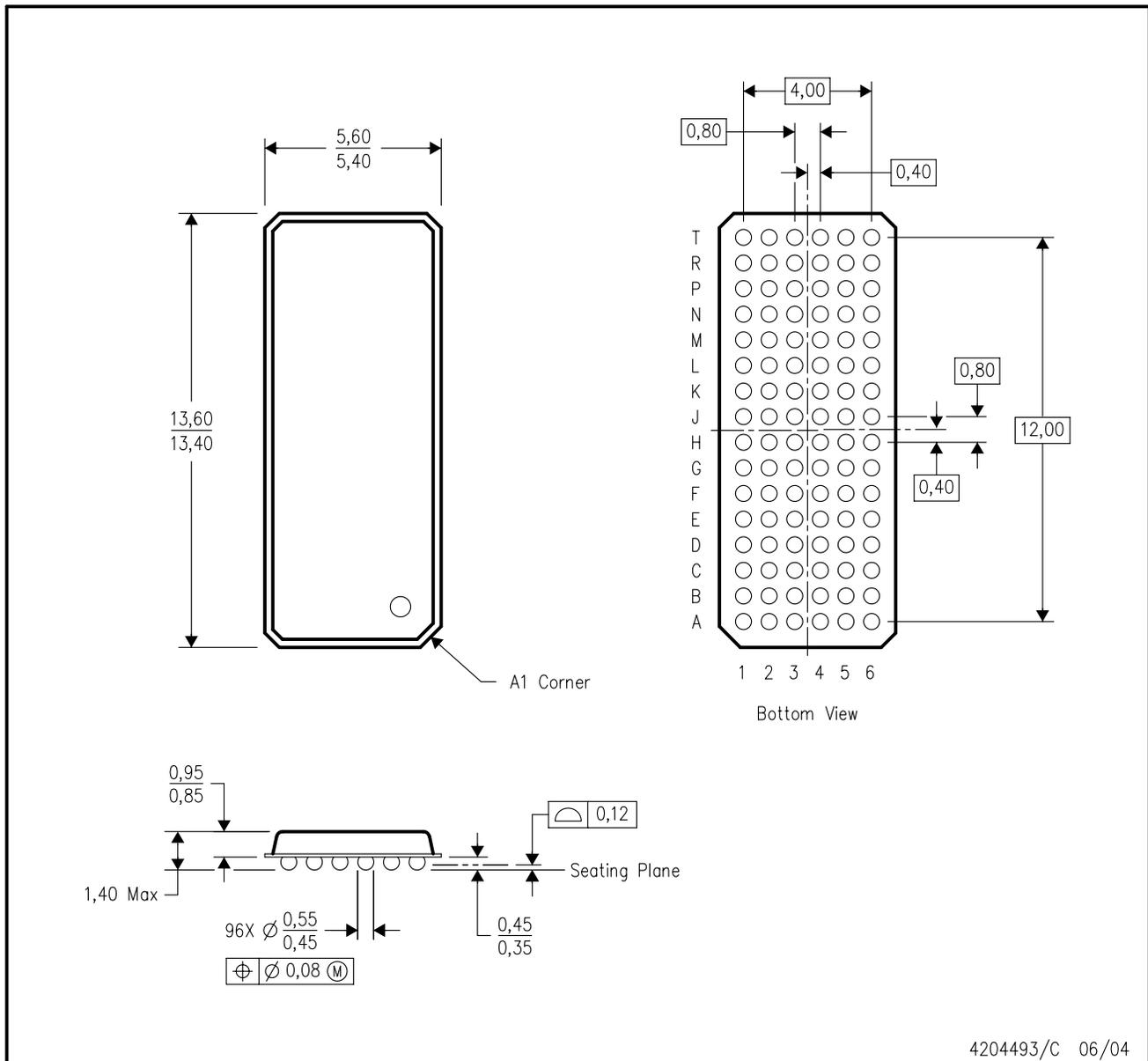
NOTES:    A.    All linear dimensions are in millimeters.
          B.    This drawing is subject to change without notice.
          C.    Falls within JEDEC MO−205 variation CC.
          D.    This package is lead−free.  Refer to the 96 GKE package (drawing 4188953) for tin−lead (SnPb).

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