

LM49153 Boomer™ Mono Audio Subsystem with Class G Headphone Amplifier, Class D Speaker Amplifier, Noise Gate and Speaker Protection

Check for Samples: [LM49153](#)

FEATURES

- Class G Ground Referenced Headphone Outputs
- High Efficiency Class D Amplifier with Spread Spectrum
- No Clip
- Speaker Protection
- Noise Gate
- I²C Volume and Mode Control
- Advanced Click-and-Pop Suppression
- Micro-Power Shutdown

APPLICATIONS

- Feature Phones
- Smart Phones

KEY SPECIFICATIONS

- Class G Headphone Amplifier, $HPV_{DD} = 1.8V$, $R_L = 32\Omega$
 - $IDDQ_{HP}$, 1.2mA (Typ)
 - P_{OUT} , THD+N ≤ 1%, 25mW (Typ)
 - HP V_{OS} , 0.5mV (Typ)
- Mono Class D Speaker Amplifier, $R_L = 8\Omega$, THD+N < 1%
 - P_{OUT} , $LSV_{DD} = 5.0V$, 1.35W (Typ)
 - P_{OUT} , $LSV_{DD} = 3.6V$, 680mW (Typ)
 - Efficiency 88% (Typ)

DESCRIPTION

The LM49153 is a fully integrated audio subsystem designed for portable handheld applications such as cellular phones. Part of Texas Instruments' PowerWise family of products, the LM49153 combines an earpiece switch, a high efficiency 25mW class G headphone amplifier, and a high efficiency 1.35W class D loudspeaker into a single device.

The headphone amplifiers feature Texas Instruments' class G ground referenced architecture that creates a ground-referenced output with dynamic supply rails for optimum efficiency. The class D amplifier features an ALC (Automatic Level Control) with a noise gate that provides both no-clip and speaker protection.

Mode selection, shutdown control, and volume are controlled through an I²C compatible interface.

Click and pop suppression eliminates audible transients on power-up/down and during shutdown. The LM49153 is available in an ultra-small 25-bump 0.4mm pitch DSBGA package (2.30mm x 2.42mm).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Boomer is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

Typical Application

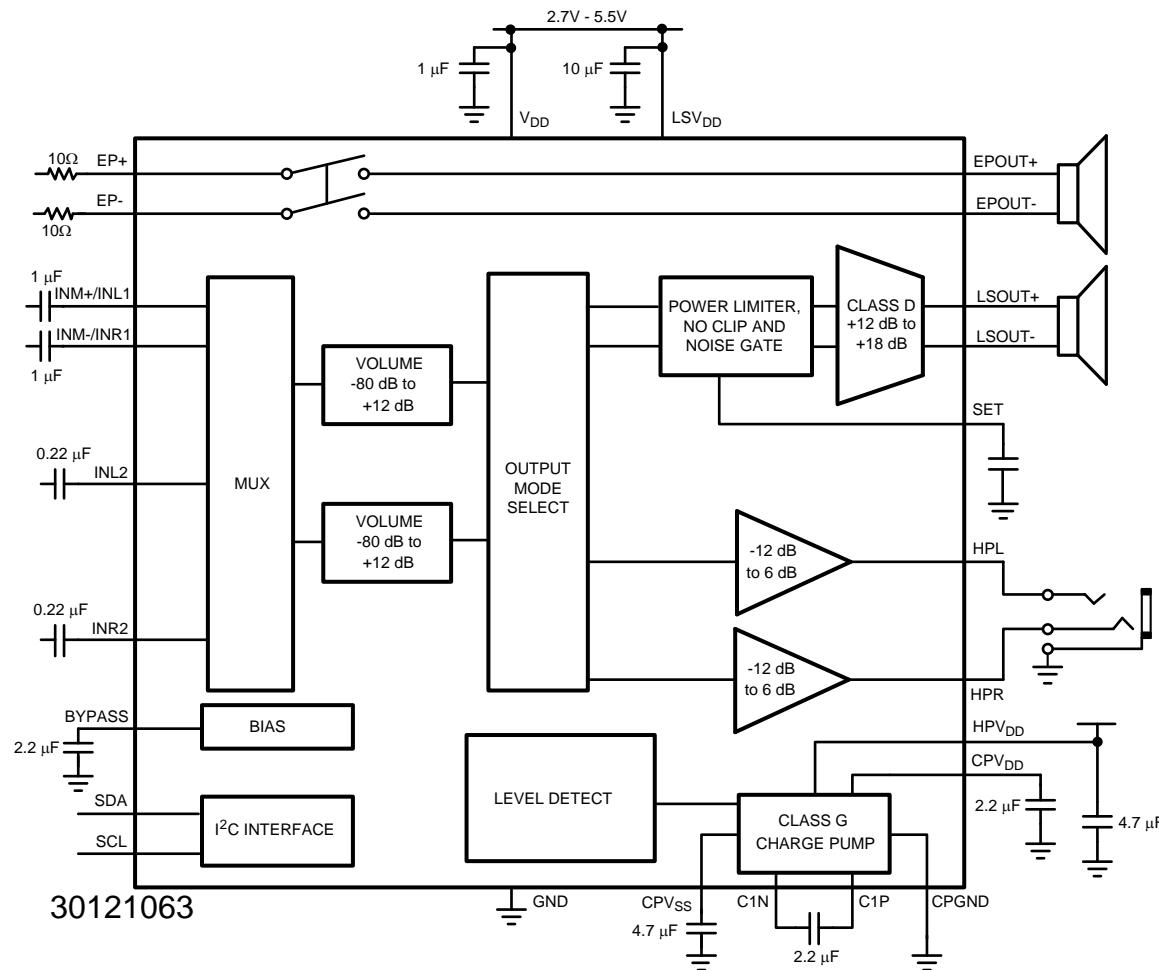
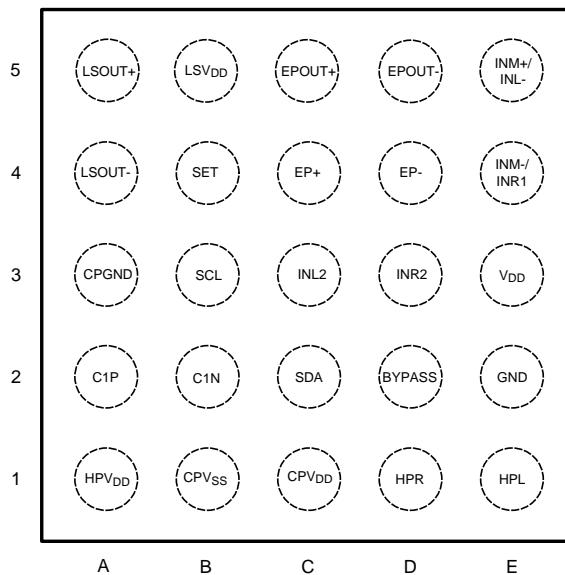


Figure 1. Typical Audio Amplifier Application Circuit

Connection Diagram



**Figure 2. 25 Bump DSBGA Package
Top View
See Package Number YFQ0025**

BUMP DESCRIPTION

Bump	Name	Description
A1	HPVDD	Headphone Power Supply
A2	C1P	Charge Pump Flying Capacitor Positive Terminal
A3	CPGND	Charge Pump Ground
A4	LSOUT-	Loudspeaker Inverting Output
A5	LSOUT+	Loudspeaker Non-Inverting Output
B1	CPVSS	Charge Pump Output
B2	C1N	Charge Pump Flying Capacitor Negative Terminal
B3	SCL	I ² C Serial Clock Input
B4	SET	ALC Timing Set
B5	LSV _{DD}	Loudspeaker Power Supply
C1	CPVDD	Charge Pump Power Supply
C2	SDA	I ² C Serial Data Input
C3	INL2	Left Channel Input 2
C4	EP+	Earpiece Non-Inverting Input
C5	EPOUT+	Earpiece Non-Inverting Output
D1	HPR	Right Channel Headphone Output
D2	BYPASS	Mid-Rail Bias Bypass Node
D3	INR2	Right Channel Input 2
D4	EP-	Earpiece Inverting Input
D5	EPOUT-	Earpiece Inverting Output
E1	HPL	Left Channel Headphone Output
E2	GND	Ground
E3	V _{DD}	Power Supply
E4	INM-/INR1	Mono Channel Inverting Input/Right Channel Input 1
E5	INM+/INL1	Mono Channel Non-Inverting Input/Left Channel Input 1



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾⁽³⁾

Supply Voltage (V_{DD} , LSV_{DD}) ⁽¹⁾	6V
Supply Voltage (HPV_{DD}) ⁽¹⁾	3V
Storage Temperature	-635°C to +150°C
Input Voltage	-0.3 to V_{DD} +0.3
Power Dissipation ⁽⁴⁾	Internally Limited
ESD Rating ⁽⁵⁾	2.0kV
ESD Rating ⁽⁶⁾	200V
Junction Temperature	150°C
Thermal Resistance	θ_{JA} (YFQ0025)
Soldering Information	See AN-1112 (SNVA009) "DSBGA Wafer Level Chip Scale Package"

- (1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
- (2) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.
- (3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} , θ_{JA} , and the ambient temperature, T_A . The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in *Absolute Maximum Ratings*, whichever is lower.
- (5) Human body model, applicable std. JESD22-A114C.
- (6) Machine model, applicable std. JESD22-A115-A.

Operating Ratings

Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$	-40°C $\leq T_A \leq$ +85°C
	Supply Voltage (V_{DD} , LSV_{DD})	2.7V $\leq V_{DD} \leq$ 5.5V
	Supply Voltage (HPV_{DD})	1.7V $\leq HPV_{DD} \leq$ 2.0V

Electrical Characteristics $V_{DD} = 3.6V$, $HPV_{DD} = 1.8V^{(1)(2)}$

The following specifications apply for $V_{DD} = LSV_{DD}$, $A_V = 0dB$, $R_L = 15\mu H + 8\Omega + 15\mu H$ (Loudspeaker), $R_L = 32\Omega$ (Headphone), $C_{SET} = 0.1\mu F$, $f = 1kHz$, ALC off, unless otherwise specified. Limits apply for $T_A = 25^\circ C$.⁽³⁾

Symbol	Parameter	Conditions	LM49153		Units (Limits)
			Typical ⁽⁴⁾	Limits ⁽⁵⁾	
I_{DD}	Supply Current	$V_{IN} = 0$, No Load			
		EP Receiver (Output Mode Bit EP Bypass = 1)	0.3	2.5	μA (max)
		LS only (Mode 2) V_{DD} , LSV_{DD} HPV_{DD}	3.0 0	4.3	mA (max) mA
		HP only (Mode 1) $V_{DD} + LSV_{DD}$ HPV_{DD}	1.8 1.2	2.5 1.6	mA (max) mA (max)
		LS + HP (Mode 6) $V_{DD} + LSV_{DD}$ HPV_{DD}	4.3 1.2	5.5 1.6	mA (max) mA (max)
I_{SD}	Shutdown Current	$V_{SCL} = V_{SDA} = 3.6V$	0.3	2.5	μA (max)
V_{OS}	Output Offset Voltage	$V_{IN} = 0$, Mode 3, 6, 9			
		LS Output, $R_L = 8\Omega$, $A_V = 12dB$	9		mV
		HP Output, $R_L = 32\Omega$, $A_V = 0dB$	0.5		mV
t_{WU}	Wake Up Time	HP Mode, $C_{BYPASS} = 2.2\mu F$ Normal turn on time Fast turn on time	32 18		ms ms
A_{VOL}	Volume Control	Mute	-86		dB
		Minimum Gain Setting (mono input)	-52.5	-51 -54	dB (max) dB (min)
		Maximum Gain Setting (mono input)	12	12.5 11.5	dB (max) dB (min)
		Minimum Gain Setting (stereo input)	-80		dB (max) dB (min)
		Maximum Gain Setting (stereo input)	18		dB (max) dB (min)

- (1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
- (2) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.
- (3) Loudspeaker R_L is a resistive load in series with two inductors to simulate an actual speaker load. For $R_L = 8\Omega$, the load is $15\mu H + 8\Omega + 15\mu H$. For $R_L = 4\Omega$, the load is $15\mu H + 4\Omega + 15\mu H$.
- (4) Typical values represent most likely parametric norms at $T_A = +25^\circ C$, and at the *Recommended Operation Conditions* at the time of product characterization and are not specified.
- (5) Datasheet min/max specification limits are specified by test or statistical analysis.

Electrical Characteristics $V_{DD} = 3.6V$, $HPV_{DD} = 1.8V^{(1)(2)}$ (continued)

The following specifications apply for $V_{DD} = LSV_{DD}$, $A_V = 0\text{dB}$, $R_L = 15\mu\text{H}+8\Omega+15\mu\text{H}$ (Loudspeaker), $R_L = 32\Omega$ (Headphone), $C_{SET} = 0.1\mu\text{F}$, $f = 1\text{kHz}$, ALC off, unless otherwise specified. Limits apply for $T_A = 25^\circ\text{C}$.⁽³⁾

Symbol	Parameter	Conditions	LM49153		Units (Limits)
			Typical ⁽⁴⁾	Limits ⁽⁵⁾	
A_V	Gain	LS Mode			
		Gain 0	12		dB
		Gain 1	18		dB
		HP Mode			
		Gain 0	6	5 7	dB (min) dB (max)
		Gain 1	3		dB
		Gain 2	0		dB
		Gain 3	-1.5		dB
		Gain 4	-3		dB
		Gain 5	-6		dB
		Gain 6	-9		dB
		Gain 7	-12	-13 -11	dB (min) dB (max)
A_{VMUTE}	Mute Attention	LS Output	-80		dB
		HP Output	-98		dB
R_{IN}	Input Resistance	Analog Switch	4.5	6	Ω (max)
		MONO, R_{IN} , LIN, Inputs			
		Maximum Gain Setting	13	11 15.5	$\text{k}\Omega$ (min) $\text{k}\Omega$ (max)
		Minimum Gain Setting	110	90 130	$\text{k}\Omega$ (min) $\text{k}\Omega$ (max)
P_O	Output Power	LS Mode, $A_V = 18\text{dB}$, $R_L = 8\Omega$			
		$LSV_{DD} = 3.3V$	570		mW
		$LSV_{DD} = 3.6V$	680	620	mW (min)
		$LSV_{DD} = 4.2V$	935		mW
		$LSV_{DD} = 5.0V$	1350		mW
		HP Mode, $A_V = 6\text{dB}$			
		$R_L = 16\Omega$	25		mW
		$R_L = 32\Omega$	25	22	mW (min)
THD+N	Total Harmonic Distortion + Noise	$f = 1\text{kHz}$			
		LS Mode, $P_O = 250\text{mW}$, mono input	0.02		%
		HP Mode, $P_O = 12\text{mW}$, Stereo input	0.02		%
		EP Bypass Mode, $R_L = 32\Omega$	0.05		%
PSRR	Power Supply Rejection Ratio (Output referred)	$f = 217\text{Hz}$, $V_{RIPPLE} = 200\text{mV}_{\text{PP}}$, $C_B = 2.2\mu\text{F}$, Inputs AC GND			
		LS Mode, mono input, $A_V = 12\text{dB}$	72		dB
		LS Mode, stereo input, $A_V = 12\text{dB}$	64		dB
		HP Mode, mono input, ripple on V_{DD}	94		dB
		HP Mode, mono input, ripple on HPV_{DD}	81		dB
		HP Mode, stereo input, ripple on V_{DD}	80		dB
CMRR	Common Mode Rejection Ratio	$V_{RIPPLE} = 1\text{V}_{\text{P-P}}$, $f_{RIPPLE} = 217\text{Hz}$, mono input, $A_V = 0\text{dB}$			
		LS Mode 2	38		dB
		HP Mode 1	51		dB
η	Efficiency	LS Mode, THD+N = 1%	88		%
X_{TALK}	Crosstalk	$P_O = 12\text{mW}$, $f = 1\text{kHz}$	80		dB

Electrical Characteristics $V_{DD} = 3.6V$, $HPV_{DD} = 1.8V^{(1)(2)}$ (continued)

The following specifications apply for $V_{DD} = LSV_{DD}$, $A_V = 0dB$, $R_L = 15\mu H + 8\Omega + 15\mu H$ (Loudspeaker), $R_L = 32\Omega$ (Headphone), $C_{SET} = 0.1\mu F$, $f = 1kHz$, ALC off, unless otherwise specified. Limits apply for $T_A = 25^\circ C$.⁽³⁾

Symbol	Parameter	Conditions	LM49153		Units (Limits)
			Typical ⁽⁴⁾	Limits ⁽⁵⁾	
ϵ_{OS}	Output Noise	A-weighted, Inputs AC GND			
		LS Mode, mono input	46		μV
		LS Mode, stereo input	52		μV
		HP Mode, mono input	11		μV
		HP Mode, stereo input	11		μV
SNR	Signal to Noise Ratio	LS Mode, $P_O = 680mW$, A-weighted, Mono HP Mode, $P_O = 25mW$, A-weighted	94 98		dB dB
t_A	Noise Gate Attack Time	$I^2C = 1$ $I^2C = 0$	0.1 0.9		ms ms
t_R	Noise Gate Release Time	$I^2C = 0$ $I^2C = 1$	1.2 2.1		s s
CC	Clip Control	Low 010 Medium 011 High 100	7.3 7.8 8.1		V_{P-P} V_{P-P} V_{P-P}
P_{LIMIT}	Output Power Limit	LS Mode 1, THD+N $\leq 1\%$, Voltage Level ⁽⁶⁾ 001 010 011 100 101 110	4 4.8 5.6 6.4 7.2 8.0		V_{P-P} V_{P-P} V_{P-P} V_{P-P} V_{P-P} V_{P-P}
t_A	ALC Attack Time		0.5		ms
t_R	ALC Release Time		200		ms

(6) The LM49153 ALC limits the output power to which ever is lower, the supply voltage or output power limit.

I^2C Interface Characteristics $V_{DD} = 3.6V^{(1)(2)}$

The following specifications apply for $A_V = 0dB$, $R_L = 8\Omega$, $f = 1kHz$, unless otherwise specified. Limits apply for $T_A = 25^\circ C$.

Symbol	Parameter	Conditions	LM49153		Units (Limits)
			Typical (3)	Limits (4)	
t_1	SCL Period			2.5	μs (min)
t_2	SDA Setup Time			250	ns (min)
t_3	SDA Stable Time			0	ns (min)
t_4	Start Condition Time			250	ns (min)
t_5	Stop Condition Time			250	ns (min)
V_{IH}	Input High Voltage			1.2	V (min)
V_{IL}	Input Low Voltage			0.6	V (max)

- (1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
- (2) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.
- (3) Typical values represent most likely parametric norms at $T_A = +25^\circ C$, and at the *Recommended Operation Conditions* at the time of product characterization and are not specified.
- (4) Datasheet min/max specification limits are specified by test or statistical analysis.

Typical Performance Characteristics⁽¹⁾

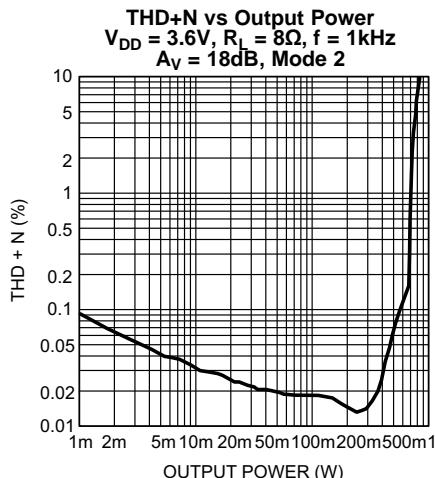


Figure 3.

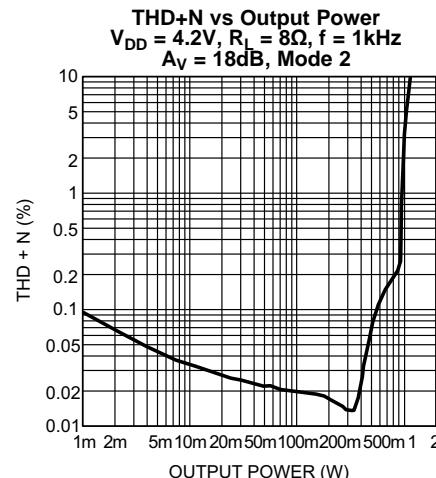


Figure 4.

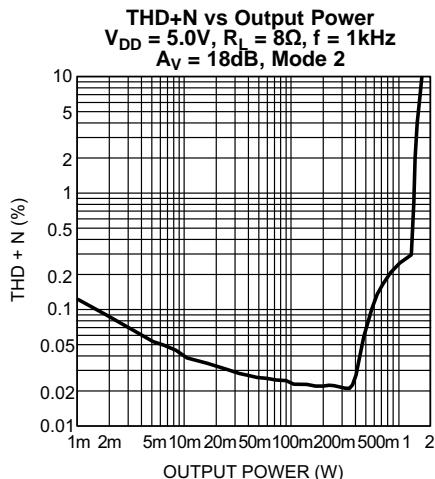


Figure 5.

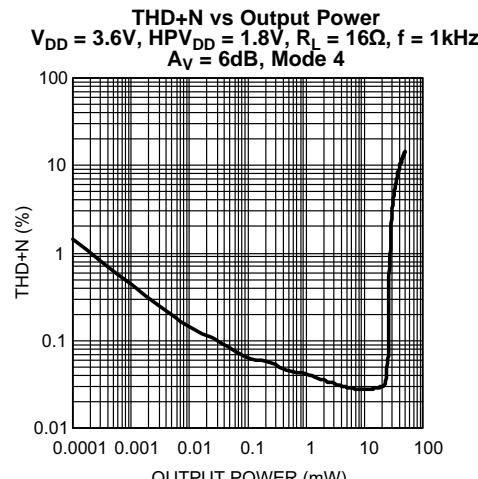


Figure 6.

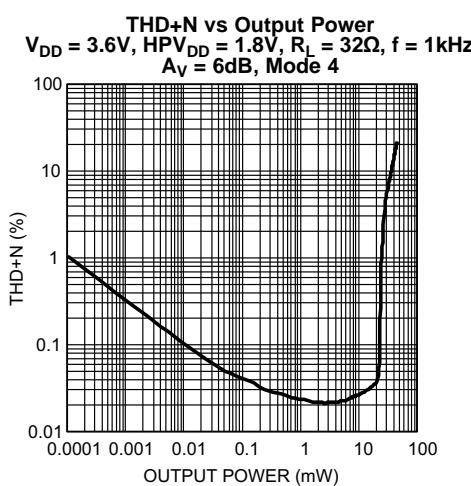


Figure 7.

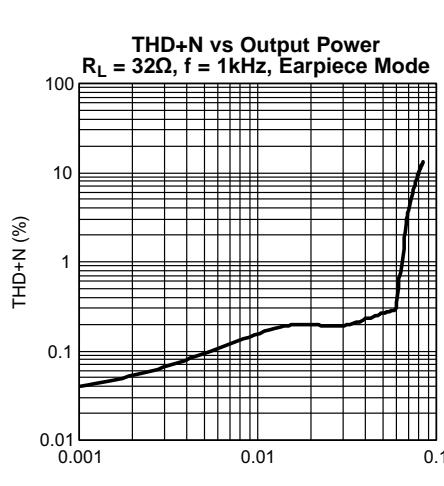
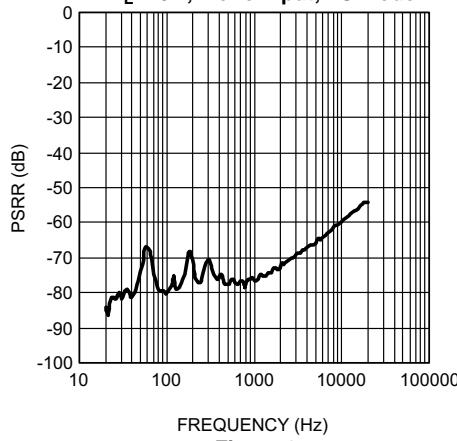


Figure 8.

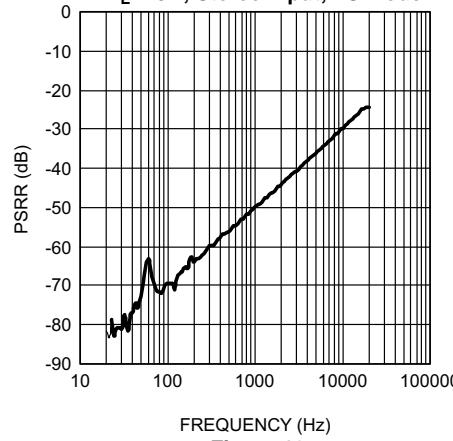
(1) Loudspeaker R_L is a resistive load in series with two inductors to simulate an actual speaker load. For $R_L = 8\Omega$, the load is $15\mu\text{H} + 8\Omega$, $+15\mu\text{H}$. For $R_L = 4\Omega$, the load is $15\mu\text{H} + 4\Omega + 15\mu\text{H}$.

Typical Performance Characteristics⁽¹⁾ (continued)

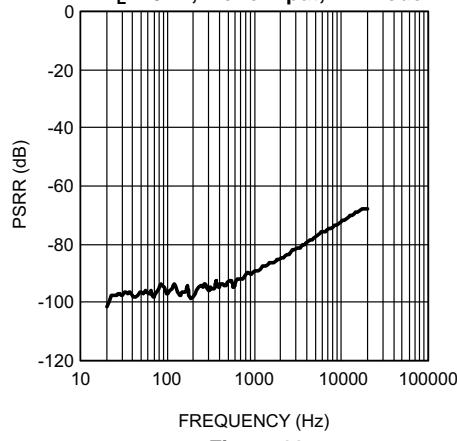
PSRR vs FREQUENCY
 $V_{DD} = 3.6V$, $HPV_{DD} = 1.8V$, $V_{DD\text{-RIPPLE}} = 200mV_{P\text{-P}}$
 $R_L = 8\Omega$, Mono Input, LS Mode


Figure 9.

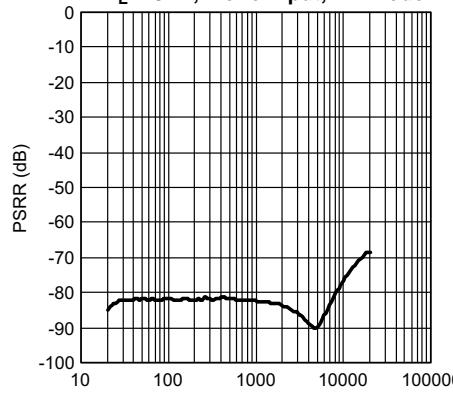
PSRR vs FREQUENCY
 $V_{DD} = 3.6V$, $HPV_{DD} = 1.8V$, $V_{DD\text{-RIPPLE}} = 200mV_{P\text{-P}}$
 $R_L = 8\Omega$, Stereo Input, LS Mode


Figure 10.

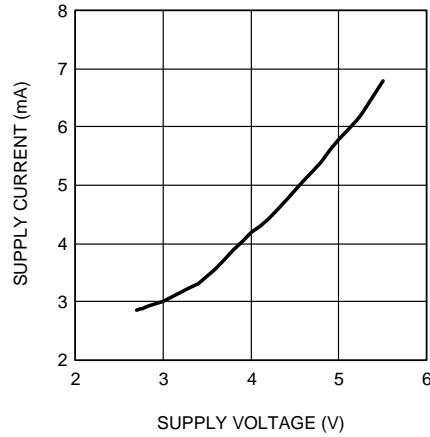
PSRR vs FREQUENCY
 $V_{DD} = 3.6V$, $HPV_{DD} = 1.8V$, $V_{DD\text{-RIPPLE}} = 200mV_{P\text{-P}}$
 $R_L = 32\Omega$, Mono Input, HP Mode


Figure 11.

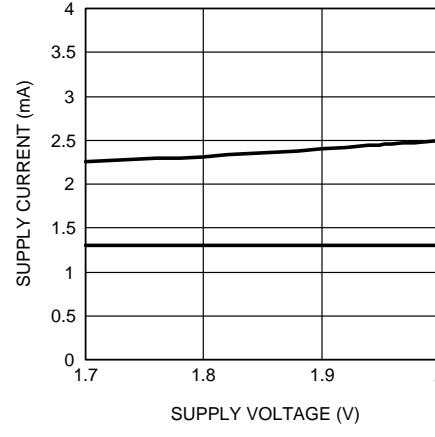
PSRR vs FREQUENCY
 $V_{DD} = 3.6V$, $HPV_{DD} = 1.8V$, $HPV_{DD\text{-RIPPLE}} = 200mV_{P\text{-P}}$
 $R_L = 32\Omega$, Mono Input, HP Mode


Figure 12.

SUPPLY CURRENT vs SUPPLY VOLTAGE
No Load, Loudspeaker Mode 2


Figure 13.

SUPPLY CURRENT vs SUPPLY VOLTAGE
No Load, Loudspeaker Mode 4


Figure 14.

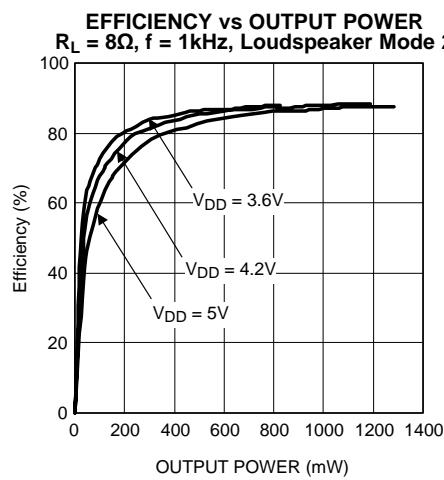
Typical Performance Characteristics⁽¹⁾ (continued)


Figure 15.

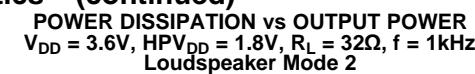


Figure 16.

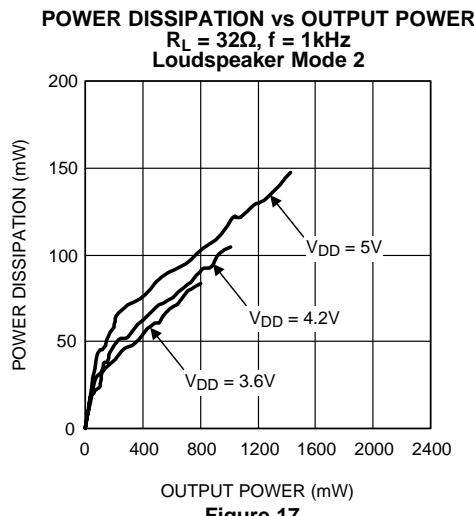


Figure 17.

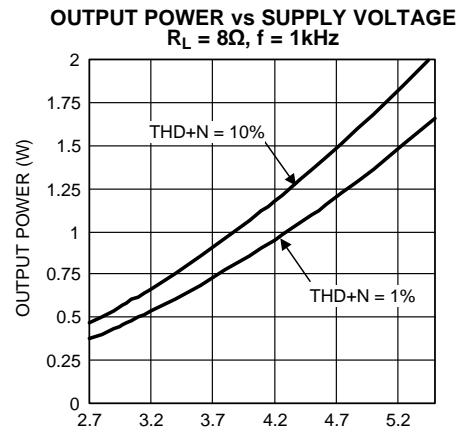


Figure 18.

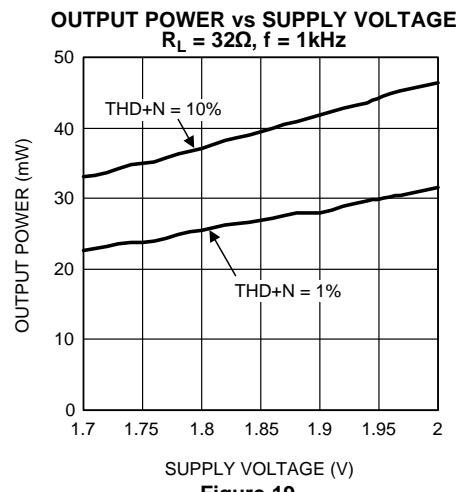


Figure 19.

APPLICATION INFORMATION

WRITE-ONLY I²C COMPATIBLE INTERFACE

The LM49153 is controlled through an I²C compatible serial interface that consists of a serial data line (SDA) and a serial clock (SCL). The clock line is uni-directional. The data line is bi-directional (open drain). The LM49153 and the master can communicate at clock rates up to 400kHz. [Figure 20](#) shows the I²C interface timing diagram. Data on the SDA line must be stable during the HIGH period of SCL. The LM49153 is a transmit/receive slave-only device, reliant upon the master to generate the SCL signal. Each transmission sequence is framed by a START condition and a STOP condition ([Figure 21](#)). Each data word, device address and data, transmitted over the bus is 8 bits long and is always followed by an acknowledge pulse. The LM49153 device address is 1100000.

I²C BUS FORMAT

The I²C bus format is shown in [Figure 21](#). The START signal, the transition of SDA from HIGH to LOW while SCL is HIGH, is generated, alerting all devices on the bus that a device address is being written to the bus.

The 7-bit device address is written to the bus, most significant bit (MSB) first, followed by the R/W bit. R/W = 0 indicates the master is writing to the slave device, R/W = 1 indicates the master wants to read data from the slave device. Set R/W = 0; the LM49153 is a WRITE-ONLY device and will not respond the R/W = 1. The data is latched in on the rising edge of the clock. Each address bit must be stable while SCL is HIGH. After the last address bit is transmitted, the master device releases SDA, during which time, an acknowledge clock pulse is generated by the slave device. If the LM49153 receives the correct address, the device pulls the SDA line low, generating an acknowledge bit (ACK).

Once the master device registers the ACK bit, the 8-bit register data word is sent. Each data bit should be stable while SCL is HIGH. After the 8-bit register data word is sent, the LM49153 sends another ACK bit. Following the acknowledgement of the register data word, the master issues a STOP bit, allowing SDA to go high.

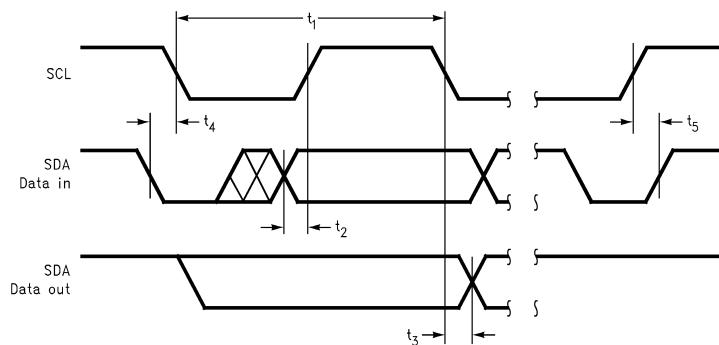


Figure 20. I²C Timing Diagram

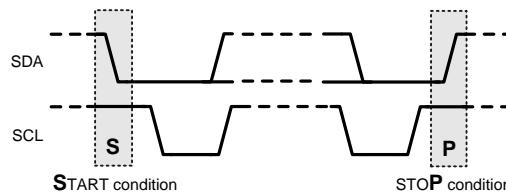


Figure 21. Example I²C Write Cycle

DEVICE ADDRESS REGISTER

Table 1. Device Address

	B7	B6	B5	B4	B3	B2	B1	B0 (W)
Device Address	1	1	1	1	1	0	0	0

I²C CONTROL REGISTER

Table 2. I²C Control

Register Name	B7	B6	B5	B4	B3	B2	B1	B0
Shutdown control	0	0	0	1	GAMP_ON	HPR_SD	ClassG_SD	PWR_ON
Mode control	0	0	1	EP			MODE_CONTROL	
Power limiter control	0	1	0	ATTACK_TIME			POWER_LEVEL	
No clip control	0	1	1	RELEASE_TIME			OUTPUT_CLIP_CONTROL	
Gain control	1	0	0	0	LSGAIN		HP_GAIN	
Volume control	1	0	1		LS_VOLUME/HP_VOLUME			
LS control	1	1	0	0	NOISE_GATE_LEVEL		NOISE_GATE_TIME	
Other control	1	1	1	0	0	0	0	0
Class-G control	1	1	1	0	1	0	CLASS_G_TRIP_LEVEL	
Other control	1	1	1	1	0	0	SS_EN	TURN_ON TIME

SHUTDOWN CONTROL REGISTER

Table 3. Shutdown Control

Bit	Name	Value	Description
B0	PWR_ON	This enables or disables the device.	
		0	Device disabled
		1	Device enabled
B1	Class G_SD	This enables or disables the Class G of the headphone.	
		0	Class G enabled
		1	Class G disabled
B2	HPR_SD	This disables the right headphone output.	
		0	Normal Operation
		1	Right headphone disabled
B3	GAMP_ON	This disables the gain amplifiers that are not in use to minimize I _{DD} .	
		0	Normal Operation
		1	Disable unused gain amplifiers

MODE CONTROL REGISTER

Table 4. Mode Control

Bits	Field	Description								
B3:B0	MODE_CONTROL	This set the different mixer output modes.								
		Mode	Input (Diff/SE) ⁽¹⁾	Input ⁽²⁾	SPK	HP	LS	HP(L)	HP (R)	
		0	0	X	0	0	SD	SD	SD	
		1	0	X	0	1	SD	GM X M	GM X M	
		2	0	X	0	1	GM ⁽³⁾ X M ⁽⁴⁾	SD	SD	
		3	0	X	1	1	GM X M	GM X M	GM X M	
		4	1	0	0	1	SD	GST X L1	GST X R1	
		5	1	0	1	0	GST ⁽⁵⁾ X (L1 + R1) ⁽⁶⁾⁽⁷⁾	SD	SD	
		6	1	0	1	1	GST X (L1 + R1)	GST X L1	GST X R1	
		7	1	1	0	1	SD ⁽⁸⁾	GST X L2	GST X R2	
		8	1	1	1	0	GST X (L2 + R2) ⁽⁶⁾⁽⁷⁾	SD	SD	
		9	1	1	1	1	GST X (L2 + R2)	GST X L2	GST X R2	
B4	EP	This enables the receiver bypass path.								
		0	Normal output mode operation							
		1	Enable the receiver bypass path							

(1) 0: Differential, 1: Single-Ended

(2) 0: Stereo 1CH, 1: Stereo 2CH

(3) G_M : Differential input gain path

(4) M: Mono differential input

(5) G_{ST} : Single-Ended input path

(6) R1/R2: Right channel stereo input

(7) L1/L2: Left channel stereo input

(8) SD: Shutdown

VOLTAGE LIMIT CONTROL REGISTER

Table 5. Shutdown Control

Bits	Field	Description	
B2:B0	VOLTAGE LEVEL	This sets the output voltage limit level.	
		000	Voltage limit disabled
		001	$V_{TH(VLIM)} = 4.0V_{P-P}$
		010	$V_{TH(VLIM)} = 4.8V_{P-P}$
		011	$V_{TH(VLIM)} = 5.6V_{P-P}$
		100	$V_{TH(VLIM)} = 6.4V_{P-P}$
		101	$V_{TH(VLIM)} = 7.2V_{P-P}$
		110	$V_{TH(VLIM)} = 8.0V_{P-P}$
		111	Voltage limit disabled
B4:B3	ATTACK_TIME	This sets the attack time of the automatic limiter control circuit based on $C_{SET} = 0.1\mu F$.	
		00	0.7ms
		01	0.975ms
		10	1.5ms
		11	2.025ms

NO CLIP CONTROL REGISTER

Table 6. No Clip Control

Bits	Field	Description	
B2:B0	OUTPUT_CLIP_CONTROL	This sets the output voltage limit level.	
		000	No Clip disabled, output clip control disabled
		010	No Clip enabled, output clip control disabled
		011	Low
		100	Med
		101	High
B4:B3	RELEASE_TIME	This sets the release time of the automatic limiter control circuit.	
		00	1s
		01	0.8s
		10	0.65s
		11	0.4s

GAIN CONTROL REGISTER

Table 7. Gain Control

Bits	Field	Description	
B2:B0	HP_GAIN	This sets the headphone output gain level.	
		000	0dB
		001	-1.5dB
		010	-3dB
		011	-6dB
		100	-9dB
		101	-12dB
		110	-15dB
B3	LS_GAIN	This sets the loudspeaker output gain level.	
		0	12dB
		1	18dB

VOLUME CONTROL REGISTER

Table 8. Volume Control

VOLUME STEP	_G4	_G3	_G2	_G1	_G0	Stereo GAIN (dB)	Mono GAIN (dB)
1	0	0	0	0	0	-109	-115
2	0	0	0	0	1	-46.5	-52.5
3	0	0	0	1	0	-40.5	-46.5
4	0	0	0	1	1	-34.5	-40.5
5	0	0	1	0	0	-30	-36
6	0	0	1	0	1	-27	-33
7	0	0	1	1	0	-24	-30
8	0	0	1	1	1	-21	-27
9	0	1	0	0	0	-18	-24
10	0	1	0	0	1	-15	-21
11	0	1	0	1	0	-13.5	-19.5
12	0	1	0	1	1	-12	-18

Table 8. Volume Control (continued)

VOLUME STEP	_G4	_G3	_G2	_G1	_G0	Stereo GAIN (dB)	Mono GAIN (dB)
13	0	1	1	0	0	-10.5	-16.5
14	0	1	1	0	1	-9	-15
15	0	1	1	1	0	-7.5	-13.5
16	0	1	1	1	1	-6	-12
17	1	0	0	0	0	-4.5	-10.5
18	1	0	0	0	1	-3	-9
19	1	0	0	1	0	-1.5	-7.5
20	1	0	0	1	1	0	-6
21	1	0	1	0	0	1.5	-4.5
22	1	0	1	0	1	3	-3
23	1	0	1	1	0	4.5	-1.5
24	1	0	1	1	1	6	0
25	1	1	0	0	0	7.5	1.5
26	1	1	0	0	1	9	3
27	1	1	0	1	0	10.5	4.5
28	1	1	0	1	1	12	6
29	1	1	1	0	0	13.5	7.5
30	1	1	1	0	1	15	9
31	1	1	1	1	0	16.5	10.5
32	1	1	1	1	1	18	12

NOISE GATE CONTROL REGISTER

Table 9. Noise Gate Control

Bits	Field	Description		
B1:B0	NOISE_GATE_TIME	This sets the noise gate attack and release time.		
		00	0.9ms	1.2s
		01	0.9ms	2.1s
		10	0.1ms	1.2s
		11	0.1ms	2.1s
B4:B3	NOISE_GATE_LEVEL	This sets the noise gate trip level *		
		000	Noise gate disabled	
		010	Low — 26mV _{RMS}	
		011	Medium — 40mV _{RMS}	
		100	High — 60mV _{RMS}	

CLASS-G CONTROL REGISTER

Table 10. Class-G Control

B4:B3	CLASS_G_TRIP_LEVEL	This sets the Class G trip level and determines when the headphone rails switches.		
		00	Highest Level Trip Point (Default)	
		01	High Level Trip Point	
		10	Medium Level Trip Point	
		11	Low Level Trip Point	

OTHER CONTROL REGISTER

Table 11. Other Control

B0	TURN_ON_TIME	This sets the turn on time.	
		0	Normal Turn On Time
B1	SS_EN	This enables Spread Spectrum.	
		0	Spread Spectrum Disabled
		1	Spread Spectrum Enabled

DIFFERENTIAL AMPLIFIER EXPLANATION

The LM49153 features a differential input stage for the mono inputs, which offers improved noise rejection compared to a single-ended input amplifier. Because a differential input amplifier amplifies the difference between the two input signals, any component common to both signals is cancelled. An additional benefit of the differential input structure is the possible elimination of the DC input blocking capacitors. Since the DC component is common to both inputs, and thus cancelled by the amplifier, the LM49153 can be used without input coupling capacitors when configured with a differential input signal.

INPUT MIXER/MULTIPLEXER

The LM49153 includes a comprehensive mixer multiplexer controlled through the I²C interface. The mixer/multiplexer allows any input combination to appear on any output of LM49153. Multiple input paths can be selected simultaneously. Under these conditions, the selected inputs are mixed together and output on the selected channel. [Table 4 \(MODE CONTROL\)](#) shows how the input signals are mixed together for each possible input selection.

SHUTDOWN FUNCTION

The LM49153 features the following shutdown controls: Bit B4 (GAMP_ON) of the SHUTDOWN CONTROL register controls the gain amplifiers. When GAMP_SD = 1, it disables the gain amplifiers that are not in use. For example, in Modes 1, 4 and 5, the Mono inputs are in use, so the Left and Right input gain amplifiers are disabled, causing the I_{DD} to be minimized. Bit B0 (PWR_ON) of the SHUTDOWN CONTROL register is the global shutdown control for the entire device. Set PWR_ON = 0 for normal operation. PWR_ON = 1 overrides any other shutdown control bit.

CLASS D AMPLIFIER

The LM49153 features a mono class D audio power amplifier with a filterless modulation scheme that reduces external component count, conserving board space and reducing system cost. With no signal applied, the outputs (LSOUT+ and LSOUT-) switch between VDD and GND with 50% duty cycle, in phase, causing the two outputs to cancel. This cancellation results in no net voltage across the speaker, thus there is no current to the load in the idle state.

With an input signal applied, the duty cycle (pulse width) of the class D output changes. For increasing output voltage, the duty cycle of LSOUT+ increases, while the duty cycle of LSOUT- decreases. For decreasing output voltages, the converse occurs. The difference between the two pulse widths yields the differential output voltage.

ENHANCED EMISSION SUPPRESSION (E²S)

The LM49153 class D amplifier features Texas Instruments' patent-pending E²S system that reduces EMI, while maintaining high quality audio reproduction and efficiency. The E²S system features selectable spread spectrum and advanced edge rate control (ERC). The LM49153 class D ERC greatly reduces the high frequency components of the output square waves by controlling the output rise and fall times, slowing the transitions to reduce RF emissions, while maximizing THD+N and efficiency performance.

SPREAD SPECTRUM

The selectable spread spectrum mode minimizes the need for output filters, ferrite beads or chokes. In spread spectrum mode, the switching frequency varies randomly by 30% about a 300kHz center frequency, reducing the wideband spectral content, improving EMI emission radiated by the speaker and associated cables and traces. Where a fixed frequency class D exhibits large amounts of spectral energy at multiples of the switching frequency, the spread spectrum architecture spreads that energy over a larger bandwidth. The cycle-to-cycle variation of the switching period does not affect the audio reproduction, efficiency, or PSRR. Set bit B0 (SS_EN) of the SS CONTROL register to 1 to enable spread spectrum mode.

GROUND REFERENCE HEADPHONE AMPLIFIER

The LM49153 features a low noise inverting charge pump that generates an internal negative supply voltage. This allows the headphone outputs to be biased about GND instead of a nominal DC voltage, like traditional headphone amplifiers. Because there is no DC component, the large DC blocking capacitors (typically 220 μ F) are not necessary. The coupling capacitors are replaced by two small ceramic charge pump capacitors, saving board space and cost. Eliminating the output coupling capacitors also improves low frequency response. In traditional headphone amplifiers, the headphone impedance and the output capacitor from a high-pass filter that not only blocks the DC component of the output, but also attenuates low frequencies, impacting the bass response. Because the LM49153 does not require the output coupling capacitors, the low frequency response of the device is not degraded by external components. In addition to eliminating the output coupling capacitors, the ground referenced output nearly doubles the available dynamic range of the LM49153 headphone amplifiers when compared to a traditional headphone amplifier operating from the same supply voltage.

EARPIECE (EP) BYPASS

When B4 of MODE_CONTROL register is set to 1, earpiece amplifier is enabled and differential inputs are passed down to speaker outputs. This in turn disables the class D amplifier.

AUTOMATIC LIMITER CONTROL (ALC)

When enabled, the ALC continuously monitors and adjusts the gain of the loudspeaker amplifier signal path if necessary. The ALC serves two functions: voltage limiter/speaker protection and output clip prevention (No-Clip) with three clip controls levels. The voltage limiter/speaker protection prevents an output overload condition by maintaining the loudspeaker output signal below a preset amplitude (See [VOLTAGE LIMITER](#) section). The No Clip feature monitors the output signal and maintains audio quality by preventing the loudspeaker output from exceeding the amplifier's headroom (see [NO CLIP/OUTPUT CLIP CONTROL](#) section). The voltage limiter thresholds, clip control levels, attack and release times are configured through the I²C interface.

VOLTAGE LIMITER

The voltage limiter function of the ALC monitors and prevents the audio signal from exceeding the voltage limit threshold ([Figure 22](#)). The voltage limit threshold ($V_{TH(VLIM)}$) is set by bits B2:B0 in the Voltage Limit Threshold Register (see [Table 5](#)). Although the ALC reduces the gain of the speaker path to maintain the audio signal below the voltage limit threshold, it is still possible to overdrive the speaker output in which case loudspeaker output will exceed the voltage limit threshold and cause clipping on the output, and speaker damage is possible. Please see the [ALC HEADROOM](#) section for further details.

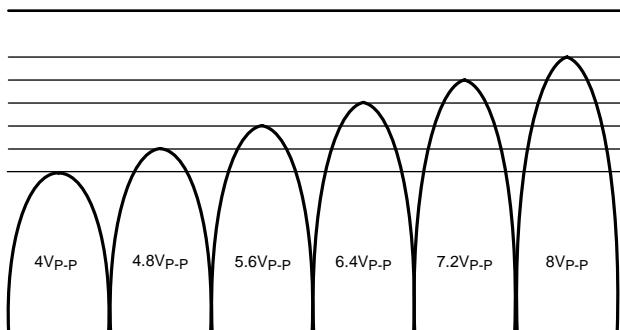


Figure 22. Voltage Limit Output Level

NO CLIP/OUTPUT CLIP CONTROL

The LM49153 No Clip circuitry detects when the loudspeaker output is near clipping and reduces the signal gain to prevent output clipping and preserve audio quality (Figure 23). Although the ALC reduces the gain of the speaker path to prevent output clipping, it is still possible to overdrive the speaker output. Please see the [ALC HEADROOM](#) section for further details.

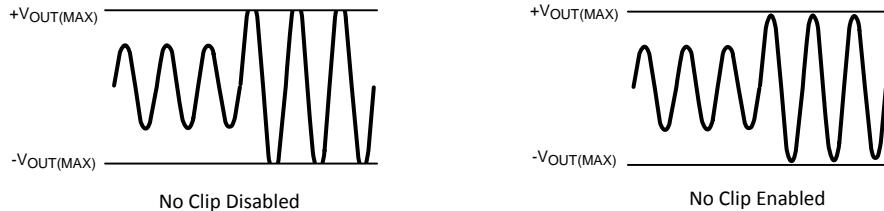


Figure 23. No Clip Function

The LM49153 also features an output clip control that allows a certain amount of clipping at the output in order to increase the loudspeaker output power. The clip level is set by B2:B0 in the No Clip Control Register (see [Table 6](#)). The clip control works by allowing the output to enter clipping before the ALC turns on and maintains the output level. The clip control has three levels: low, medium, and high. The low and high clip level control settings give the lowest distortion and highest distortion respectively on the output (see [SHUTDOWN FUNCTION](#)). The actual output level of the device will depend upon the supply voltage, and the output power will depend upon the load impedance.

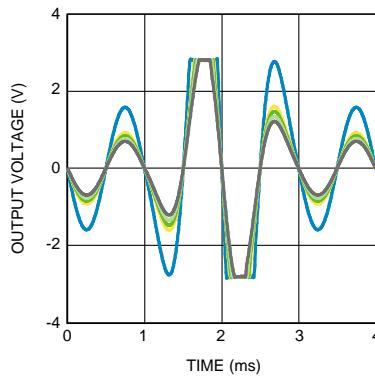


Figure 24. Clip Control Levels

ALC HEADROOM

When either voltage limiter or no clip is enabled, it is still possible to drive LM49153 into clipping by overdriving the input volume stage of the signal path beyond its output dynamic range. In this case, clipping occurs at the input volume stage, and although ALC is active, the gain reduction will have no effect on the output clipping. The maximum input that can safely pass through the input volume stage can be calculated by following formula:

$$V_{IN} \leq \frac{V_{DD}}{Av \text{ (volume gain)}} \quad (1)$$

So in the case of 0 dB volume gain, audio input has to be less than V_{DD} for both voltage limiter or No clip settings.

When voltage limiter is enabled, ALC can reach its max attenuation for lower voltage limit levels as shown in the [Figure 26](#). Typically, after the ALC started working, with 6dB of audio input change ALC is well within its regulation. Voltage limiter Input headroom can be increased by switching to the LS_GAIN to 18dB in the Gain Control Register (see [Table 7](#)).

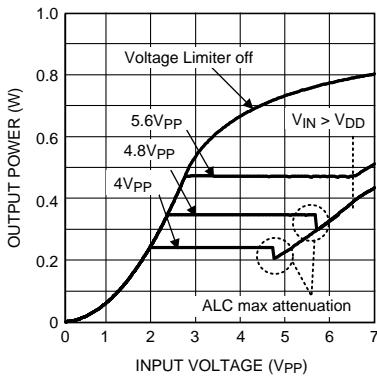


Figure 25. Voltage Limiter Function
 $V_{DD} = 3.3V$, $R_L = 8\Omega + 30\mu H$
 $f_{IN} = 1kHz$, $LS_GAIN = 0$

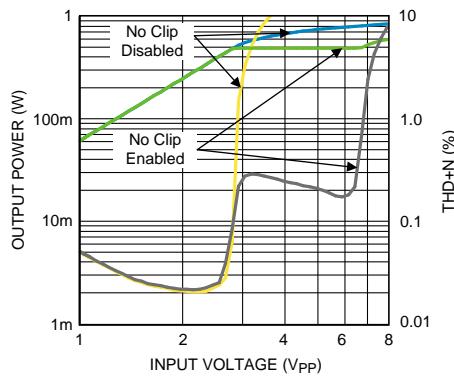


Figure 26. No Clip Function
 $V_{DD} = 3.3V$, $R_L = 8\Omega + 30\mu H$
 $f_{IN} = 1kHz$, $LS_GAIN = 0$
Gray, Yellow = THD+N vs Input Voltage

When No Clip is enabled, class D speaker output reduces when it's about to enter clipping region and power stay constant as long as V_{IN} is less than V_{DD} for 0dB volume gain (see Figure 26). For example, in the case of $V_{DD} = 3.3V$, there is a 6dB of headroom for the change in input. Please see the ALC typical performance curves for additional plots relating to different supply voltages and LS_GAIN settings for specific application parameters.

ATTACK TIME

Attack time (t_{ATK}) is the time it takes for the gain to be reduced by 6dB ($LS_GAIN = 0$) once the audio signal exceeds the ALC threshold. Fast attack times allow the ALC to react quickly and prevent transients such as symbol crashes from being distorted. However, fast attack times can lead to volume pumping, where the gain reduction and release becomes noticeable, as the ALC cycles quickly. Slower attack times cause the ALC to ignore the fast transients, and instead act upon longer, louder passages. Selecting an attack time that is too slow can lead to increased distortion in the case of the No Clip function, and possible output overload conditions in the case of the Voltage limiter. The attack time is set by a combination of the value of C_{SET} and the attack time coefficient as given by Equation 2:

$$t_{ATK} = 20k\Omega C_{SET} / \alpha_{ATK} \quad (2)$$

Where α_{ATK} is the attack time coefficient (Table 12) set by bits B4:B3 in the Voltage Limit Control Register (see Table 5). The attack time coefficient allows the user to set a nominal attack time. The internal 20k Ω resistor is subject to temperature change, and it has tolerance between -11% to +20%.

Table 12. Attack Time Coefficient

B5	B4	α_{ATK}
0	0	2.667
0	1	2
1	0	1.333
1	1	1

RELEASE TIME

Release time (t_{RL}) is the time it takes for the gain to return from 6dB (LS_GAIN = 0) to its normal level once the audio signal returns below the ALC threshold. A fast release time allows the ALC to react quickly to transients, preserving the original dynamics of the audio source. However, similar to a fast attack time, a fast release time contributes to volume pumping. A slow release time reduces the effect of volume pumping. The release time is set by a combination of the value of C_{SET} and release time coefficient as given by [Equation 3](#):

$$t_{RL} = 20M\Omega C_{SET} / \alpha_{RL} \text{ (s)} \quad (3)$$

where α_{RL} is the release time coefficient ([Table 13](#)) set by bits B4:B3 in the No Clip Control Register. The release time coefficient allows the user to set a nominal release time. The internal 20MΩ is subject to temperature change, and it has tolerance between -11% to +20%.

Table 13. Release Time Coefficient

B5	B4	α_{RL}
0	0	2
0	1	2.5
1	0	3
1	1	5

PROPER SELECTION OF EXTERNAL COMPONENTS

ALC Timing (C_{SET}) Capacitor Selection

The recommended range value of C_{SET} is between .01μF to 1μF. Lowering the value below .01μF can increase the attack time but LM49153 ALC ability to regulate its output can be disrupted and approaches the hard limiter circuit. This in turn increases the THD+N and audio quality will be severely affected.

Charge Pump Capacitor Selection

Use low ESR ceramic capacitors (less than 100mΩ) for optimum performance.

Charge Pump Flying Capacitor (C1)

The flying capacitor (C1) affects the load regulation and output impedance of the charge pump. A C1 value that is too low results in a loss of current drive, leading to a loss of amplifier headroom. A higher valued C1 improves load regulation and lowers charge pump output impedance to an extent. Above 2.2μF, the $R_{DS(ON)}$ of the charge pump switches and the ESR of C1 and C2 dominate the output impedance. A lower value capacitor can be used in systems with low maximum output power requirements.

Charge Pump Hold Capacitor (C2)

The value and ESR of the hold capacitor (C2) directly affects the ripple on CPV_{SS} . Increasing the value of C2 reduces output ripple. Decreasing the ESR of C2 reduces both output ripple and charge pump output impedance. A lower value capacitor can be used in systems with low maximum output power requirements.

Input Capacitor Selection

Input capacitors may be required for some applications, or when the audio source is single-ended. Input capacitors block the DC component of the audio signal, eliminating any conflict between the DC component of the audio source and the bias voltage of the LM49153. The input capacitors create a high-pass filter with the input resistors R_{IN} . The -3dB point of the high-pass filter is found using [Equation 4](#) below.

$$f = 1 / 2\pi R_{IN} C_{IN} \text{ (Hz)} \quad (4)$$

Where the value of R_{IN} is given in the Electrical Characteristics Table.

High-pass filtering the audio signal helps protect the speakers. When the LM49153 is using a single-ended source, power supply noise on the ground is seen as an input signal. Setting the high-pass filter point above the power supply noise frequencies, 217Hz in a GSM phone, for example, filters out the noise such that it is not amplified and heard on the output. Capacitors with a tolerance of 10% or better are recommended for impedance matching and improved CMRR and PSRR.

DEMO BOARD GUIDELINES

Introduction

The LM49153 demoboard is shown in Figure TBD.

Quick Start Guide:

1. Connect the one end of the USB cable to the PC that will be used to control the demo board and the other end to J1 of the LM49153 demo board.
2. Install the LM49153 I²C interface software.
3. Apply 2.7V to 5.5V to the header labeled V_{DD} and apply a ground connection to the header labeled GND above C5.
4. Apply 1.7V to 2.0V to the header labeled HPV_{DD} and apply a ground connection to the header labeled GND7.
5. Apply a mono differential signal or two single-ended signal to headers labeled INM-/INR1 and INM+/INL1. Then, apply a single-ended signal to headers labeled INL2 and INR2.
6.
 - (a) For class D speaker output, connect a speaker or load ($\geq 4\Omega$) to LSOUT- and LSOUT+ header pins (a low pass filter may be required for measurements).
 - (b) For headphone output, connect either through headphone output jack or HPR and HPL header pins.
7. Run the LM49153 I²C interface software, select desired mode, set 0dB volume gain, and Power on options from the GUI.

Board Features

The LM49153 demonstration board has all of the necessary connections, using 100mil headers, to apply the power supply voltage and the audio input signals. The Class D amplifier's output is available on 100mil headers. The Class AB headphone's amplified audio signal is available on both a stereo headphone jack and 100 mil headers. The input and output of the earpiece analog switch are also available on 100mil headers. On-board I²C signal generation microcontroller allows for a convenient connection via USB jack.

Connections

Headers/Jumpers Description	Function/Use
V_{DD} and GND	Power supply connection. Connect an external power supply's positive voltage source to V_{DD} and the supply's ground source to GND header pins respectively.
HPV_{DD} and GND7	Headphone power supply connection. Connect an external power supply's positive voltage source to HPV_{DD} and the supply's ground source to GND7 header pins respectively.
INM+/INL1 and INM-/INR1	These header pins provide a connection to a mono differential or stereo left and right single-ended input.
INL2 and INR2	These header pins provide a connection to stereo left and right single-ended input.
EP+ and EP-	These header pins provide a connection to the input of the earpiece bypass switch.
LSOUT- and LSOUT+	These header pins provide a connection to Class D loudspeaker outputs. Apply a load greater than 4Ω . A low pass filter may be required for measurements.
HPL and HPR	These header pins provide a connection to headphone outputs. Apply a load greater than 16Ω .
J1	J1 provides a USB connection to control the LM49153.
JU1	Stereo headphone jack

Power Supply Sequencing

The LM49153 uses two power supply voltages, V_{DD} for the Class D and HPV_{DD} for the Headphones. If using two separate power supplies, apply V_{DD} first before applying HPV_{DD} to ensure proper operation.

I²C Interface GUI Software

The LM49153 demo board has the I²C signal generation microcontroller integrated and will generate the address byte and the data byte when used with the LM49153 GUI software (see [Figure 27](#)).

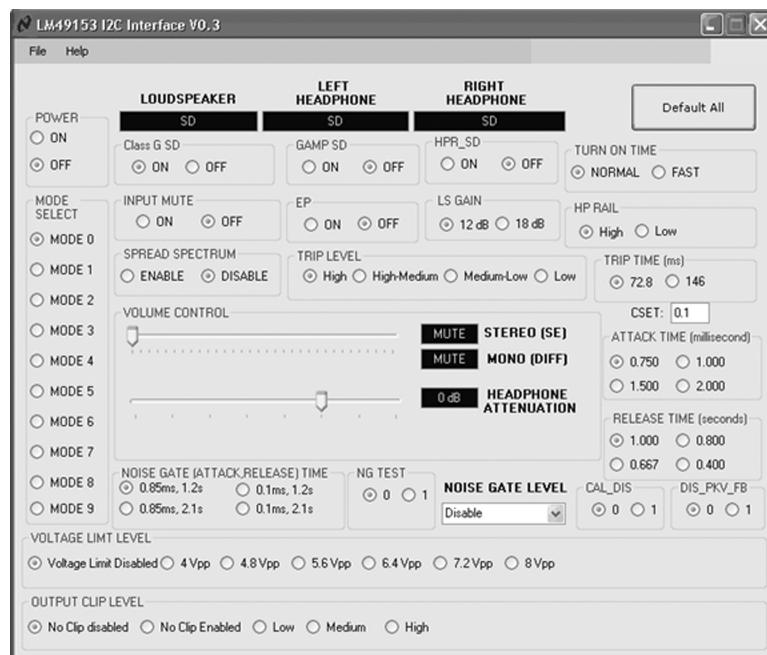


Figure 27. GUI Software

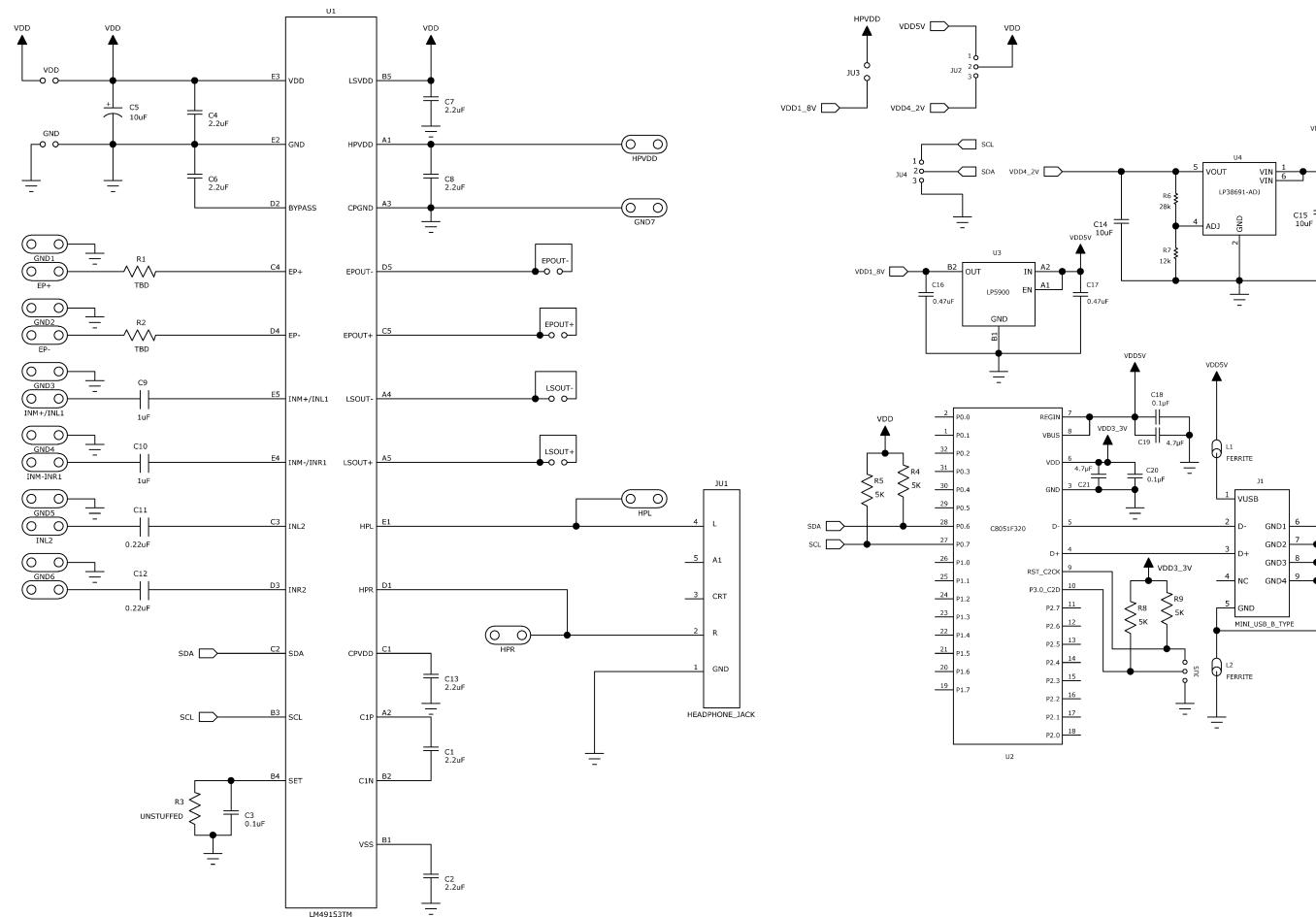
Software Installation Instructions

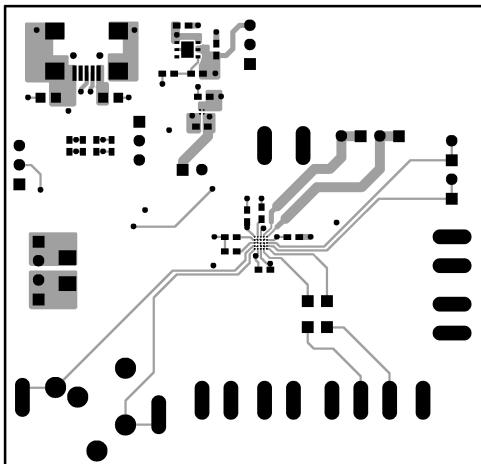
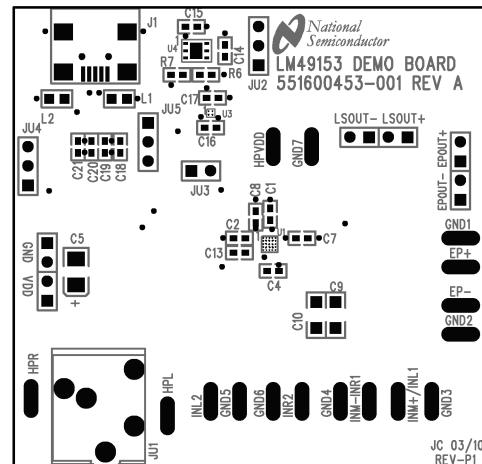
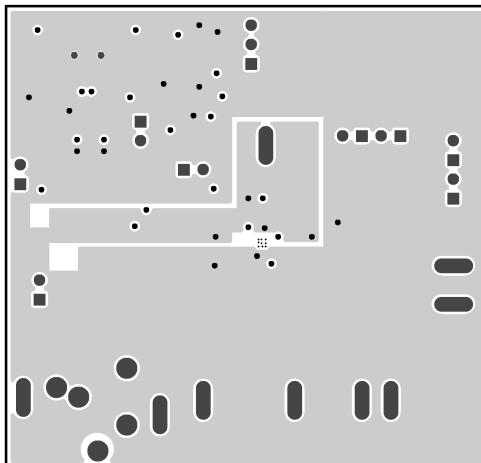
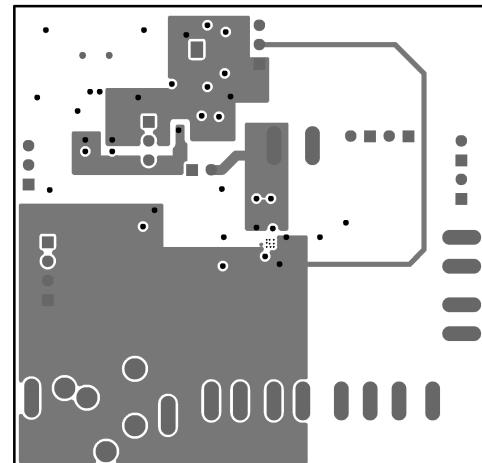
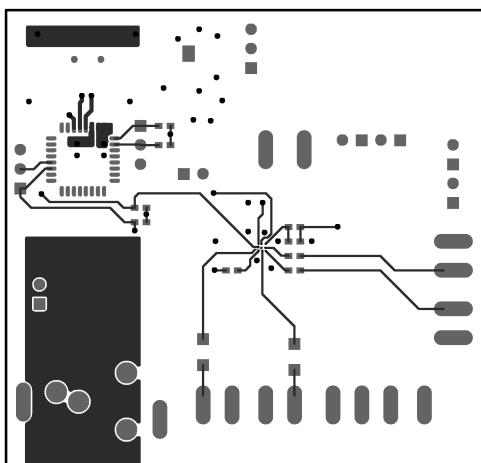
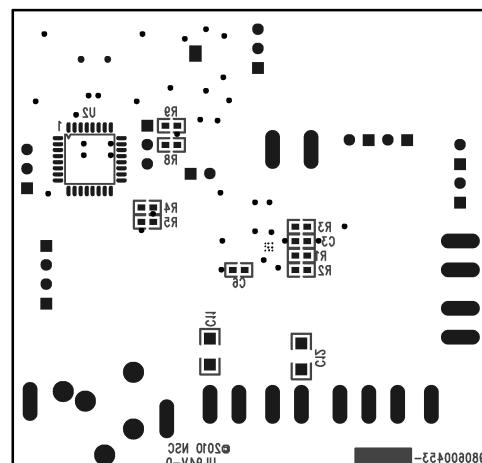
1. Unzip the LM49153 setup.zip file to a specified folder.
2. Run “LM49153 setup.msi” from the specified folder. If prompted to install Microsoft framework 2.0, please proceed to do so, internet connection may be required)
3. The LM49153 Control Software installation will begin.

Bill Of Materials

Item	Ref Designator	Part Description	Manufacturer	Part Number	Value	Footprint	Qty
1	PCB	LM49153EVAL PCB	Texas Instruments	551600453-001 RevA			1
2	U1	LM49153TMEVAL IC	Texas instruments	LM49153TM			1
3	U2	C8051F320	Silicon Labs	C8051F320		LQFP-32	1
4	U3	LP5900	Texas instruments	LP5900TL-1.8		uSMD-4	1
5	U4	LP38691-ADJ	Texas instruments	LP38691SD-ADJ		LLP-6	
6	C1, C4, C6, C7, C13	Ceramic Capacitor	Panasonic	ECJ-1VB1A225K	2.2uF	603	7
7	C5	Tantalum capacitor	AVX	TPSB106K016R0800	10uF	B Case	1
8	C9, C10	Ceramic Capacitor	Taiyo Yuden	EMK316B7105KF-T	1uF	1206	2
9	C11, C12	Ceramic Capacitor	Panasonic	ECJ-3VB1C224K	0.22uF	1206	2
10	C14, C15	Ceramic Capacitor	Taiyo Yuden	JMK107BJ106MA-T	10uF	603	2
11	C16, C17	Ceramic Capacitor	Kemet	C0603C474K4RACTU	0.47uF	603	2
12	C3, C18, C20	Ceramic Capacitor	Kemet	C0603C104J3RACTU	0.1uF	603	2
13	C2, C8, C19, C21	Ceramic Capacitor	Taiyo Yuden	LMK107BJ475KA-T	4.7uF	603	2
14	J1	Mini USB B Type	Hirose	UX60-MB-5ST			1
15	JU1	5-pole Headphone Jack	Switch Craft	35RAPC4BH3			1
16	L1, L2	FERRITE	Murata	BLM21PG300SN1D	FERRITE CHIP 30 OHM 3000MA 0805	805	2
17	R1, R2	0603 Resistor	Panasonic	ERJ-3EKF10R0V	10ohm	603	2
18	R4, R5, R8, R9	0603 Resistor	Vishay/Dale			603	4
19	R6	0603 Resistor	Vishay/Dale			603	1
20	R7	0603 Resistor	Vishay/Dale			603	1
21	EP+, EP-, EPOUT+, EPOUT-, GND, GND1, GND2, GND3, GND4, GND5, GND6, GND7, GND8, HPL, HPR, HPVDD, INL2, INM+/INL1, INM-/INR1, INR2, VDD, LSOUT+, LSOUT-, JU3	2-pin 100 mil Jumper	AMP	87220-2			24
22	JU2, JU4, JU5	CONN HEADR BRKWAY. 10003POS STR	TYCO	9-146285-0-03			
23	R3						

Demo Board Schematic Diagram



Demo Board Layout

Figure 28. Top Layer

Figure 29. Top Silkscreen

Figure 30. Layer 2

Figure 31. Layer 3

Figure 32. Bottom Layer

Figure 33. Bottom Silkscreen

Revision History

Rev	Date	Description
1.0	12/02/10	Initial WEB released.
1.01	12/08/10	Text edits.
1.02	03/31/11	Changed the Typical value on Xtalk from 68 to 78 (EC table).
1.03	04/01/11	Changed the Typical value on Xtalk from 78 to 80 (EC table).
C	05/03/13	Changed layout of National Data Sheet to TI format.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM49153TME/NOPB	ACTIVE	DSBGA	YFQ	25	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GO1	Samples
LM49153TMX/NOPB	ACTIVE	DSBGA	YFQ	25	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GO1	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

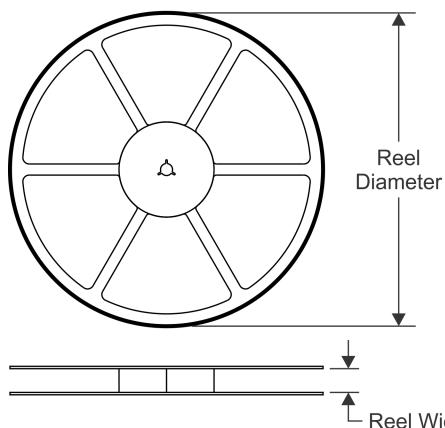
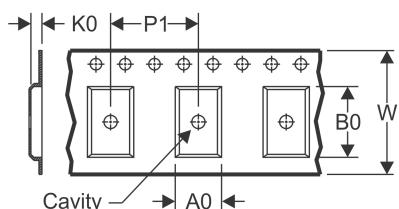
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

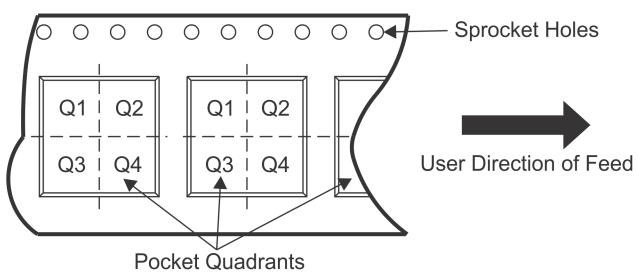
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

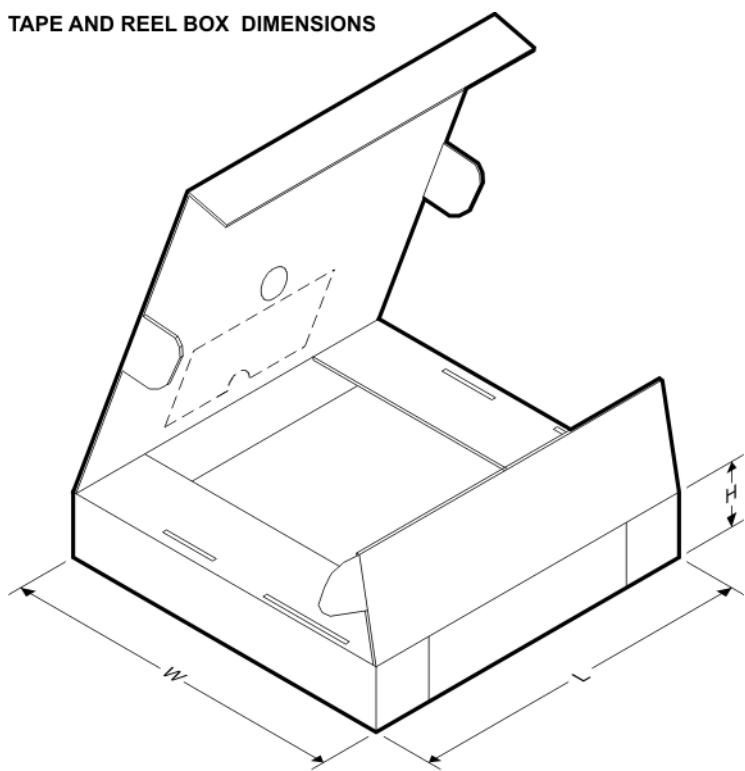
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

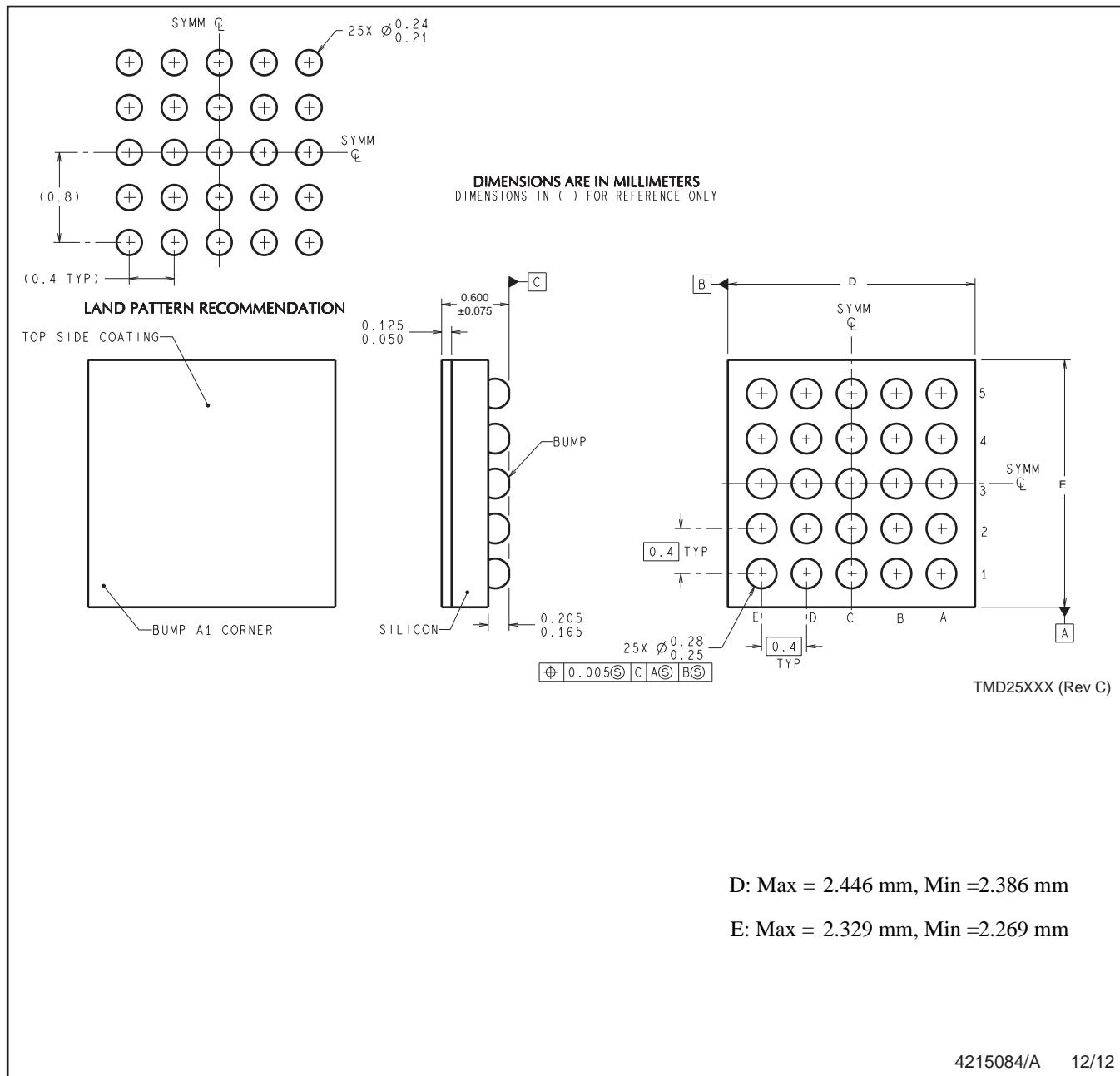
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM49153TME/NOPB	DSBGA	YFQ	25	250	178.0	8.4	2.39	2.64	0.76	4.0	8.0	Q1
LM49153TMX/NOPB	DSBGA	YFQ	25	3000	178.0	8.4	2.39	2.64	0.76	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM49153TME/NOPB	DSBGA	YFQ	25	250	210.0	185.0	35.0
LM49153TMX/NOPB	DSBGA	YFQ	25	3000	210.0	185.0	35.0

YFQ0025



IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.