Si8900/1/2

ISOLATED MONITORING ADC

Features

- ADC
  - 3 input channels
  - 10-bit resolution
  - 2.5 µs conversion time
- Isolated serial I/O port
  - UART (Si8900)
  - I^2C/SMbus (Si8901)
  - 2 MHz SPI port (Si8902)
- Transient immunity: 45 kV/µs (typ)
- Temperature range: –40 to +85 °C
- >60-year life at rated working voltage
- CSA component notice 5A approval
- IEC 60950, 62368, 60601
- VDE 0884-10
- UL1577 recognized
  - Up to 5 kVrms for 1 minute

Ordering Information:

See page 27.

Applications

- Isolated data acquisition
- AC mains monitor
- Solar inverters
- Isolated temp/humidity sensing
- Switch mode power systems
- Telemetry

Description

The Si8900/1/2 series of isolated monitoring ADCs are useful as linear signal galvanic isolators, level shifters, and/or ground loop eliminators in many applications including power-delivery systems and solar inverters. These devices integrate a 10-bit SAR ADC subsystem, supervisory state machine and isolated UART (Si8900), I^2C/SMbus port (Si8901), or SPI Port (Si8902) in a single package. Based on Silicon Labs' proprietary CMOS isolation technology, ordering options include a choice of 2.5 or 5 kV isolation ratings. All products are safety certified by UL, CSA, and VDE. The Si8900/1/2 devices offer a typical common-mode transient immunity performance of 45 kV/µs for robust performance in noisy and high-voltage environments. Devices in this family are available in 16-pin SOIC wide-body packages.

Safety Approval

- UL 1577 recognized
  - Up to 5 kVrms for 1 minute
- CSA component notice 5A approval
  - IEC 60950, 62368, 60601
- VDE certification conformity
  - VDE 0884-10

Pin Assignments

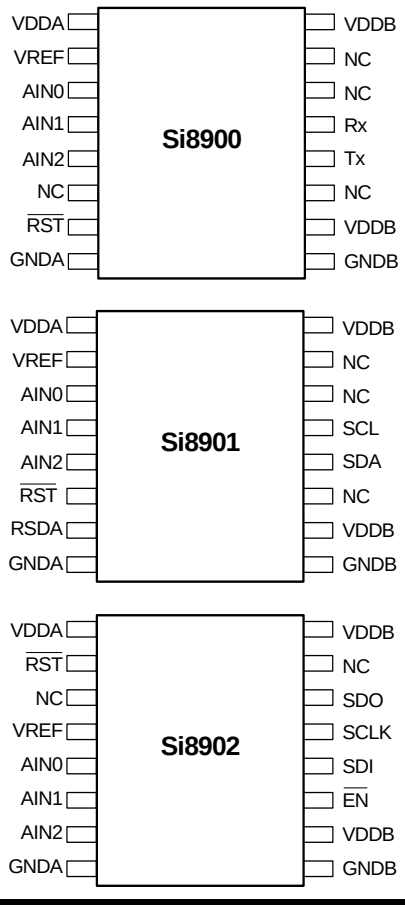


TABLE OF CONTENTS

1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Side Supply Voltage	V_{DDA}	With respect to GNDA	2.7	—	3.6	V
Input Side Supply Current	I_{DDA}	V_{DDA} = 3.3 V, Si890x active	—	10	13.3	mA
		V_{DDA} = 3.3 V, Si890x idle	—	8.6	11.4	
Output Side Supply Voltage	V_{DDB}	With respect to GNDB	2.7	—	5.5	V
Output Side Supply Current	I_{DDB}	V_{DDB} = 3.3 V to 5.5 V, Si890x active	—	4.4	5.8	mA
		V_{DDB} = 3.3 V to 5.5 V, Si890x idle	—	3.3	3.9	
Operating Temperature	T_A		–40	—	+85	°C

Table 2. Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ADC						
Resolution	R			10		bits
Integral Nonlinearity	INL	VREF = 2.4 V	—	±0.5	±1	LSB
Differential Nonlinearity	DNL	VREF = 2.4 V, Guaranteed Monotonic	—	±0.5	±1	LSB
Offset Error	OFS		–2	0	+2	LSB
Full Scale Error	FSE		–2	0	+2	LSB
Offset Tempco	T_{OS}		—	45	—	ppm/°C
Input Voltage Range	V_{IN}		0		V_{REF}	V
Sampling Capacitance	C_{IN}		—	5	—	pF
Input MUX Impedance	R_{MUX}		—	5	—	kΩ
Power Supply Rejection	PSRR		—	–70	—	dB
Reference Voltage	V_{REF}	Default V_{REF} = V_{DDA}	0	—	V_{DDA}	V
VREF Supply Current	I_{VREF}		—	12	—	µA
ADC Conversion Time	t_{CONV}			2.5		µs

Table 2. Electrical Specifications (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Reset and Undervoltage Lockout						
Power-on RESET Voltage Threshold High	VRSTH		—	—	1.8	V
Power-on RESET Voltage Threshold Low	VRSTL		1.7	—	—	V
VDDA Power-On Reset Ramp Time	tRAMP	Time from VDDA = 0 V to VDDA ≥ VRST	—	—	1	ms
Power-On Reset Delay Time	tPOR	tRAMP < 1 ms			0.3	ms
Output Side UVLO Threshold	UVLO		—	2.3	—	V
Output side UVLO Hysteresis	H		—	100	—	mV
Digital Inputs						
Logic High Level Input Voltage	V_{IH}		0.7 x V_{DDB}	—	—	V
Logic Low Level Input Voltage	V_{IL}		—	—	0.6	V
Logic Input Current	I_{IN}	VIN = 0 V or V_{DD}	–10		+10	µA
Input Capacitance	C_{IN}		—	15	—	pF
Digital Outputs						
Logic High Level Output Voltage	V_{OH}	V_{DDB} = 5 V, I_{OH} = –4 mA	V_{DDB} – 0.4	4.8	—	V
		V_{DDB} = 3.3 V, I_{OH} = –4 mA	V_{DDB} – 0.4	3.1	—	V
Logic Low Level Output Voltage	V_{OL}	V_{DDB} = 3.3 to 5 V, I_{OL} = 4 mA	—	0.2	0.4	V
Digital Output Source Impedance	R_{OUT}		—	50	—	Ω
Serial Ports						
UART Bit Rate			60	—	500	kbps
SMBus/I^2C Bit Rate		Slave Address = 1111000x	—	—	240	kbps
SPI Port Bit Rate		Mode 3: CPOL = 1, CPHA = 1	—	—	2	Mbps

Table 2. Electrical Specifications (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SPI Port Timing						
$\overline{EN}$ Falling Edge to SCLK Rising Edge	t_{SE}		80	—	—	ns
Last Clock Edge to /EN Rising	t_{SD}		80	—	—	ns
$\overline{EN}$ Falling to SDO Valid	t_{SEZ}		—	—	160	ns
SCLK High Time	t_{CKH}		200	—	—	ns
SCLK Low Time	t_{CKL}		200	—	—	ns
SDI Valid to SCLK Sample Edge	t_{SIS}		80	—	—	ns
SCLK Sample Edge to SDI Change	t_{SIH}		80	—	—	ns
SCLK Shift Edge to SDO Change	t_{SOH}		—	—	160	ns

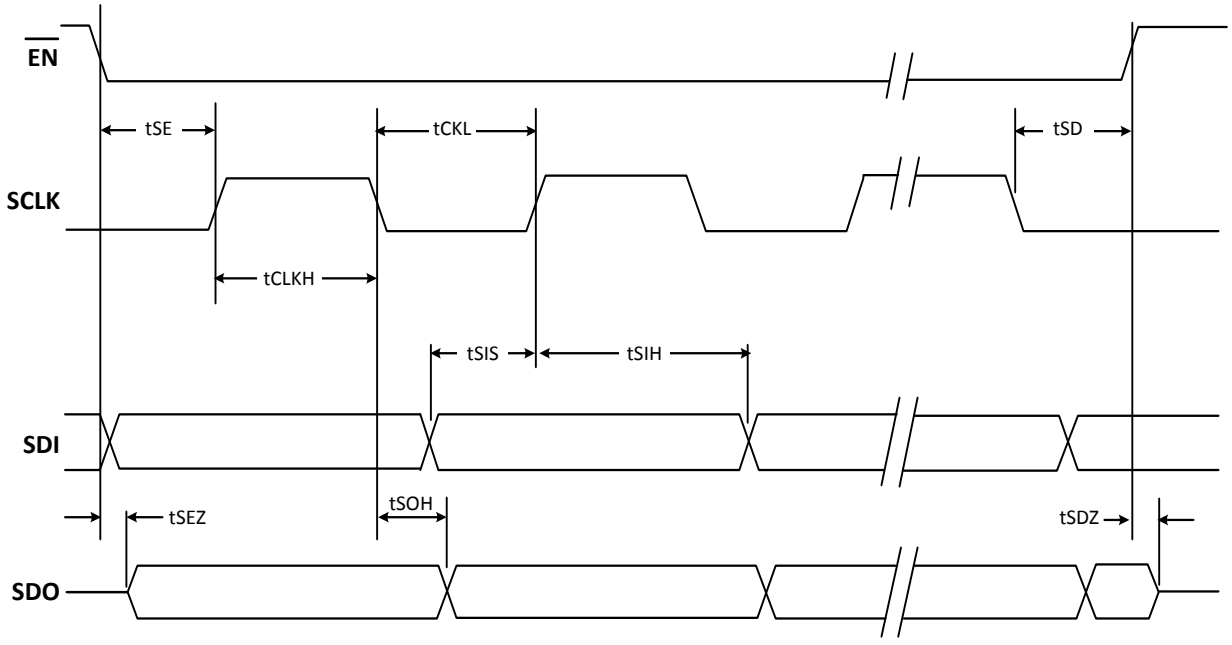


Figure 1. SPI Port Timing Characteristics

Table 3. Thermal Characteristics

Parameter	Symbol	Test Condition	WB SOIC-16	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}		100	ºC/W

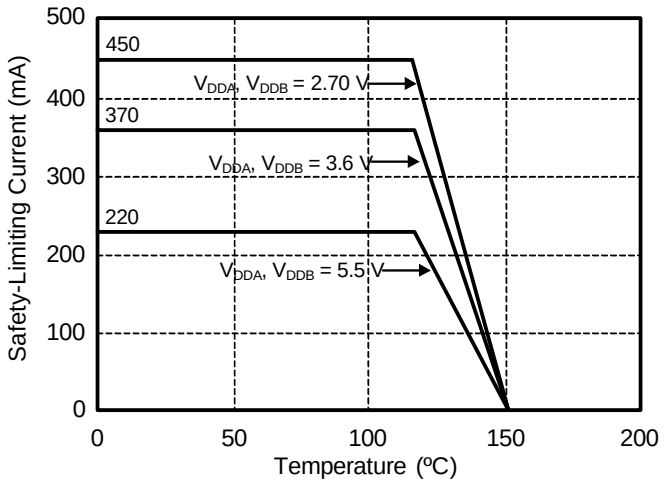


Figure 2. (WB SOIC-16) Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit
Storage Temperature	T_{STG}	–65	—	150	°C
Ambient Temperature under Bias	T_A	–40	—	85	°C
Input-Side Supply Voltage	V_{DDA}	–0.5	—	6.0	V
Output-Side Supply Voltage	V_{DDB}	–0.5	—	6.0	V
Input/Output Voltage	V_I	–0.5	—	VDD +0.5	V
Output Current Drive	I_O	—	—	10	mA
Lead Solder Temperature (10 s)		—	—	260	°C
Maximum Isolation Voltage		—	—	6500	V_{RMS}

***Note:** Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Regulatory Information

The Si8900/1/2 family is certified by Underwriters Laboratories, CSA International, and VDE. Table 5 summarizes the certification levels supported.

Table 5. Regulatory Information

CSA The Si89xx is certified under CSA Component Acceptance Notice 5A. For more details, see Master Contract Number 232873. 62368-1: Up to 600 VRMS reinforced insulation working voltage; up to 1000 VRMS basic insulation working voltage. 60950-1: Up to 600 VRMS reinforced insulation working voltage; up to 1000 VRMS basic insulation working voltage. 60601-1: Up to 125 VRMS reinforced insulation working voltage; up to 380 VRMS basic insulation working voltage.
VDE The Si89xx is certified according to VDE 0884-10. For more details, see File 5006301-4880-0001. 0884-10: Up to 1200 Vpeak for basic insulation working voltage. 60950-1: Up to 600 VRMS reinforced insulation working voltage; up to 1000 VRMS basic insulation working voltage.
UL The Si89xx is certified under UL1577 component recognition program. For more details, see File E257455. Rated up to 5000 VRMS isolation voltage for basic protection.

3. Functional Description

The Si8900/1/2 (Figure 3) are isolated monitoring ADCs that convert input signals into digital format and transmit the resulting data through an on-chip isolated serial port to an external master processor (typically a microcontroller). The Si890x access protocol is simple: The master configures and controls the start of ADC conversion by writing a configuration register (CNFG_0) Command Byte to the Si890x. The master then acquires ADC conversion data by reading the Si890x serial port. Devices in this series differ only in the type of serial port. Options include a UART with on-chip baud rate generator that operates at 500 kbps max (Si8900), an SMBus/I^2C port that operates at 240 kbps max (Si8901), and an SPI Port that operates at 2 MHz max (Si8902).

The integrated ADC subsystem consists of a three-channel analog input multiplexer (MUX) followed by a series gain amplifier (selectable 1x or 0.5x gain) and 10-bit SAR ADC. Serial-port-accessible ADC options allow the user to select VDDA or a different reference voltage applied to the VREF pin, set the programmable gain amplifier (PGA), and select the ADC MUX address. The master can configure the Si890x to return ADC data on-demand (Demand Mode) or continuously (Burst Mode). For more information, see " CNFG_0 Command Byte" on page 20.

The $\overline{RST}$ pin on the input side resets the state machine. For the Si8901, the RSDA pin connects to an external pullup resistor to VDDA to allow operation of I2C/SMBus communication.

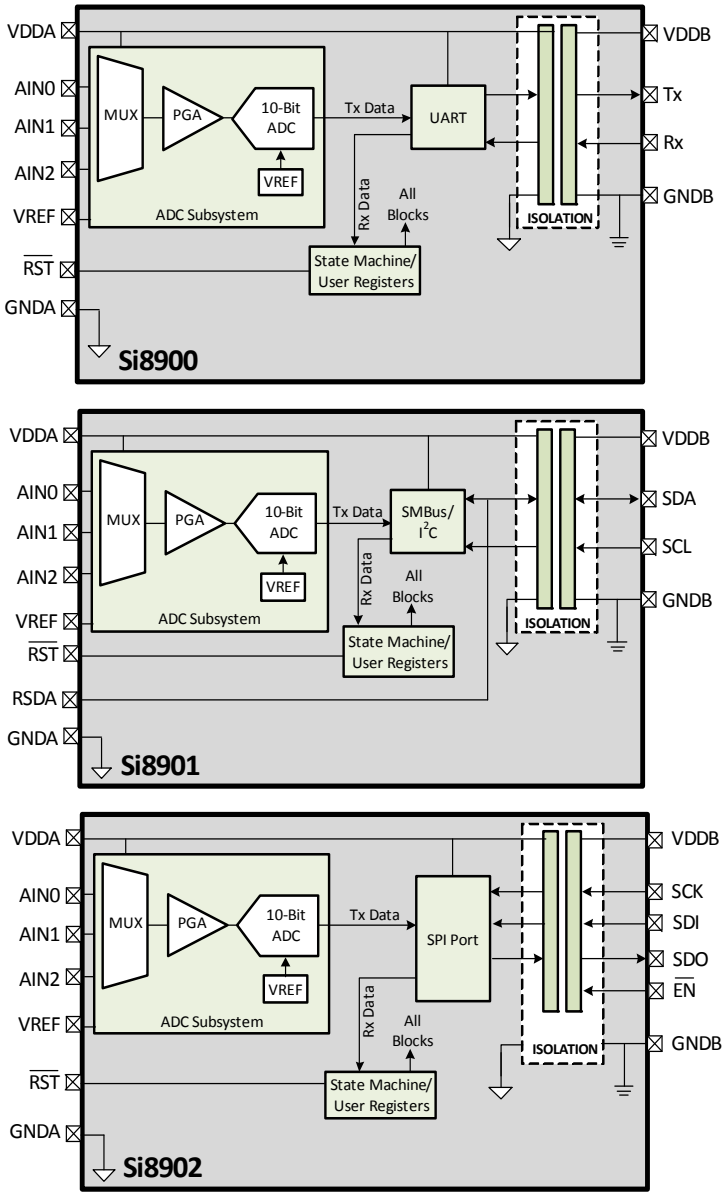


Figure 3. Si8900/1/2 Block Diagrams

4. ADC Data Transmission Modes

The Si890x ADC performs conversions by exercising the serial port. Each of the three channels can be in Demand Mode (MODE=1) or Burst Mode (MODE=0). Upon power cycle or reset, all channels are initialized to Demand Mode. The CNFG=0 command byte can be used to switch a channel between Demand and Burst modes. Demand Mode ADC conversions are initiated by Demand Mode CNFG=0 commands. Once a channel is in Burst Mode, ADC conversions are initiated by byte reads of the serial port. An advantage of Burst Mode is the conversion time of each ADC sample is masked by the time it takes to read data bytes on the serial port. An advantage of Demand Mode over multiple channels in Burst Mode is the master controller will dictate which ADC channel is sampled immediately.

4.1. Demand Mode

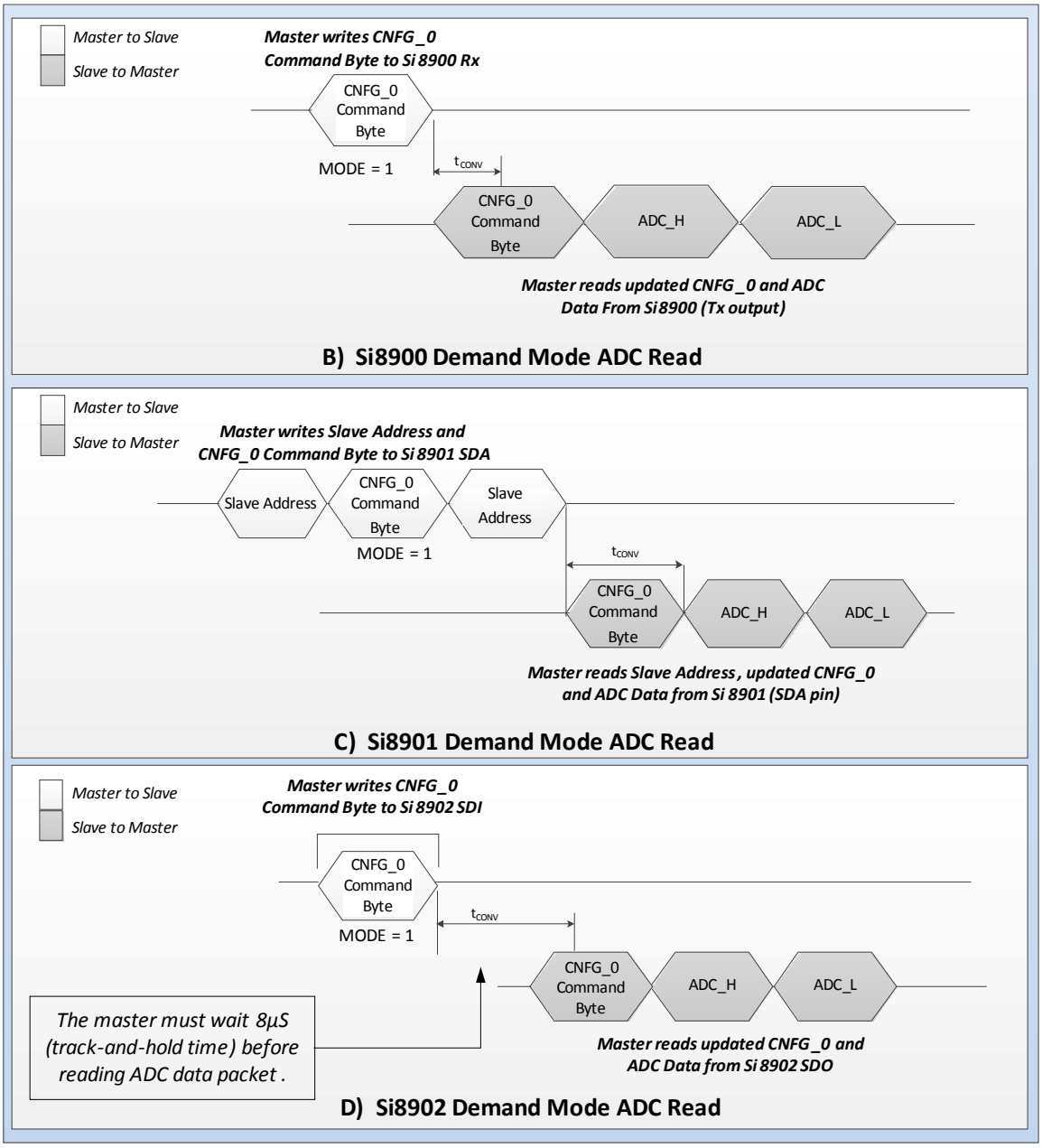


Figure 4. ADC Demand Mode Operation

Referring to Figure 4A, a Demand Mode ADC read is initiated when the master writes a Command Byte to the Si8900. Upon receipt of the Command Byte, the Si8900 updates its CNFG_0 register and triggers the start of an ADC conversion, at which time the master may immediately begin reading ADC conversion data from the Si8900 UART. The ADC conversion data packet contains an echo of the Command Byte for verification and two-bytes of ADC conversion data. The Si8901 (Figure 4B) ADC read transaction is identical to that of the Si8900 with the exception of the added I^2C/SMBus Slave Address byte (Si8901 Slave Address is 0xF0). For the slower UART and I^2C, the required tconv delay is consumed by reading the echo command byte. Since SPI supports the fastest data rate, the master controller may need to delay before reading the SPI port. If the SPI read request occurs before valid data is available, the Si8902 will output 0xFF bytes until valid data is available. The Si8902 Demand Mode ADC read transaction (Figure 4C) is the same as that of the Si8900, except the master must wait 8 µs after the transmission of the Command Byte before reading the Si8902 SPI port because byte transmission time is two times shorter versus the Si8900/01.

4.2. Burst Mode

Figure 5 shows the byte sequence for a channel operating in Burst Mode. A channel is switched from Demand Mode to Burst Mode by writing a command CNFG_0 byte with MODE=0. Placing a channel in Burst Mode negates the need to write subsequent CNFG_0 commands to initiate ADC conversions. At all serial port communication speeds, the tconv is masked by the data rate of the data byte reads. Like the Demand Mode example, the Si8901 has a Slave Address byte prior to the CNFG_0 Command Byte. When using the Si8901, the master must write the I^2C port address prior to reading the serial port. The Si8902 Burst Mode (Figure 5C) is similar to that of the Si8900/1, except the master must wait 8 µs before reading the first Burst Mode ADC data packet. After reading the first Burst Mode ADC data packet, the master may read all ADC data packets that follow without delay.

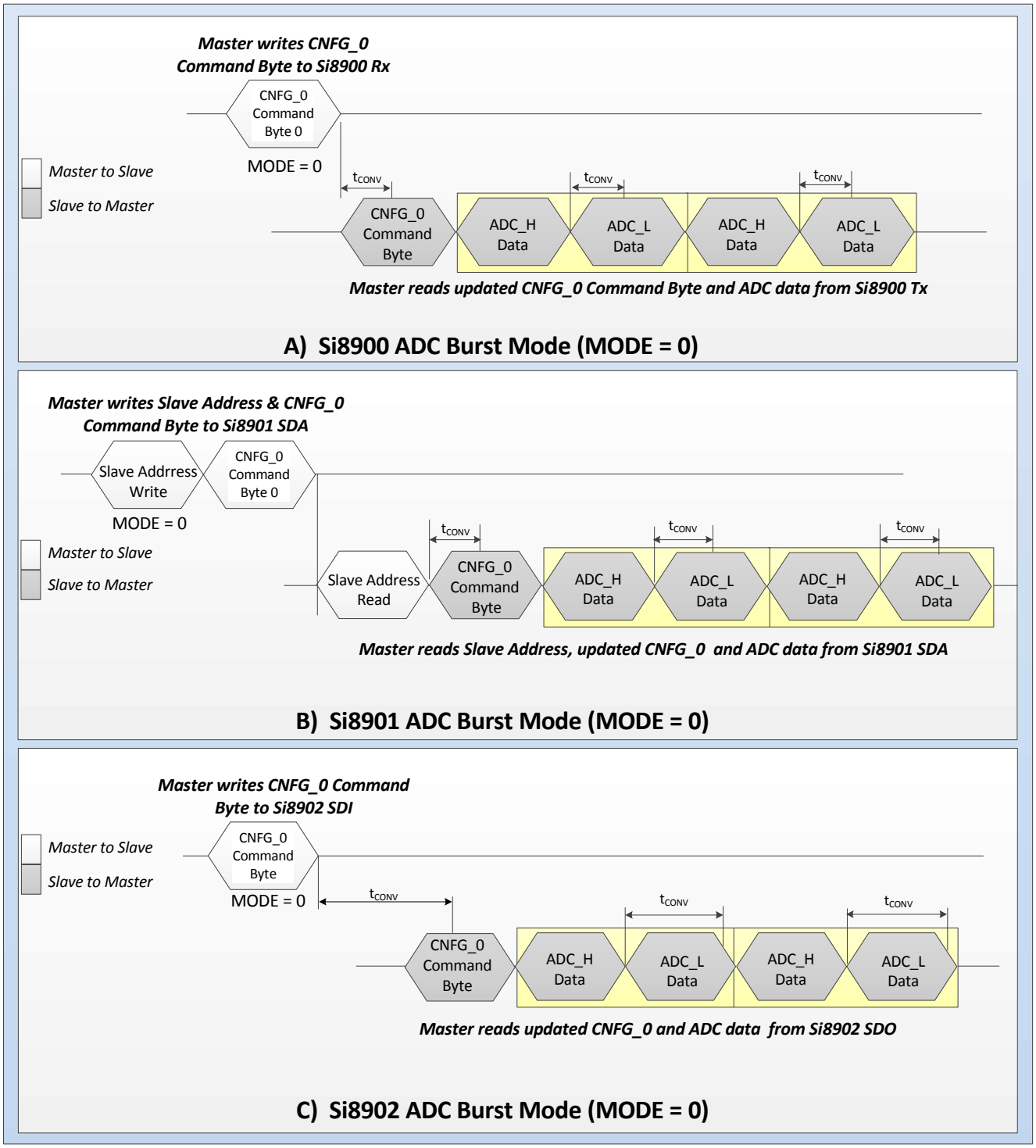


Figure 5. ADC Burst Mode Operation

4.3. Multiple Channel Burst Mode

It is possible to set any channel from Demand to Burst Mode and any Burst Mode Channel back to Demand Mode. However, CNFG_0 command byte can only write to one channel at a time. To operate two or more channels in Burst Mode, first set one channel to Burst Mode. This will enable the first Burst Channel operation. The master controller will then need to set additional channels to Burst Mode by writing another CNFG_0 command byte.

For the Si8901, communication is half duplex. Therefore, the data reads of a previously set burst channel must be interrupted by writing a new CNFG_0 command to set the additional channel to Burst Mode.

For the Si8900 and Si8902, communication is full duplex, and a new CFNG_0 command byte can be written at the same time as reading data from a previously set burst channel. Depending on where the new CNFG_0 command is received during the burst read, the Si8902 may output data with MX0 = 1 and MX1 = 1 (see “5. Si8900/1/2 Configuration Registers”), which does not point to a valid channel. Ignore that ADC_H byte and the following ADC_L byte. This is a temporary artifact of having restarted the burst sequence with an additional burst-enabled channel. See "4.7. Master Controller Firmware" on page 19.

To parse the data stream for multiple burst mode channels, the master controller must analyze the MX0 and MX1 bits of the ADC_H byte. For each ADC_H byte received, the next ADC_L byte received is the second part of that channel's data. The Si890x will cycle through all Burst Mode channels sequentially. For example, if channels 0 and 1 are in Burst Mode, the data read back will have this order: ADC_H (MX1=0, MX0=0), ADC_L, ADC_H (MX1=0, MX0=1), ADC_L, ADC_H (MX1=0, MX0=0), ADC_L, and so on.

4.4. UART (Si8900)

The UART is a two-wire interface (Tx, Rx) and operates as an asynchronous, full-duplex serial port with internal auto baud rate generator that measures the period of incoming data stream and automatically adjusts the internal baud rate generator to match. The auto baud rate detection and matching optimizes UART timing for minimum bit error rate. For more information, see “AN635: Si8900 Automatic Baud Rate Detection”.

There are a total of 10 bits per data byte: One start bit, eight data bits (LSB first), and one stop bit with data transmitted LSB first as shown in Figure 6. Figure 7A and Figure 7B show master/Si8900 ADC read transactions for Demand Mode and Burst Mode, respectively.

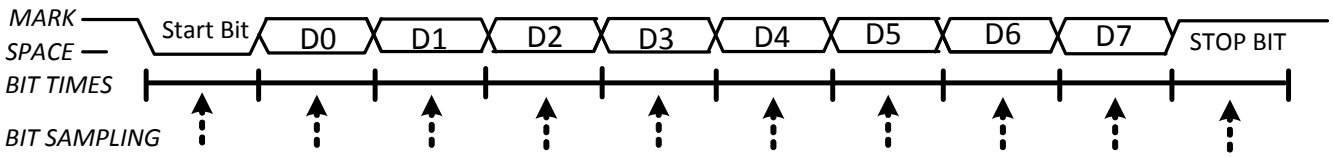


Figure 6. UART Data Byte

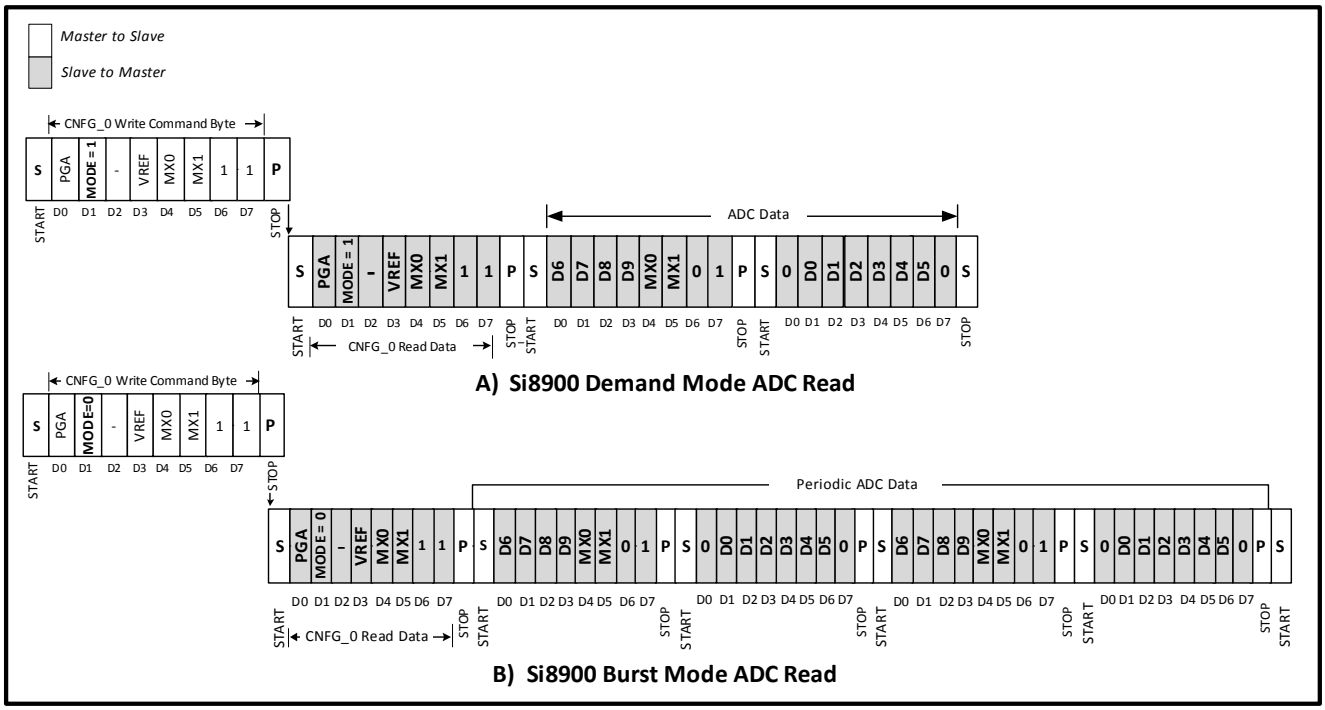


Figure 7. Si8900 ADC Read Operation

4.5. I²C/SMBus (Si8901)

The I²C/SMBus serial port is a two-wire serial bus where data line SDA is bidirectional and clock line SCL is unidirectional. Reads and writes to this interface by the master are byte-oriented, with the I²C/SMBus master controlling the serial data rates up to 240 kbps. The SDA and SCL lines must be pulled high through pull-up resistors of 5 kΩ or less. An Si8901 ADC read transaction begins with a START condition (“S” or Repeated START condition “SR”), which is defined as a high-to-low transition on SDA while SCL is high (Figure 8). The master terminates a transmission with a STOP condition (P), defined as a low-to-high transition on SDA while SCL is high. The data on SDA must remain stable during the high period of the SCL clock pulse because such changes in either line will be interpreted as a control command (e.g., S, P SR). SDA and SCL idle in the high state when the bus is not busy. Acknowledge bits (Figure 9) provide detection of successful data transfers, whereas unsuccessful transfers conclude with a not-acknowledge bit (NACK). Both the master and the Si8901 generate ACK and NACK bits. An ACK bit is generated when the receiving device pulls SDA low before the rising edge of the acknowledged related (ninth) SCL pulse and maintains it low during the high period of the clock pulse. A NACK bit is generated when the receiver allows SDA to be pulled high before the rising edge of the acknowledged related SCL pulse and maintains it high during the high period of the clock pulse. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master attempts communication at a later time. Figure 10A shows the I²C Slave Address Byte and CNFG_0 byte for the Si8901. Figure 10B and Figure 10C show master/Si8901 ADC read transactions for Demand Mode and Burst Mode, respectively.

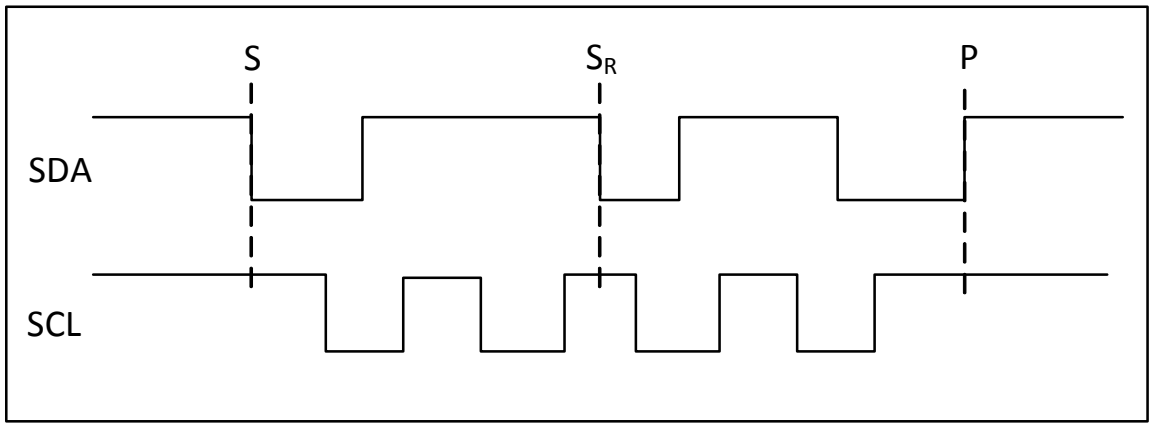


Figure 8. Start and Stop Conditions

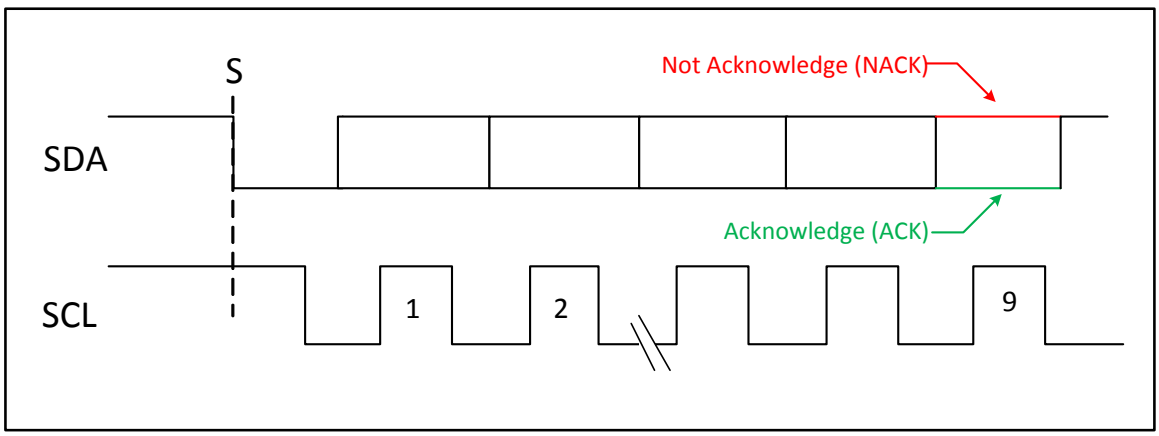


Figure 9. Acknowledge Cycle

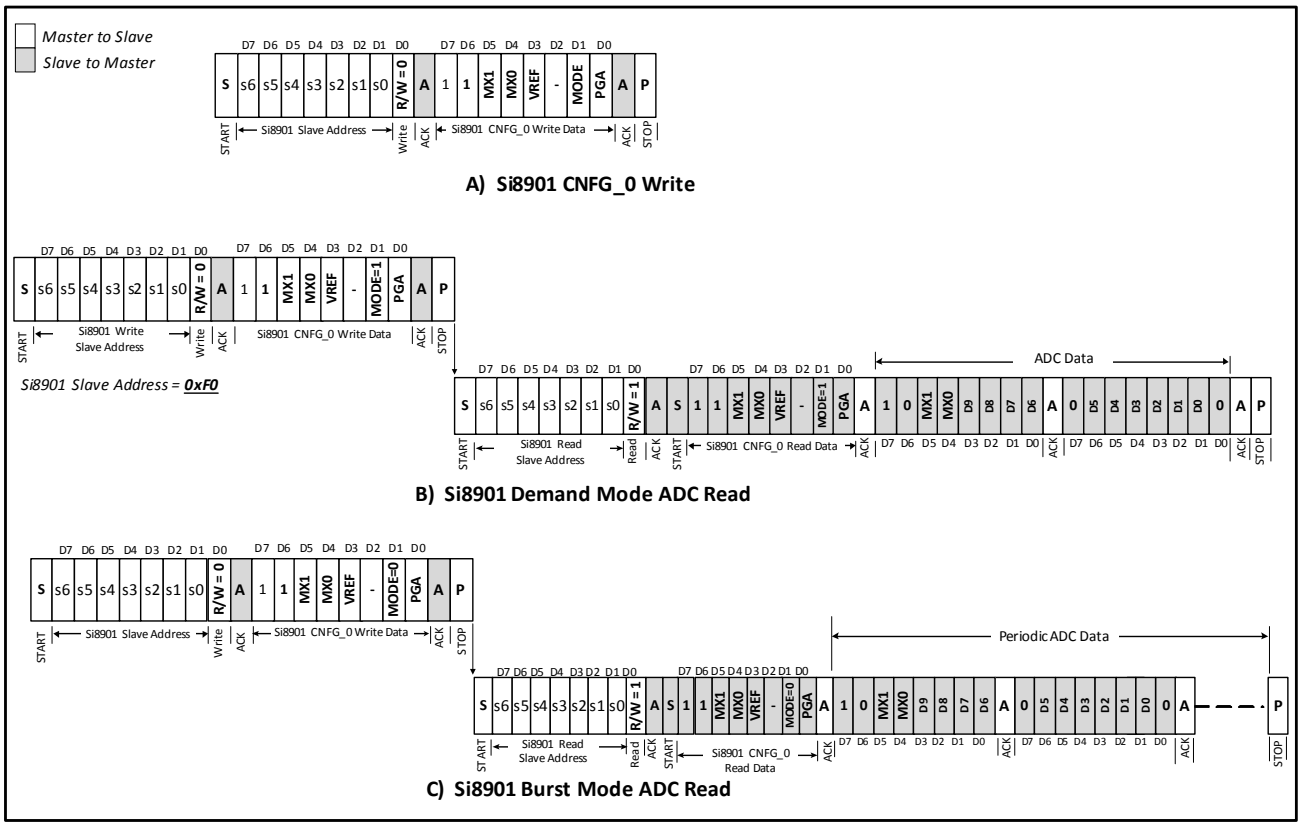


Figure 10. Si8901 ADC Read Operation

4.6. SPI Port (Si8902)

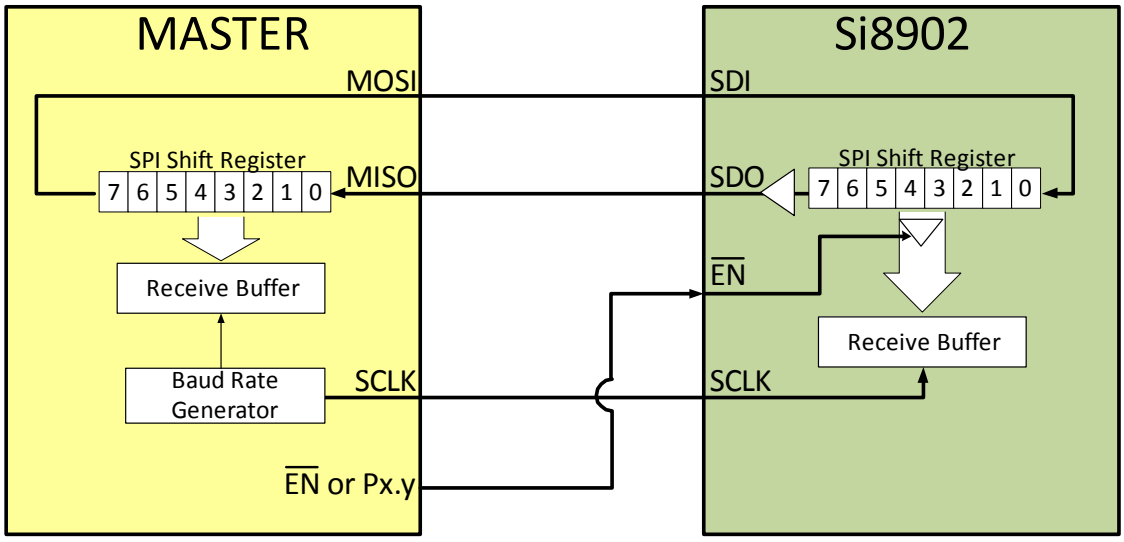


Figure 11. Master Connection to Si8902

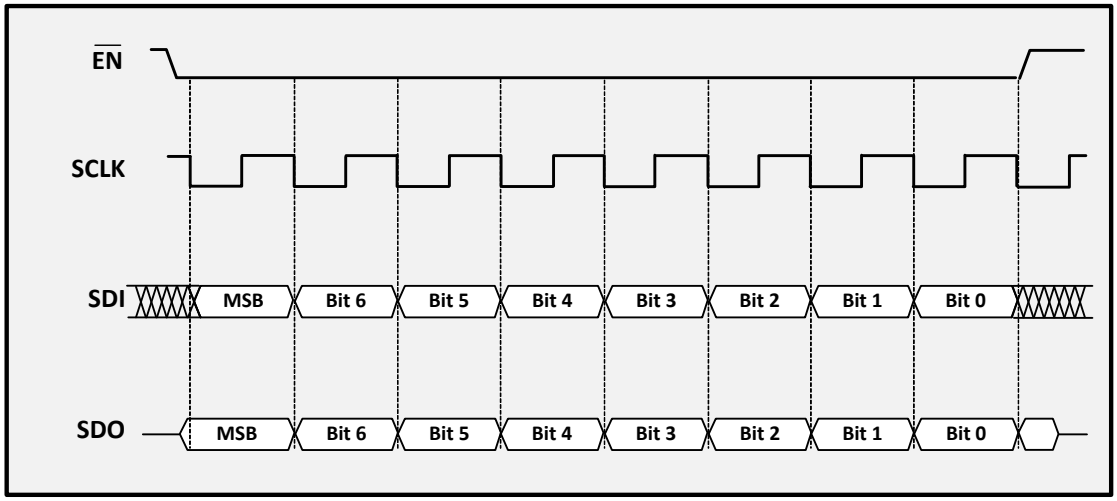


Figure 12. Si8902 Data/Clock Relationship

The Serial Peripheral Interface (SPI port) is a slave mode, full-duplex, synchronous, 4-wire serial bus that connects to the master as shown in Figure 11. The master's clock and data timing must match the Si8902 timing shown Figure 12 (for more information about clock and data timing, please see the “SPI Port” section of Table 2 on page 5).

As shown in Figure 13, the Si8902 will update output data on SDO with falling SCLK edge and sample data on SDI with rising SCLK edge. For idle condition between bytes, EN and SCLK should be held high by the master controller. Also, during ADC_H and ADC_L byte reads, the master controller must hold SDI high. The master transmits data from its master-out/slave-in terminal (MOSI) to the Si8902 serial read/write input terminal (SDI). The Si8902 transmits data to the master from its serial data-out terminal (SDO) to the master-in/slave-out terminal (MISO), and data transfer ends when the master returns EN to the high state. Figure 13A shows the Si8902 CNFG_0 Command Byte format, while Figures 13B and 13C show Si8902 Demand Mode and Burst Mode ADC reads.

The Si8902 SDO pin will either drive low or drive high. It does not go into Hi-Z when EN is deasserted. Therefore, a system with multiple SPI slaves should use separate MISO signals to avoid SPI bus contentions.

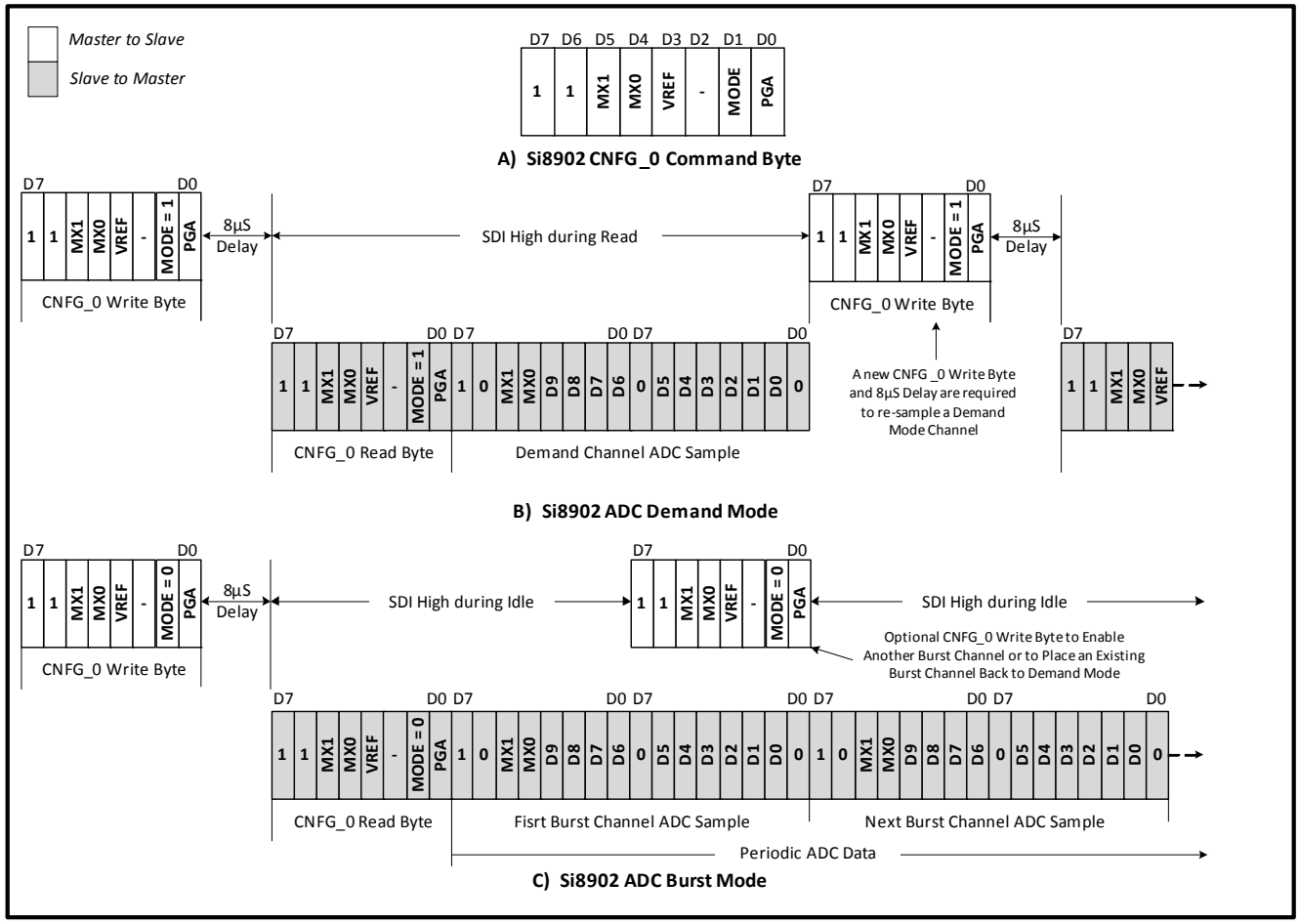


Figure 13. Si8902 ADC Read Operation

4.7. Master Controller Firmware

The user's master controller must include firmware to manage the Si890x Demand and Burst operating modes and serial port control. For more information on master controller firmware, see “AN637: Si890x Master Controller Recommendations”, available for download at www.silabs.com/isolation.

5. Si8900/1/2 Configuration Registers

CNFG_0 Command Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	1	1	MX1	MX0	VREF	—	MODE	PGA
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Function
7:6	1,1	Internal use. These bits are always set to 1.
5:4	MX1, MX0	**ADC MUX Address.** ADC MUX address selection is controlled by MX1, MX0 as follows: MX1 / MX0 / Selected ADC MUX Channel 1 / 1 / Not Used 1 / 0 / AIN2 0 / 1 / AIN1 0 / 0 / AIN0
3	VREF	**ADC Voltage Reference Source** VDD is selected as the reference voltage when this bit is set to 1. An externally connected voltage reference generator is selected when this bit is reset to 0.
2	—	Not used.
1	MODE	**ADC Read Mode** ADC Demand Mode read is enabled when this bit is 1, and Burst Mode is enabled when this bit is 0. For more information on Demand and Burst mode operation, please see "4. ADC Data Transmission Modes" on page 11.
0	PGA	**PGA Gain Set** PGA gain is 1 when this bit is set to 1. PGA gain is 0.5 when this bit is reset to 0.

ADC_H Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	1	0	MX1	MX0	D9	D8	D7	D6
Type	R	R	R	R	R	R	R	R

Bit	Name	Function
7:6	1,0	Internal use. These bits are always set to 1,0.
5:4	MX1, MX0	**ADC MUX Address** ADC input MUX address for the converted data in ADC_H, ADC_L.
3:0	D9: D6	**ADC conversion data bits D9:D6** Most significant 4 bits of ADC conversion data.

ADC_L Byte

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	D5	D4	D3	D2	D1	D0	0
Type	R	R	R	R	R	R	R	R

Bit	Name	Function
7	0	Internal use. This bit is always set to 0.
6:1	D5:D0	**ADC Conversion Data Bits D5:D0** Least significant 6 bits of ADC conversion data.
0	0	Internal use. This bit is always set to 0.

6. Applications

6.1. Isolated Outputs

The Si890x serial outputs are internally isolated from the device input side. To ensure safety in the end-user application, high voltage circuits (i.e., circuits with >30 VAC) must be physically separated from the safety extra-low voltage circuits (i.e., circuits with <30 VAC) by a certain distance (creepage/clearance). If a component straddles this isolation barrier, it must meet those creepage/clearance requirements and also provide a sufficiently large high-voltage breakdown protection rating (commonly referred to as working voltage protection). Tables published in the component standards (UL1577, VDE 0884-10, CSA 5A) are readily accepted by certification bodies to provide proof for end-system specifications requirements. Refer to the end-system specification (62368-1, 60950-1, 60601-1, etc.) requirements before starting any circuit design that uses galvanic isolation. The nominal output impedance of a digital output is approximately 50 Ω ± 40%, which is a combination of the on-chip series termination resistor and channel resistance of the output driver FET. When driving high-impedance terminated PCB traces, outputs can be source terminated to minimize reflection.

The Si890x supply inputs must be bypassed with a parallel combination of 10 µF and 0.1 µF capacitors at VDDA and VDDB as shown in Figure 14A. The 0.1 µF capacitors should be placed as close to the package as possible. The Si890x uses the VDDA supply as its internal ADC voltage reference by default. A precision external reference can be installed as shown in Figure 14A and must be bypassed with a parallel combination of 0.1 µF and 4.7 µF capacitors. (Note that the CNFG_0 VREF bit must be set to 0 when using the external reference.) The Si890x has an on-chip power-on-reset circuit (POR) that maintains the device in its reset state until VDDA has stabilized. A 2 kΩ pull-up resistor and 10 nF capacitor on $\overline{\text{RST}}$ is strongly recommended to reduce the possibility of external noise coupling into the reset input. The capacitor slows the rise of voltage on $\overline{\text{RST}}$ during power up. The delay ensures a state machine resets on power up. A state machine reset with power on using the RC on $\overline{\text{RST}}$ will suffice for most applications. For the master controller to have access to this pin, a single channel Si8610 digital isolator can be placed in parallel with the Si890x and connected to the $\overline{\text{RST}}$ input. The Si8901 requires a 5 kΩ pull-up resistor to VDDA on the RSDA input.

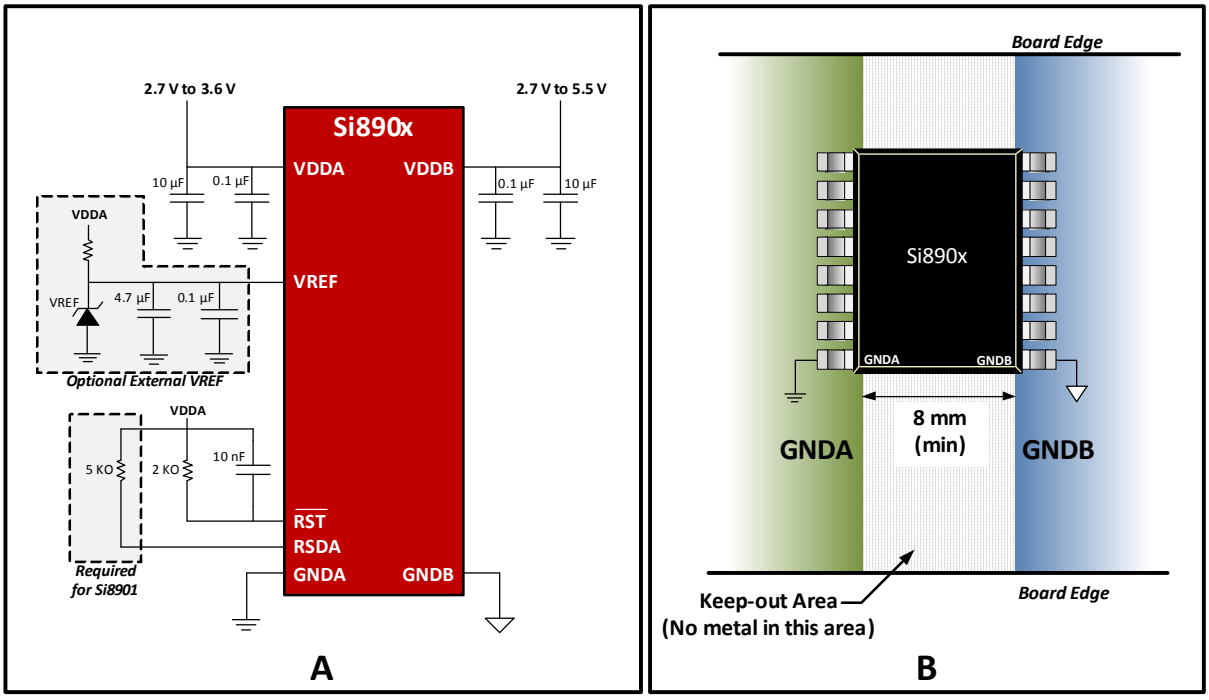


Figure 14. Si890x Installation

Figure 14B shows the required PCB ground configuration, where an 8 mm (min) “keep-out area” is provided to ensure adequate creepage and clearance distances between the two grounds. PCB metal traces *cannot* be present or cross through the keep-out area on the PCB top or bottom layer.

6.2. Device Reset

During power-up, the Si890x is held in the reset state by the internal power-on reset signal (POR) until VDDA settles above VRST. When this condition is met, a delay is initiated that maintains the Si890x in the reset state for time period tPOR, after which the reset signal is driven high allowing the Si890x to start-up. Note the maximum allowable VDD ramp time (i.e. time from 0 V to VDDA settled above VRST) is 1 ms. Slower ramp times may cause the Si890x to be released from reset before VDDA reaches the VRST level.

Figure 15 shows typical VDDA monitor reset timing where the internal reset is driven low (Si890x in reset) when VDDA falls below VRST (e.g., during a power down or VDDA brownout). The internal reset is released to its high state when VDDA again settles above VRST. External circuitry can also be used to force a reset event by driving the external RST input low. A 2 kΩ pull-up resistor on RST is recommended to avoid erroneous reset events from external noise coupling to the RST input.

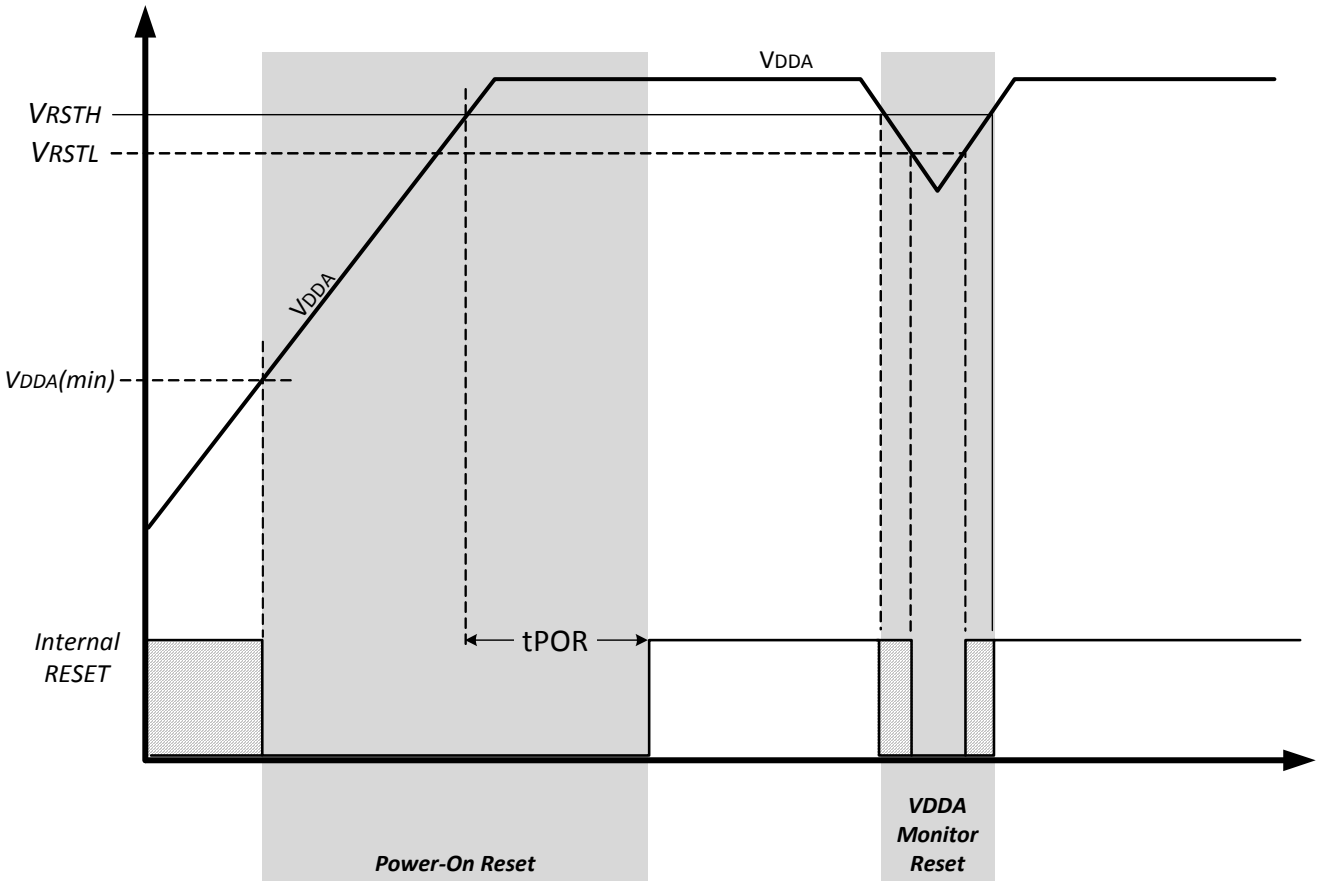


Figure 15. Si890x Power-on and Monitor Reset

6.3. Application Example

Figure 16 shows the Si8900 operating as a single-phase ac line voltage and current monitor. The VDDA dc bias circuit uses a low-cost 3.3 V linear regulator referenced to the neutral (white wire). The ac current is measured on ADC input AIN0. The ac line voltage is scaled by resistors R17 and R18 and level-shifted by the 1.5 V VREF. AC line current is measured using differential amplifier U1 connected across shunt resistor R1. Data is transferred to the external controller or processor via the isolated UART.

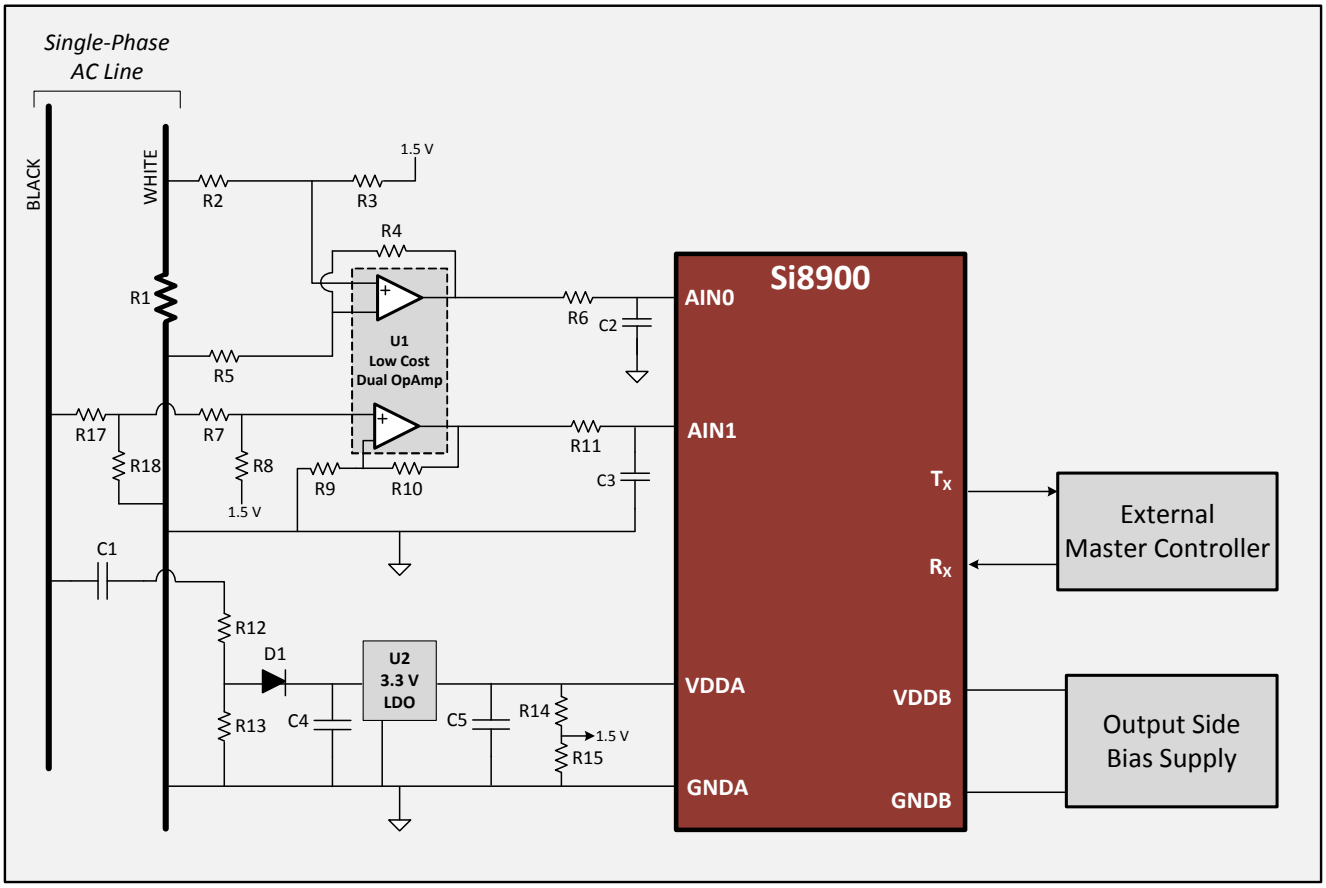


Figure 16. AC Line Monitor Application Example

7. Device Pin Assignments

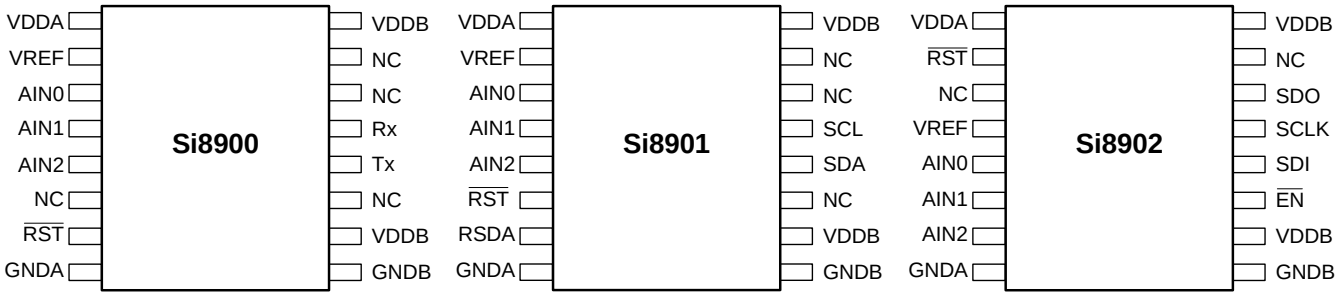


Figure 17. Si8900/1/2 Pinout (SOIC-16 WB)

Table 6. Si8900/1/2 Pin Assignments

Pin	Si8900 Pin	Si8901 Pin	Si8902 Pin	Description
1	VDDA			Input side VDD bias voltage (typically 3.3 V)
2	VREF		$\overline{\text{RST}}$	Si8900/1: External voltage reference input. Si8902: Active low reset.
3	AIN0	AIN0	NC	Si8900: ADC analog input channel 0. Si8901: ADC analog input channel 0. Si8902: No connection
4	AIN1	AIN1	VREF	Si8900: ADC analog input channel 1. Si8901: ADC analog input channel 1. Si8902: External VREF in.
5	AIN2	AIN2	AIN0	Si8900: ADC analog input channel 2. Si8901: ADC analog input channel 2. Si8902: ADC analog input channel 0.
6	NC	$\overline{\text{RST}}$	AIN1	Si8900: No Connection. Si8901: Active low reset. Si8902: ADC analog input channel 1.
7	$\overline{\text{RST}}$	RSDA	AIN2	Si8900: Active low reset. Si8901: RSDA bias resistor (typically 5 kΩ). Si8902: ADC analog input channel 2.
8	GNDA			Input side ground
9	GNDB			Output side ground
10	VDDB			Output side VDD bias voltage (2.7 V to 5.5 V)
11	NC		$\overline{\text{EN}}$	Si8900/1: No connection. Si8902: SPI Port Enable.
12	Tx	SDA	SDI	Si8900: UART unidirectional transmit output. Si8901: I^2C bidirectional data input/output. Si8902: SPI port serial data in.

Table 6. Si8900/1/2 Pin Assignments (Continued)

Pin	Si8900 Pin	Si8901 Pin	Si8902 Pin	Description
13	Rx	SCL	SCLK	Si8900: UART unidirectional receive input. Si8901: I^2C port unidirectional serial clock input. Si8902: SPI port unidirectional serial clock input.
14	NC		SDO	Si8900/1: No connection. Si8902: SPI port Serial data out (SDO)
15	NC			No connection
16	VDDB			Si8900/1/2: Output side VDD bias voltage (2.7 V to 5.5 V).

8. Ordering Guide

Table 7. Product Ordering Information[1,2]

Part Number (OPN)	Serial Port	Package	Isolation Rating	Temp Range
Si8900B-A01-GS	UART	WB SOIC	2.5 kV	–40 to +85 °C
Si8900D-A01-GS	UART	WB SOIC	5.0 kV	–40 to +85 °C
Si8901B-A02-GS	I^2C/SMBus	WB SOIC	2.5 kV	–40 to +85 °C
Si8901D-A02-GS	I^2C/SMBus	WB SOIC	5.0 kV	–40 to +85 °C
Si8902B-A01-GS	SPI Port	WB SOIC	2.5 kV	–40 to +85 °C
Si8902D-A01-GS	SPI Port	WB SOIC	5.0 kV	–40 to +85 °C

Notes:
1. Add an “R” suffix to the part number to specify the tape and reel option. Example: “Si8900AB-A-ISR”.
2. All packages are RoHS-compliant.

9. Package Outline: 16-Pin Wide Body SOIC

Figure 18 illustrates the package details for the Si8900/1/2 Digital Isolator. Table 8 lists the values for the dimensions shown in the illustration.

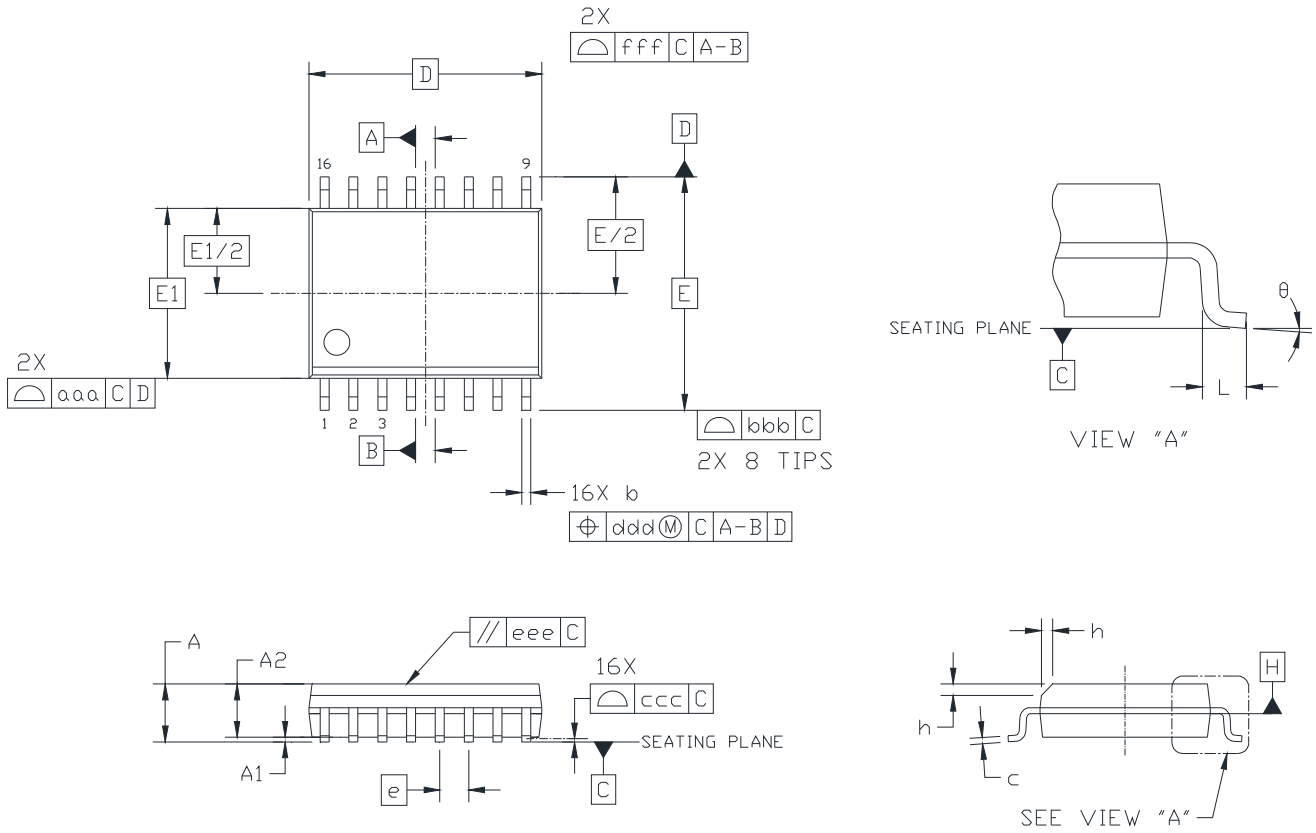


Figure 18. 16-Pin Wide Body SOIC

Table 8. Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	—	2.65
A1	0.10	0.30
A2	2.05	—
b	0.31	0.51
c	0.20	0.33
D	10.30 BSC	
E	10.30 BSC	
E1	7.50 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.75
θ	0°	8°
aaa	—	0.10
bbb	—	0.33
ccc	—	0.10
ddd	—	0.25
eee	—	0.10
fff	—	0.20

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MS-013, Variation AA.
4. Recommended reflow profile per JEDEC J-STD-020C specification for small body, lead-free components.

10. Land Pattern: 16-Pin Wide-Body SOIC

Figure 19 illustrates the recommended land pattern details for the Si8900/1/2 in a 16-pin wide-body SOIC. Table 9 lists the values for the dimensions shown in the illustration.

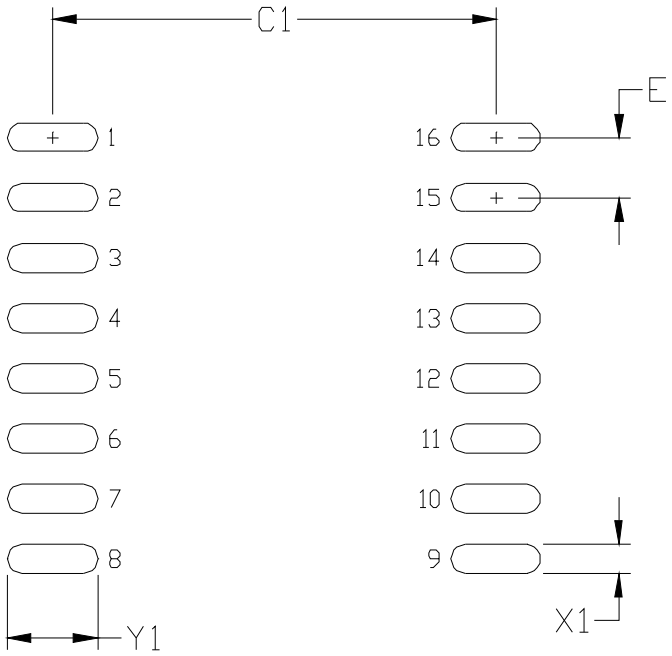


Figure 19. 16-Pin SOIC Land Pattern

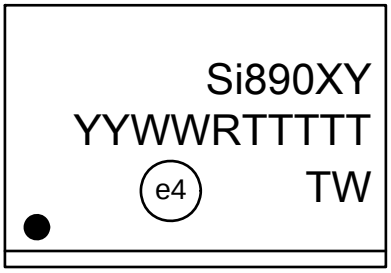
Table 9. 16-Pin Wide Body SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	9.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.90

Notes:
1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

11. Top Marking: 16-Pin Wide Body SOIC

11.1. Si8900/1/2 Top Marking



11.2. Top Marking Explanation

Line 1 Marking:	Base Part Number Ordering Options (See Ordering Guide for more information).	Si890 = Isolator product series X = Serial Port 0 = UART 1 = I^2C 2 = SPI Y = Insulation rating B = 2.5 kV; D = 5.0 kV
Line 2 Marking:	YY = Year WW = Workweek	Assigned by assembly subcontractor. Corresponds to the year and workweek of the mold date.
	RTTTTT = Mfg Code	Manufacturing code from assembly house “R” indicates revision
Line 3 Marking:	Circle = 1.7 mm Diameter (Center-Justified)	“e4” Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	TW = Taiwan

Document Change List

Revision 0.5 to Revision 1.0

- No changes.

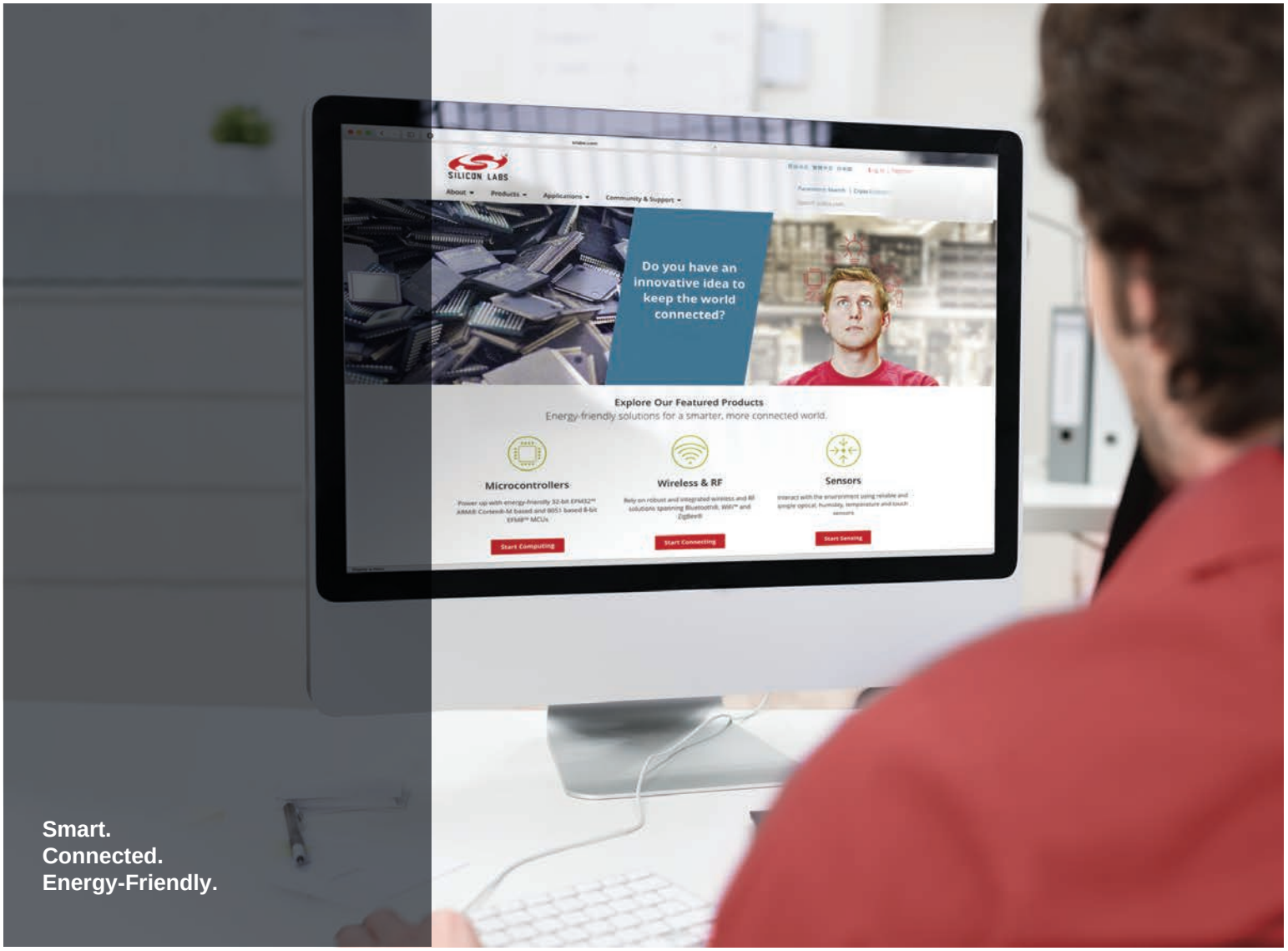
Revision 1.0 to Revision 1.1

- Removed “pending” throughout.
- Changed AN638 reference to AN637.
- Updated "11. Top Marking: 16-Pin Wide Body SOIC" on page 31.

Revision 1.1 to Revision 1.2

April, 2019

- Table 1, Changed GND1 to GNDA and GND2 to GNDB.
- Table 2, tconv changed from 2 µs to 2.5 µs.
- Table 2, Digital Outputs, changed min for Voh with VDDB=3.3 V to 3.1 V.
- Table 2, Digital Outputs, added typical for Voh with VDDB=3.3 V to 3.1 V.
- Table 2, Digital Outputs, changed specification name Digital Output Series Impedance to Digital Output Source Resistance.
- Table 2, Digital Outputs, changed typical source resistance from 85 Ω to 50 Ω typical.
- Table 2, Serial Ports, changed maximum UART Bit Rate from 234 kbps to 500 kbps.
- Table 2, Serial Ports, changed specification name SPI port to SPI Bit Rate.
- Table 2, Serial Ports, added test condition for SPI Port, Mode 3: CPOL=1, CPHA=1.
- Table 2, Serial Ports, changed maximum SPI Bit Rate from 2 mbps to 2.5 mbps.
- Table 3, Removed data from NB SOIC 16.
- Figure 2, Changed VDD1 and VDD2 to VDDA and VDDB.
- Table 5, Updated certification nomenclature for CSA from 61010-1 to 62368-1, up to 1000 VRMS basic insulation working voltage.
- Table 5, Updated certification nomenclature for VDE from IEC 60747-5-2 to VDE 0884-10.
- Removed Figure 3, NB SOIC 16 derating curve.
- Function Description, removed ADC option of internal voltage reference.
- Function Description, described $\overline{\text{RST}}$ and RSDA pin functions.
- Figure 4, Updated Si8902 GND pin names.
- ADC Data Transmission Modes, Updated description of Demand and Burst Modes.
- Figure 5, Showed tconv starting at the end of CNFG_0 byte for Si8901 Demand Mode.
- UART (Si8900), Changed name of AN635 from AC Line Monitoring to Si8900 Automatic Band Rate Detection.
- Figure 8A, Showed proper span of ADC data.
- Figure 11B and 11C, Added ACK bit between slave address and echo CNFG_0 byte.
- Figure 12, Removed $\overline{\text{EN}}$ signal from controlling SDO driver circuit.
- SPI Port (Si8902), Added requirement of SDI being held high during byte reads.
- SPI Port (Si8902), SDO does not enter Hi-Z state with $\overline{\text{EN}}$ function.
- Si8900/1/2 Configuration Registers, removed default setting from registers.
- Applications, Isolated Outputs, recommend a 10 nF capacitor from $\overline{\text{RST}}$ to GNDA for reliable reset on power cycle.
- Table 7, updated OPN for Si8901 from revision A01 to A02.
- Table 7, removed Note 3.



Products
www.silabs.com/products

Quality
www.silabs.com/quality

Support and Community
community.silabs.com

SILICON LABS

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

http://www.silabs.com

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Silicon Laboratories:

SI8901D-A01-GS SI890XPWR-KIT SI8900B-A01-GS SI8900B-A01-GSR SI8900D-A01-GS SI8900D-A01-GSR SI8902B-A01-GS SI8902B-A01-GSR SI8902D-A01-GS SI8902D-A01-GSR SI8901B-A01-GS SI8901B-A01-GSR SI8901D-A01-GSR