

Transistors

# 2.5V Drive Nch+Pch MOSFET

## QS6M4

●Structure

Silicon P-channel MOSFET  
Silicon N-channel MOSFET

●Features

- 1) The QS6M4 combines Pch MOSFET with a Nch MOSFET in a single TSMT6 package.
- 2) Low on-state resistance with a fast switching.
- 3) Low voltage drive (2.5V).

●Applications

Load switch, inverter

●Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
QS6M4		○

●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits		Unit
		Nchannel	Pchannel	
Drain-source voltage	V <sub>DSS</sub>	30	-20	V
Gate-source voltage	V <sub>GSS</sub>	±12	±12	V
Drain current	Continuous	I <sub>D</sub>	±1.5	A
	Pulsed	I <sub>DP</sub> *1	±6.0	A
Source current (Body diode)	Continuous	I <sub>S</sub>	0.8	A
	Pulsed	I <sub>SP</sub> *1	6.0	A
Total power dissipation	P <sub>D</sub> *2		1.25	W / TOTAL
			0.9	W / ELEMENT
Channel temperature	T <sub>ch</sub>		150	°C
Storage temperature	T <sub>stg</sub>		-55 to +150	°C

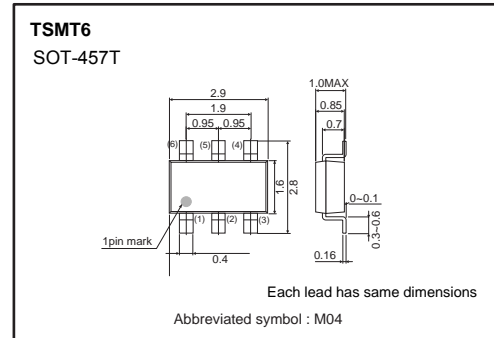
\*1 P<sub>WS</sub>≤10μs, Duty cycle≤1%  
\*2 Mounted on a ceramic board

●Thermal resistance

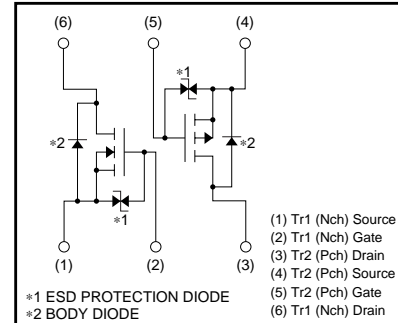
Parameter	Symbol	Limits	Unit
Channel to ambient	R <sub>th</sub> (ch-a) *	100	°C / W / TOTAL
		139	°C / W / ELEMENT

\* Mounted on a ceramic board

●Dimensions (Unit : mm)



●Equivalent circuit



Transistors

●Electrical characteristics (Ta=25°C)

<Tr1. N-ch MOSFET>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I <sub>GSS</sub>	–	–	±10	μA	V <sub>GS</sub> =±12V / V <sub>DS</sub> =0V
Drain-source breakdown voltage	V <sub>(BR) DSS</sub>	30	–	–	V	I <sub>D</sub> =1mA / V <sub>GS</sub> =0V
Zero gate voltage drain current	I <sub>DSS</sub>	–	–	1	μA	V <sub>DS</sub> =30V / V <sub>GS</sub> =0V
Gate threshold voltage	V <sub>GS(th)</sub>	0.5	–	1.5	V	V <sub>DS</sub> =10V / I <sub>D</sub> =1mA
Static drain-source on-state resistance	R <sub>DS(on)</sub> *	–	170	230	mΩ	I <sub>D</sub> =1.5A / V <sub>GS</sub> =4.5V
		–	180	245		I <sub>D</sub> =1.5A / V <sub>GS</sub> =4.0V
		–	260	360		I <sub>D</sub> =1.0A / V <sub>GS</sub> =2.5V
Forward transfer admittance	Y <sub>fs</sub>   *	1.0	–	–	S	V <sub>DS</sub> =10V / I <sub>D</sub> =1.0A
Input capacitance	C <sub>iss</sub>	–	80	–	pF	V <sub>DS</sub> =10V
Output capacitance	C <sub>oss</sub>	–	25	–	pF	V <sub>GS</sub> =0V
Reverse transfer capacitance	C <sub>rss</sub>	–	15	–	pF	f=1MHz
Turn-on delay time	t <sub>d(on)</sub> *	–	7	–	ns	I <sub>D</sub> =1A, V <sub>DD</sub> ≐15V
Rise time	t <sub>r</sub> *	–	18	–	ns	V <sub>GS</sub> =4.5V
Turn-off delay time	t <sub>d(off)</sub> *	–	15	–	ns	R <sub>L</sub> =15Ω / R <sub>G</sub> =10Ω
Fall time	t <sub>f</sub> *	–	15	–	ns	
Total gate charge	Q <sub>g</sub> *	–	1.6	–	nC	V <sub>DD</sub> ≐15V R <sub>L</sub> =10Ω
Gate-source charge	Q <sub>gs</sub> *	–	0.5	–	nC	V <sub>GS</sub> =4.5V R <sub>G</sub> =10Ω
Gate-drain charge	Q <sub>gd</sub> *	–	0.9	–	nC	I <sub>D</sub> =1.5A

\*Pulsed

●Body diode characteristics (Source-Drain)

<Tr1. N-ch MOSFET>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V <sub>SD</sub> *	–	–	1.2	V	I <sub>S</sub> =3.2A / V <sub>GS</sub> =0V

\*Pulsed

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●Electrical characteristics (Ta=25°C)

<Tr2. P-ch MOSFET>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I <sub>gss</sub>	–	–	±10	μA	V <sub>GS</sub> = ±12V / V <sub>DS</sub> =0V
Drain-source breakdown voltage	V <sub>(BR) DSS</sub>	–20	–	–	V	I <sub>D</sub> = –1mA / V <sub>GS</sub> =0V
Zero gate voltage drain current	I <sub>DSS</sub>	–	–	–1	μA	V <sub>DS</sub> = –20V / V <sub>GS</sub> =0V
Gate threshold voltage	V <sub>GS(th)</sub>	–0.7	–	–2.0	V	V <sub>DS</sub> = –10V / I <sub>D</sub> =–1mA
Static drain-source on-state resistance	R <sub>DS(on)</sub> *	–	155	215	mΩ	I <sub>D</sub> = –1.5A / V <sub>GS</sub> = –4.5V
		–	170	235		I <sub>D</sub> = –1.5A / V <sub>GS</sub> = –4.0V
		–	310	430		I <sub>D</sub> = –0.75A / V <sub>GS</sub> = –2.5V
Forward transfer admittance	Y <sub>fs</sub>   *	1.0	–	–	S	V <sub>DS</sub> = –10V / I <sub>D</sub> = –0.75A
Input capacitance	C <sub>iss</sub>	–	270	–	pF	V <sub>DS</sub> = –10V
Output capacitance	C <sub>oss</sub>	–	40	–	pF	V <sub>GS</sub> =0V
Reverse transfer capacitance	C <sub>rss</sub>	–	35	–	pF	f=1MHz
Turn-on delay time	t <sub>d(on)</sub> *	–	10	–	ns	I <sub>D</sub> = –0.75A, V <sub>DD</sub> ≐ –15V
Rise time	t <sub>r</sub> *	–	12	–	ns	V <sub>GS</sub> = –4.5V
Turn-off delay time	t <sub>d(off)</sub> *	–	45	–	ns	R <sub>L</sub> =20Ω / R <sub>G</sub> =10Ω
Fall time	t <sub>f</sub> *	–	20	–	ns	
Total gate charge	Q <sub>g</sub> *	–	3.0	–	nC	V <sub>DD</sub> ≐ –15V R <sub>L</sub> =10Ω
Gate-source charge	Q <sub>gs</sub> *	–	0.8	–	nC	V <sub>GS</sub> = –4.5V R <sub>G</sub> =10Ω
Gate-drain charge	Q <sub>gd</sub> *	–	0.85	–	nC	I <sub>D</sub> = –1.5A

\*Pulsed

●Body diode characteristics (Source-Drain)

<Tr2. P-ch MOSFET>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V <sub>SD</sub>	–	–	–1.2	V	I <sub>S</sub> = –0.75A / V <sub>GS</sub> =0V

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N-ch

●Electrical characteristic curves

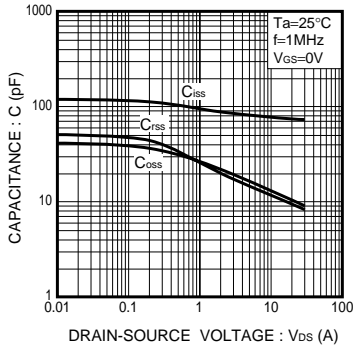


Fig.1 Typical Capacitance vs. Drain-Source Voltage

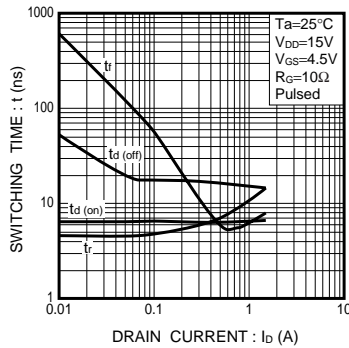


Fig.2 Switching Characteristics

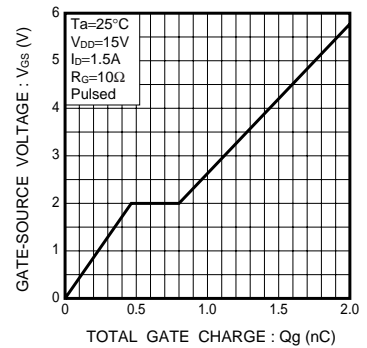


Fig.3 Dynamic Input Characteristics

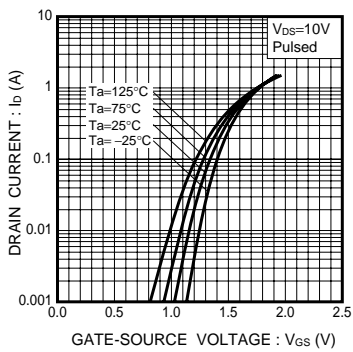


Fig.4 Typical Transfer Characteristics

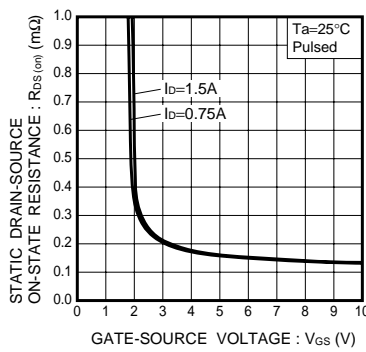


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

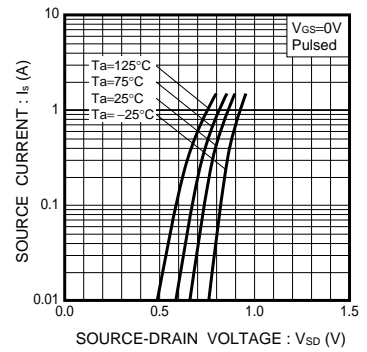


Fig.6 Source Current vs. Source-Drain Voltage

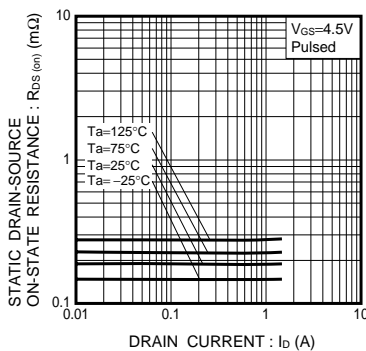


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (I)

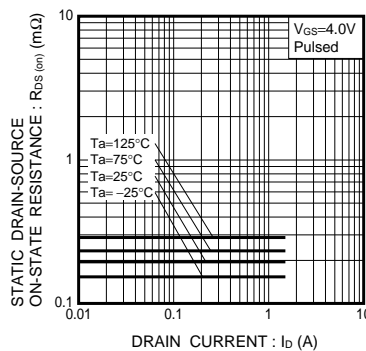


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (II)

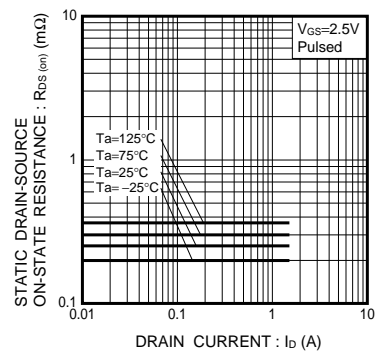


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current (III)

Transistors

P-ch

●Electrical characteristic curves

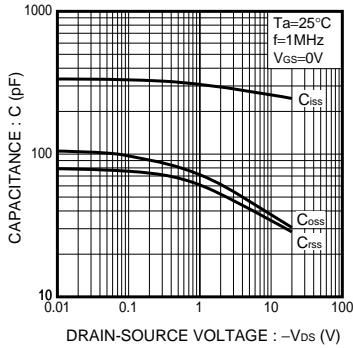


Fig.1 Typical Capacitance vs. Drain-Source Voltage

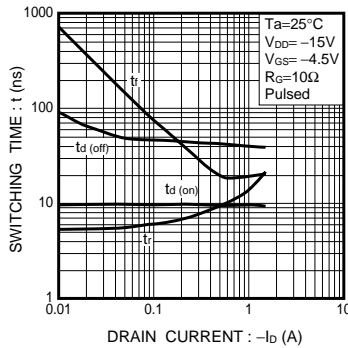


Fig.2 Switching Characteristics

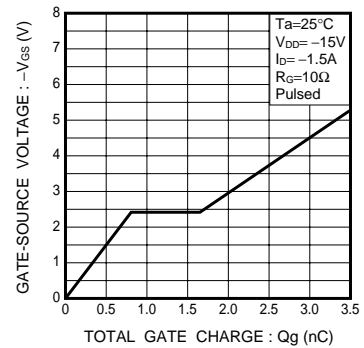


Fig.3 Dynamic Input Characteristics

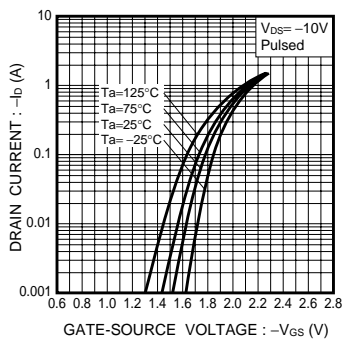


Fig.4 Typical Transfer Characteristics

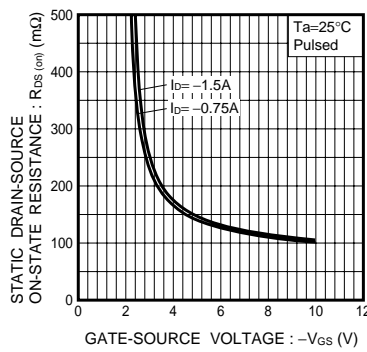


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

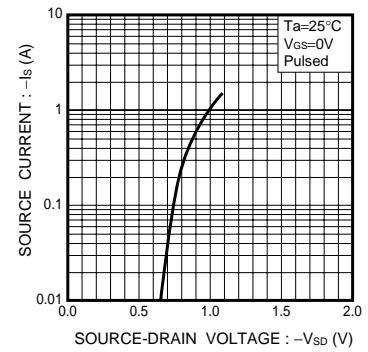


Fig.6 Source Current vs. Source-Drain Voltage

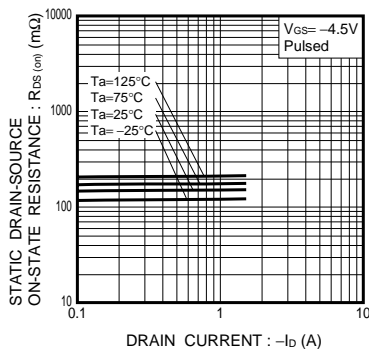


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (I)

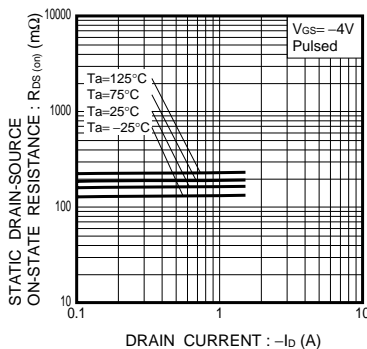


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (II)

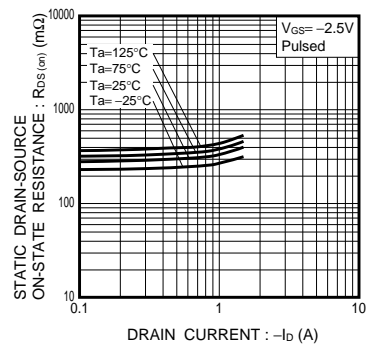


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current (III)

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