

**FEATURES**

- 2.4 pF typical off switch source capacitance, dual supply
- <1 pC charge injection
- Low leakage: 0.6 nA maximum at 85°C
- 120  $\Omega$  typical on resistance at 25°C, dual supply
- Fully specified at  $\pm 15$  V, +12 V
- No  $V_L$  supply required
- 3 V logic-compatible inputs
  - $V_{INH} = 2.0$  V minimum
  - $V_{INL} = 0.8$  V maximum
- Rail-to-rail operation
- 6-lead SOT-23 package

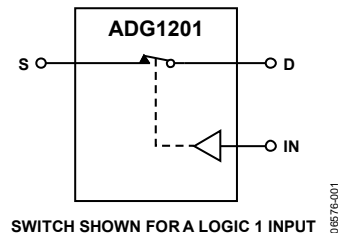
**APPLICATIONS**

- Automatic test equipment
- Data acquisition systems
- Battery-powered systems
- Sample-and-hold systems
- Audio signal routing
- Video signal routing
- Communication systems

**GENERAL DESCRIPTION**

The ADG1201 is a monolithic complementary metal-oxide semiconductor (CMOS) device containing a single-pole, single-throw (SPST) switch designed in an *i*CMOS® process. *i*CMOS is a modular manufacturing process combining a high voltage CMOS and bipolar technologies. *i*CMOS enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no previous generation of high voltage devices has been able to achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can tolerate high supply voltages while providing increased performance, dramatically lower power consumption, and reduced package size.

The ultralow capacitance and charge injection of this switch makes it an ideal solution for data acquisition and sample-and-hold applications, where low glitch and fast settling are required. Fast switching speed coupled with high signal bandwidth also makes the device suitable for video signal switching.

**FUNCTIONAL BLOCK DIAGRAM**

SWITCH SHOWN FOR A LOGIC 1 INPUT

Figure 1.

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*i*CMOS construction ensures ultra low power dissipation, making the device ideally suited for portable and battery-powered instruments.

The ADG1201 contains a SPST switch. Figure 1 shows that with a logic input of 1, the switch of the ADG1201 is closed. The switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked.

**PRODUCT HIGHLIGHTS**

1. Ultralow capacitance.
2. <1 pC charge injection.
3. Ultralow leakage.
4. 3 V logic-compatible digital inputs:  
 $V_{INH} = 2.0$  V minimum,  $V_{INL} = 0.8$  V maximum.
5. No logic voltage ( $V_L$ ) power supply required.
6. SOT-23 package.

**Rev. A****Document Feedback**

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**TABLE OF CONTENTS**

Features .....	1	Absolute Maximum Ratings .....	6
Applications.....	1	Thermal Resistance.....	6
Functional Block Diagram .....	1	ESD Caution.....	6
General Description .....	1	Pin Configuration and Function Descriptions.....	7
Product Highlights .....	1	Typical Performance Characteristics .....	8
Revision History .....	2	Test Circuits.....	11
Specifications.....	3	Terminology.....	13
Dual Supply .....	3	Outline Dimensions .....	14
Single Supply .....	4	Ordering Guide .....	14

**REVISION HISTORY**

**1/2019—Rev. 0 to Rev. A**

Deleted ADG1202 .....	Universal
Changes to Features Section and Product Highlights Section ...	1
Changes to Table 1 .....	3
Changes to Absolute Maximum Ratings Section and Table 3 ....	6
Added Thermal Resistance Section .....	6
Added Table 4; Renumbered Sequentially .....	6
Changes to Figure 3 Caption to Figure 8 Caption.....	8
Changes to Figure 9 Caption, Figure 10 Caption, and Figure 11 Caption .....	9
Changes to Figure 15 Caption and Figure 19 Caption .....	10
Changes to Figure 26 and Figure 27.....	12
Changes to Ordering Guide .....	14

**2/2008—Revision 0: Initial Version**

# SPECIFICATIONS

## DUAL SUPPLY

$V_{DD} = 15\text{ V} \pm 10\%$ ,  $V_{SS} = -15\text{ V} \pm 10\%$ , GND = 0 V, unless otherwise noted.

Table 1.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			$V_{DD}$ to $V_{SS}$	V	
On Resistance ( $R_{ON}$ )	120			$\Omega$ typ	$V_{DD} = +13.5\text{ V}$ , $V_{SS} = -13.5\text{ V}$
	200	240	270	$\Omega$ max	Analog voltage on Terminal S ( $V_S$ ) = $\pm 10\text{ V}$ , source leakage current ( $I_S$ ) = -1 mA, see Figure 20
On Resistance Flatness ( $R_{FLAT(ON)}$ )	20			$\Omega$ typ	$V_S = -5\text{ V}$ , 0 V, and +5 V, $I_S = -1\text{ mA}$
	60	72	79	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage ( $I_S$ (Off))	$\pm 0.004$			nA typ	$V_{DD} = +16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$ $V_S = \pm 10\text{ V}$ , analog voltage on Terminal D ( $V_D$ ) = $\pm 10\text{ V}$ , see Figure 21
Drain Off Leakage ( $I_D$ (Off))	$\pm 0.1$	$\pm 0.6$	$\pm 1$	nA max	
	$\pm 0.004$			nA typ	$V_S = \pm 10\text{ V}$ , $V_D = \pm 10\text{ V}$ , see Figure 21
Channel On Leakage ( $I_D$ , $I_S$ (On))	$\pm 0.1$	$\pm 0.6$	$\pm 1$	nA max	
	$\pm 0.04$			nA typ	$V_S = V_D = \pm 10\text{ V}$ , see Figure 22
	$\pm 0.15$	$\pm 0.6$	$\pm 1$	nA max	
<b>DIGITAL INPUTS</b>					
Input High Voltage ( $V_{INH}$ )			2.0	V min	
Input Low Voltage ( $V_{INL}$ )			0.8	V max	
Input Current ( $I_{INL}$ or $I_{INH}$ )	0.005			$\mu\text{A}$ typ	Voltage on IN pin ( $V_{IN}$ ) = $V_{INL}$ or $V_{INH}$
			$\pm 0.1$	$\mu\text{A}$ max	
Digital Input Capacitance ( $C_{IN}$ )	2.5			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
On Time ( $t_{ON}$ )	140			ns typ	Load resistance ( $R_L$ ) = 300 $\Omega$ , load capacitance ( $C_L$ ) = 35 pF
	170	200	230	ns max	$V_S = 10\text{ V}$ , see Figure 26
Off Time ( $t_{OFF}$ )	90			ns typ	$R_L = 300\text{ }\Omega$ , $C_L = 35\text{ pF}$
	105	130	141	ns max	$V_S = 10\text{ V}$ , see Figure 26
Charge Injection	-0.8			pC typ	$V_S = 0\text{ V}$ , supply resistance ( $R_S$ ) = 0 $\Omega$ , $C_L = 1\text{ nF}$ , see Figure 27
Off Isolation	80			dB typ	$R_L = 50\text{ }\Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ , see Figure 23
Total Harmonic Distortion + Noise (THD + N)	0.15			% typ	$R_L = 10\text{ k}\Omega$ , 5 V rms, $f = 20\text{ Hz}$ to 20 kHz
-3 dB Bandwidth	660			MHz typ	$R_L = 50\text{ }\Omega$ , $C_L = 5\text{ pF}$ , see Figure 24
Off Switch Source Capacitance ( $C_S$ (Off))	2.4			pF typ	$V_S = 0\text{ V}$ , frequency = 1 MHz
	3			pF max	$V_S = 0\text{ V}$ , frequency = 1 MHz
Off Switch Drain Capacitance ( $C_D$ (Off))	2.8			pF typ	$V_S = 0\text{ V}$ , frequency = 1 MHz
	3.3			pF max	$V_S = 0\text{ V}$ , frequency = 1 MHz
On Switch Capacitance ( $C_D$ , $C_S$ (On))	4.7			pF typ	$V_S = 0\text{ V}$ , frequency = 1 MHz
	5.6			pF max	$V_S = 0\text{ V}$ , frequency = 1 MHz

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>POWER REQUIREMENTS</b>					
Positive Supply Current ( $I_{DD}$ )	0.001		1.0	$\mu\text{A typ}$ $\mu\text{A max}$	$V_{DD} = +16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$ Digital inputs = 0 V or $V_{DD}$
$I_{DD}$	60		95	$\mu\text{A typ}$ $\mu\text{A max}$	Digital inputs = 5 V
Negative Supply Current ( $I_{SS}$ )	0.001		1.0	$\mu\text{A typ}$ $\mu\text{A max}$	Digital inputs = 0 V, 5 V, or $V_{DD}$
$V_{DD}/V_{SS}$			$\pm 5$ to $\pm 16.5$	V min/max	GND = 0 V

<sup>1</sup> Guaranteed by design, not subject to production test.

## SINGLE SUPPLY

$V_{DD} = 12\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ , GND = 0 V, unless otherwise noted.

Table 2.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	
$R_{ON}$	300			$\Omega$ typ	$V_{DD} = 10.8\text{ V}$ , $V_{SS} = 0\text{ V}$
	475	567	625	$\Omega$ max	$V_S = 0\text{ V}$ to 10 V, $I_S = -1\text{ mA}$ , see Figure 20
$R_{FLAT(ON)}$	60			$\Omega$ typ	$V_S = 3\text{ V}$ , 6 V, and 9 V, $I_S = -1\text{ mA}$
<b>LEAKAGE CURRENTS</b>					
$I_S$ (Off)	$\pm 0.006$			nA typ	$V_{DD} = 13.2\text{ V}$ , $V_{SS} = 0\text{ V}$
	$\pm 0.1$	$\pm 0.6$	$\pm 1$	nA max	$V_S = 1\text{ V}$ or 10 V, $V_D = 10\text{ V}$ or 1 V, see Figure 21
$I_D$ (Off)	$\pm 0.006$			nA typ	$V_S = 1\text{ V}$ or 10 V, $V_D = 10\text{ V}$ or 1 V, see Figure 21
	$\pm 0.1$	$\pm 0.6$	$\pm 1$	nA max	
$I_D, I_S$ (On)	$\pm 0.04$			nA typ	$V_S = V_D = 1\text{ V}$ or 10 V, see Figure 22
	$\pm 0.15$	$\pm 0.6$	$\pm 1$	nA max	
<b>DIGITAL INPUTS</b>					
$V_{INH}$			2.0	V min	
$V_{INL}$			0.8	V max	
$I_{INL}$ or $I_{INH}$	0.001			$\mu\text{A typ}$ $\mu\text{A max}$	$V_{IN} = V_{INL}$ or $V_{INH}$
$C_{IN}$	3			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
$t_{ON}$	190			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	250	295	340	ns max	$V_S = 8\text{ V}$ , see Figure 26
$t_{OFF}$	120			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	155	190	210	ns max	$V_S = 8\text{ V}$ , see Figure 26
Charge Injection	0.8			pC typ	$V_S = 6\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ , see Figure 27
Off Isolation	80			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , frequency = 1 MHz, see Figure 23
-3 dB Bandwidth	520			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , see Figure 24
$C_S$ (Off)	2.7			pF typ	$V_S = 6\text{ V}$ , frequency = 1 MHz
	3.3			pF max	$V_S = 6\text{ V}$ , frequency = 1 MHz
$C_D$ (Off)	3.1			pF typ	$V_S = 6\text{ V}$ , frequency = 1 MHz
	3.6			pF max	$V_S = 6\text{ V}$ , frequency = 1 MHz
$C_D, C_S$ (On)	5.3			pF typ	$V_S = 6\text{ V}$ , frequency = 1 MHz
	6.3			pF max	$V_S = 6\text{ V}$ , frequency = 1 MHz

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					$V_{DD} = 13.2\text{ V}$
$I_{DD}$	0.001		1.0	$\mu\text{A typ}$	Digital inputs = 0 V or $V_{DD}$
$I_{DD}$	60		95	$\mu\text{A max}$	Digital inputs = 5 V
$V_{DD}$			5 to 16.5	$\mu\text{A max}$	$V_{SS} = 0\text{ V}, \text{GND} = 0\text{ V}$
				V min/max	

<sup>1</sup> Guaranteed by design, not subject to production test.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 3.

Parameter	Rating
$V_{DD}$ to $V_{SS}$	35 V
$V_{DD}$ to GND	-0.3 V to +25 V
$V_{SS}$ to GND	+0.3 V to -25 V
Analog Inputs <sup>1</sup>	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Digital Inputs <sup>1</sup>	GND - 0.3 V to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Peak Current, S or D	100 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current per Channel, S or D	30 mA
Temperature	
Industrial Range	-40°C to +125°C
Storage Range	-65°C to +150°C
Junction	150°C
Reflow Soldering Peak, Pb- Free	260°C

<sup>1</sup> Overvoltages at IN, S, or D are clamped by internal diodes. Current must be limited to the maximum ratings given.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

$\theta_{JA}$  is the natural convection, junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.  $\theta_{JC}$  is the junction to case thermal resistance.

Table 4. Thermal Resistance

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
RJ-6 <sup>1</sup>	229.6	91.99	°C/W

<sup>1</sup> Thermal impedance values measured on a JEDEC 152P thermal test board. See JEDEC JESD-51.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

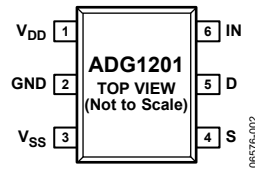


Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V <sub>DD</sub>	Most Positive Power Supply Potential.
2	GND	Ground (0 V) Reference.
3	V <sub>SS</sub>	Most Negative Power Supply Potential.
4	S	Source Terminal. This pin can be an input or output.
5	D	Drain Terminal. This pin can be an input or output.
6	IN	Logic Control Input.

Table 6. ADG1201 Truth Table

IN	Switch Condition
1	On
0	Off

TYPICAL PERFORMANCE CHARACTERISTICS

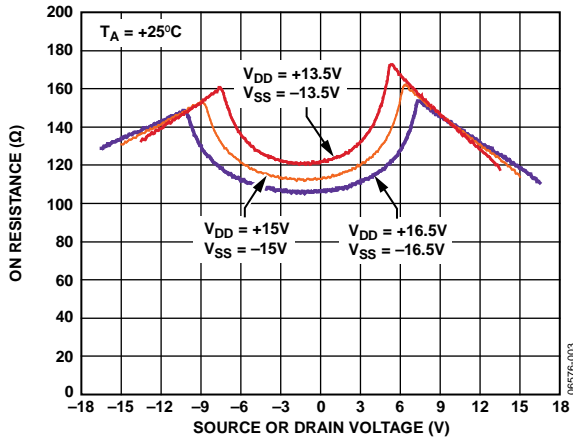


Figure 3. On Resistance vs. Source or Drain Voltage, Dual Supply

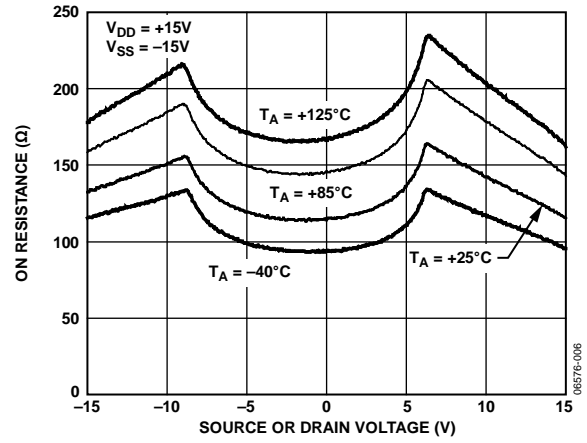


Figure 6. On Resistance vs. Source or Drain Voltage, Different Temperatures, Dual Supply

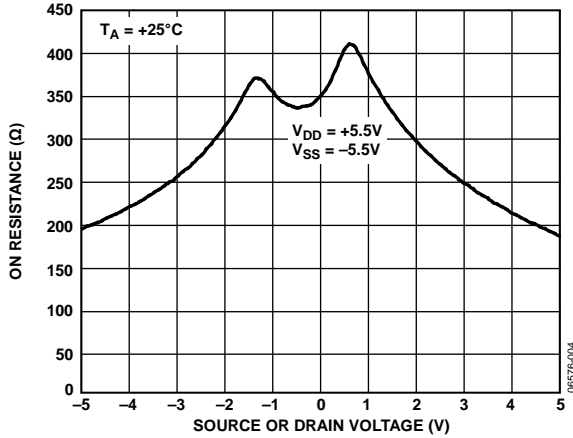


Figure 4. On Resistance vs. Source or Drain Voltage, Dual Supply

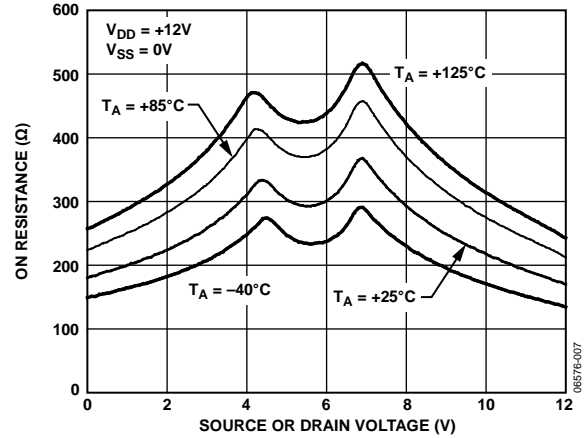


Figure 7. On Resistance vs. Source or Drain Voltage, Different Temperatures, Single Supply

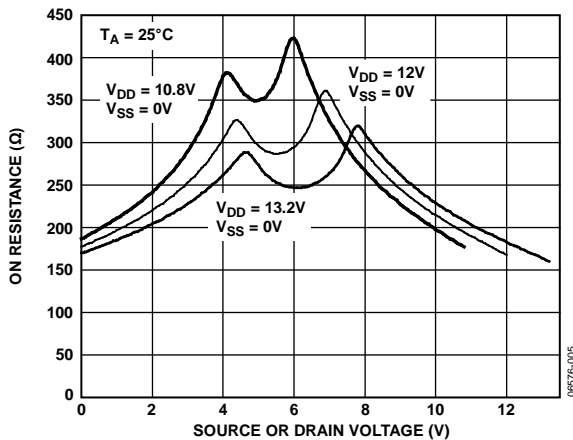


Figure 5. On Resistance vs. Source or Drain Voltage, Single Supply

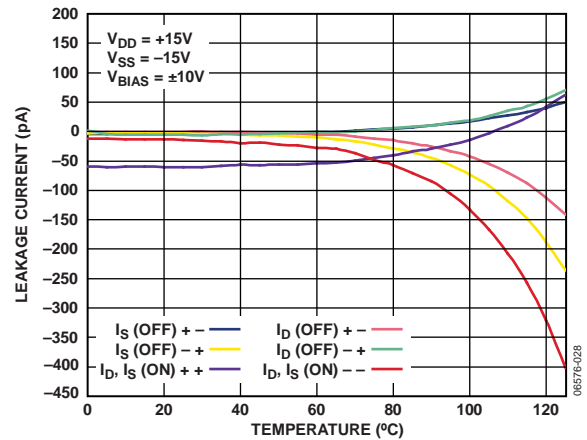


Figure 8. Leakage Current vs. Temperature, Dual Supply



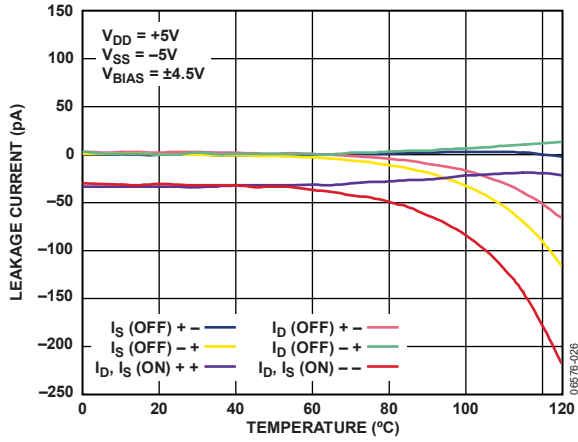


Figure 9. Leakage Currents vs. Temperature, Dual Supply

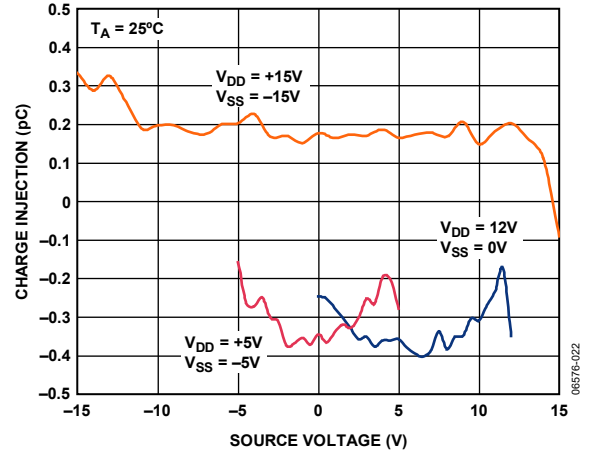


Figure 12. Charge Injection vs. Source Voltage

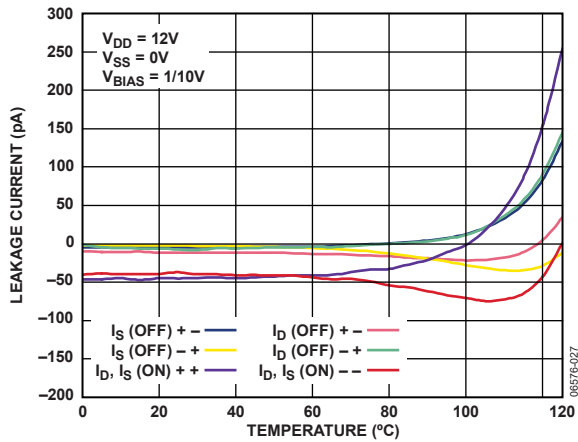


Figure 10. Leakage Currents vs. Temperature, Single Supply

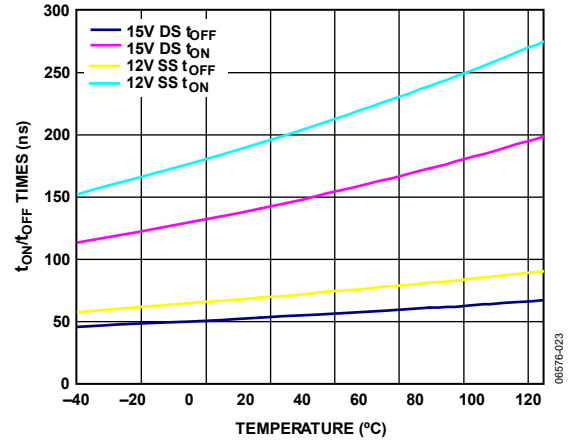


Figure 13.  $t_{ON}/t_{OFF}$  Times vs. Temperature

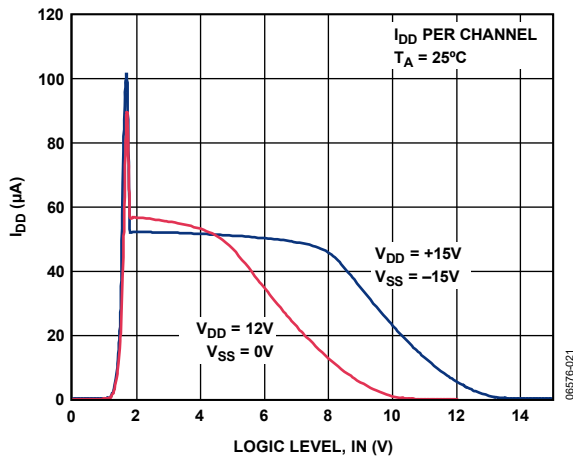


Figure 11.  $I_{DD}$  vs. Logic Level, IN

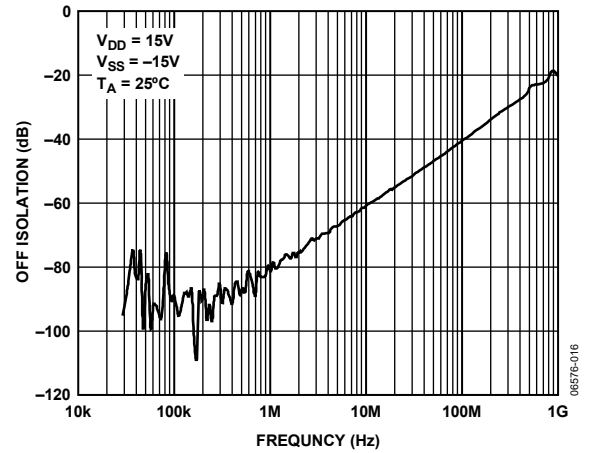


Figure 14. Off Isolation vs. Frequency

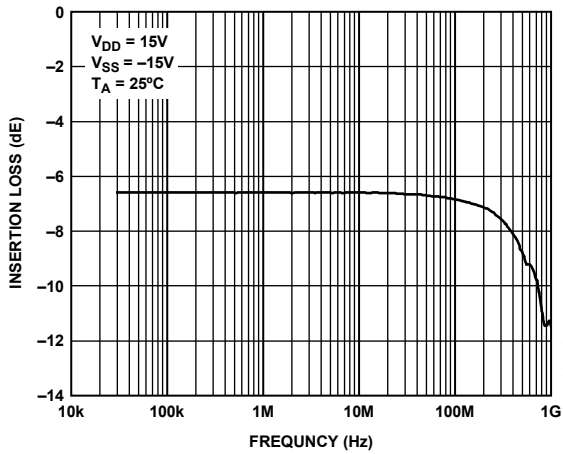


Figure 15. Insertion Loss vs. Frequency

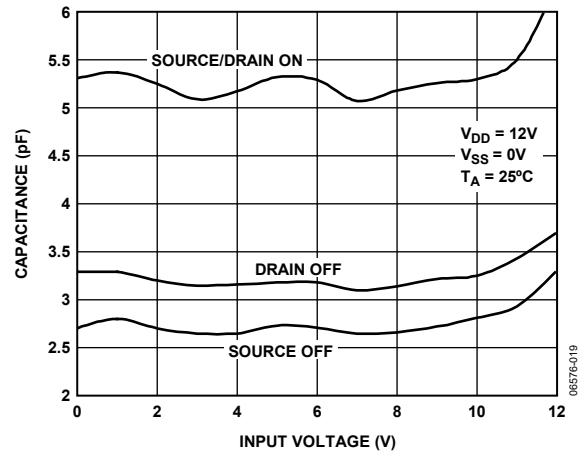


Figure 18. Capacitance vs. Input Voltage, Single Supply

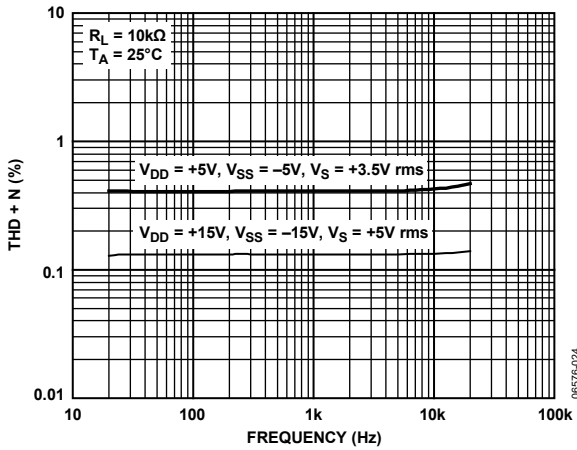


Figure 16. THD + N vs. Frequency

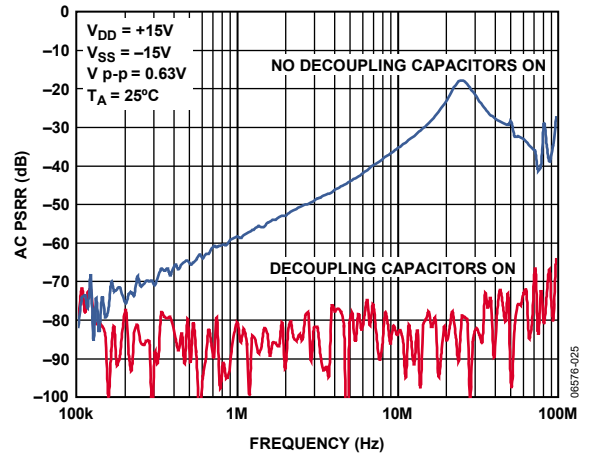


Figure 19. AC Power Supply Rejection Ratio (AC PSRR) vs. Frequency

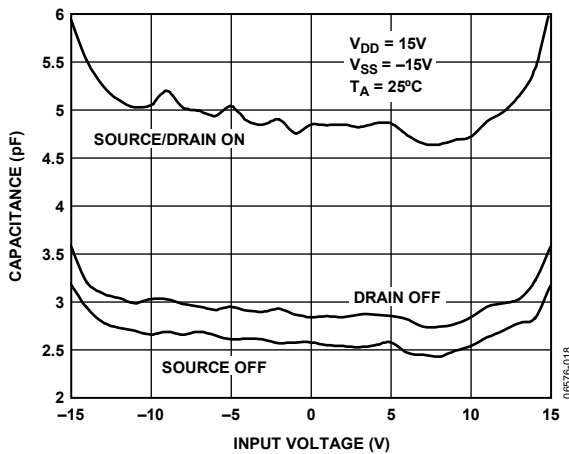


Figure 17. Capacitance vs. Input Voltage, Dual Supply

TEST CIRCUITS

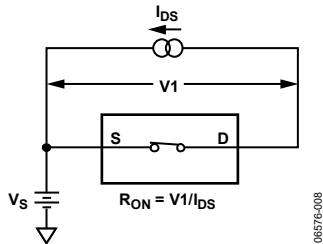


Figure 20. On Resistance

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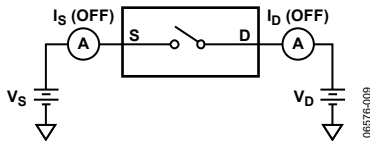


Figure 21. Off Leakage

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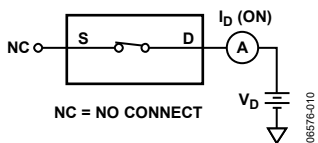


Figure 22. On Leakage

06576-010

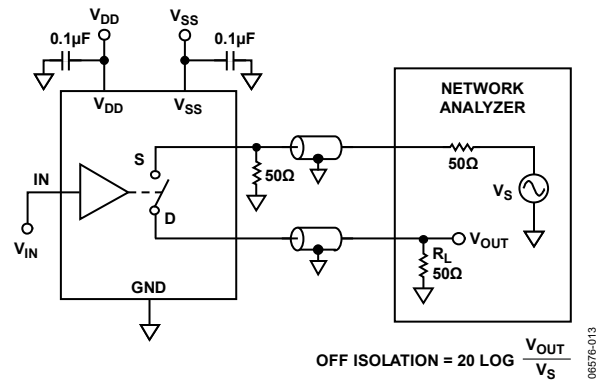


Figure 23. Off Isolation

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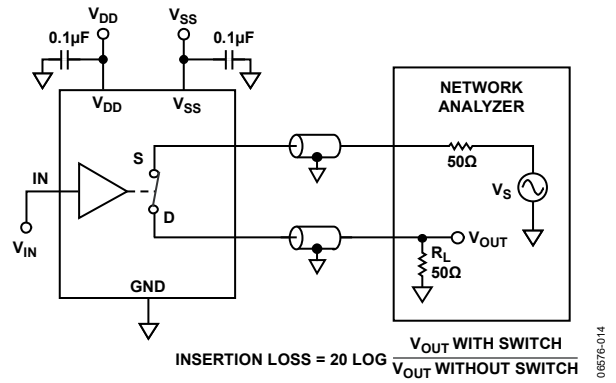


Figure 24. Bandwidth

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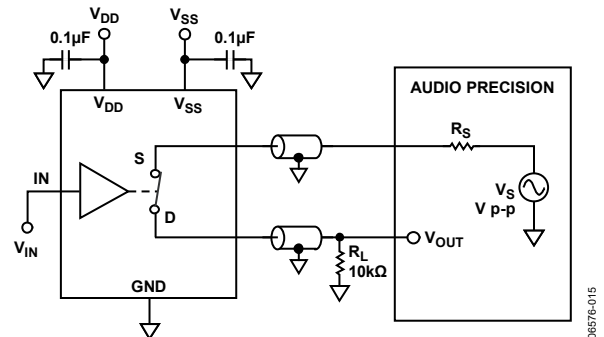


Figure 25. THD + N

06576-015

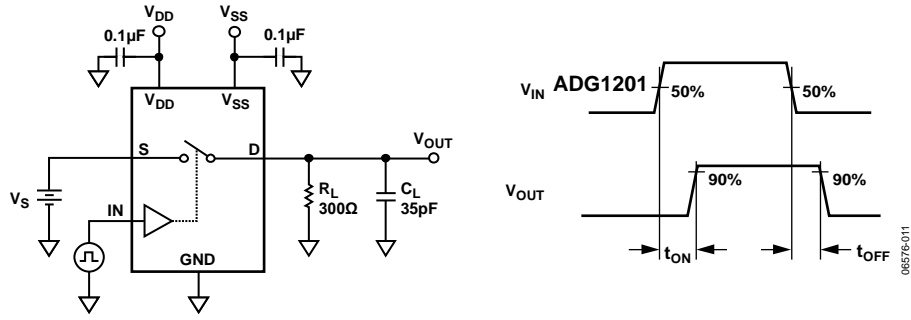


Figure 26. Switching Times

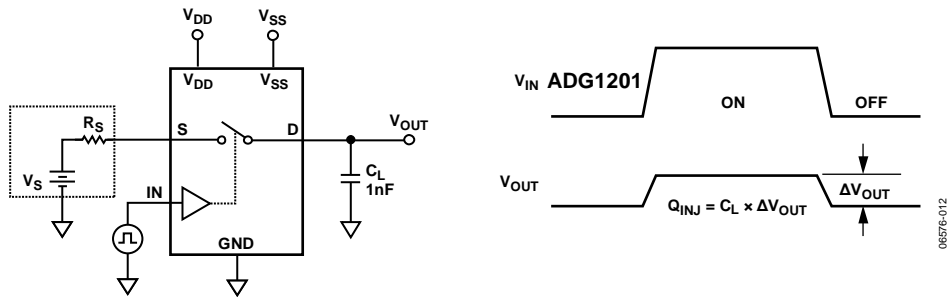


Figure 27. Charge Injection

## TERMINOLOGY

### $I_{DD}$

The positive supply current.

### $I_{SS}$

The negative supply current.

### $V_D$ ( $V_S$ )

The analog voltage on Terminal D and Terminal S.

### $R_{ON}$

The ohmic resistance between D and S.

### $R_{FLAT(ON)}$

Flatness is defined as the difference between the maximum and minimum value of on resistance, as measured over the specified analog signal range.

### $I_S$ (Off)

The source leakage current with the switch off.

### $I_D$ (Off)

The drain leakage current with the switch off.

### $I_D, I_S$ (On)

The channel leakage current with the switch on.

### $V_{INL}$

The maximum input voltage for Logic 0.

### $V_{INH}$

The minimum input voltage for Logic 1.

### $I_{INL}$ ( $I_{INH}$ )

The input current of the digital input.

### $C_S$ (Off)

The off switch source capacitance, measured with reference to ground.

### $C_D$ (Off)

The off switch drain capacitance, measured with reference to ground.

### $C_D, C_S$ (On)

The on switch capacitance, measured with reference to ground.

### $C_{IN}$

The digital input capacitance.

### $t_{ON}$

The delay between applying the digital control input and the output switching on. See Figure 26.

### $t_{OFF}$

The delay between applying the digital control input and the output switching off. See Figure 26.

### Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

### Off Isolation

A measure of unwanted signal coupling through an off switch.

### Crosstalk

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

### Bandwidth

The frequency at which the output is attenuated by 3 dB.

### On Response

The frequency response of the on switch.

### Insertion Loss

The loss due to the on resistance of the switch.

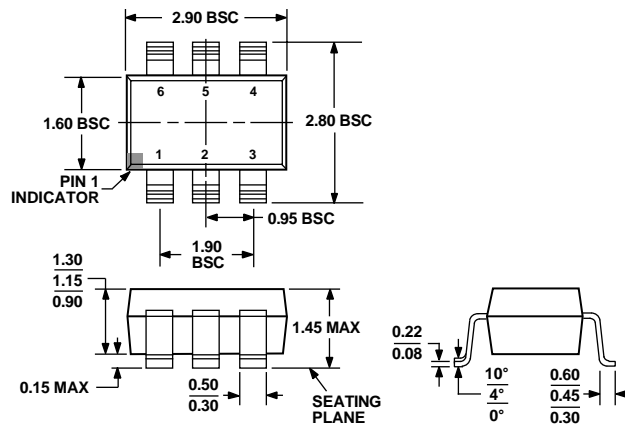
### THD + N

The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

### AC Power Supply Rejection Ratio (AC PSRR)

AC PSRR measures the ability of a device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of signal on the output to the amplitude of the modulation is the AC PSRR.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-178-AB

Figure 28. 6-Lead Small Outline Transistor Package [SOT-23] (RJ-6)  
Dimensions shown in millimeters

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Model <sup>1</sup>	Temperature Range	Package Description	Package Option	Marking Code
ADG1201BRJZ-R2	-40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	S25
ADG1201BRJZ-REEL7	-40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	S25

<sup>1</sup> Z = RoHS Compliant Part.

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