Fully Integrated, 8-Channel Ultrasound Analog Front End with Passive CW Mixer, 1.05 nV/rtHz, 12-Bit, 80 MSPS, 117 mW/CH

Check for Samples: AFE5807

FEATURES

- **8-Channel Complete Analog Front-End**
  - **LNA, VCAT, PGA, LPF, ADC, and CW Mixer**
- **Programmable Gain Low-Noise Amplifier (LNA)**
  - **24/18/12 dB Gain**
  - **0.25/0.5/1 V_{PP} Linear Input Range**
  - **0.63/0.7/0.9 nV/rtHz IRN (Low Noise Mode)**
  - **0.99/1.0/1.05 nV/rtHz IRN (Low Power Mode)**
  - **Programmable Active Termination**
- **40 dB Low Noise Voltage Controlled Attenuator (VCAT)**
- **24/30 dB Programmable Gain Amplifier (PGA)**
- **3rd Order Linear Phase Low-Pass Filter (LPF)**
  - **10, 15, 20, 30 MHz**
- **12-bit Analog to Digital Converter (ADC)**
  - **70 dBFS SNR at 80 MSPS**
  - **LVDS Outputs**
- **Noise/Power Optimizations (Full Chain)**
  - **117 mW/CH at 1.05 nV/rtHz, 80 MSPS**
  - **159 mW/CH at 0.75 nV/rtHz, 80 MSPS**
  - **80 mW/CH at CW Mode**
- **Excellent Device-to-Device Gain Matching**
  - **±0.5 dB(typical) and ±1 dB(max)**
- **Low Harmonic Distortion**
- **Fast and Consistent Overload Recovery**
- **Passive Mixer for Continuous Wave Doppler(CWD)**
  - **Low Close-in Phase Noise –156 dBc/Hz at 1 KHz off 2.5 MHz Carrier**
  - **Phase Resolution of 1/16λ**
  - **Support 16X, 8X, 4X and 1X CW Clocks**
  - **12dB Suppression on 3rd and 5th Harmonics**
  - **Flexible Input Clocks**
- **Small Package: 15 mm x 9 mm, 135-BGA**

APPLICATIONS

- **Medical Ultrasound Imaging**
- **Nondestructive Evaluation Equipments**

DESCRIPTION

The AFE5807 is an integrated Analog Front-End (AFE) solution specifically designed for ultrasound systems in which high performance and small size are required. The AFE5807 integrates a complete time-gain-control (TGC) imaging path and a continuous wave Doppler (CWD) path. It also enables users to select one of various power/noise combinations to optimize system performance. Therefore, the AFE5807 is a suitable ultrasound analog front end solution not only for high-end systems, but also for portable systems.

The AFE5807 contains eight channels of voltage controlled amplifier (VCA), 12-bit Analog-to-Digital Converter (ADC), and CW mixer. The VCA includes Low noise Amplifier (LNA), Voltage controlled Attenuator(VCAT), Programmable Gain Amplifier (PGA), and Low-Pass Filter (LPF). The LNA gain is programmable to support 250 mV_{PP} to 1 V_{PP} input signals. Programmable active termination is also supported by the LNA. The ultra-low noise VCAT provides an attenuation control range of 40 dB and improves overall low gain SNR which benefits harmonic imaging and near field imaging. The PGA provides gain options of 24 dB and 30 dB. Before the ADC, a LPF can be configured as 10 MHz, 15 MHz, 20 MHz or 30 MHz to support ultrasound applications with different frequencies. The high-performance 12 bit/80 MSPS ADC in the AFE5807 achieves 70 dBFS SNR. It ensures excellent SNR at low chain gain. The ADC's LVDS outputs enable flexible system integration desired for miniaturized systems. The AFE5807 also integrates a low power passive mixer and a low noise summing amplifier to accomplish on-chip CWD beamformer. 16 selectable phase-delays can be applied to each analog input signal. Meanwhile a unique 3rd and 5th order harmonic suppression filter is implemented to enhance CW sensitivity.

The AFE5807 is available in a 15mm × 9mm, 135-pin BGA package and it is specified for operation from 0°C to 85°C. It is also pin-to-pin compatible to the AFE5808, AFE5803, and AFE5808A. In addtion, AFE5809 is another member with enhanced digital demodulation features in this family.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

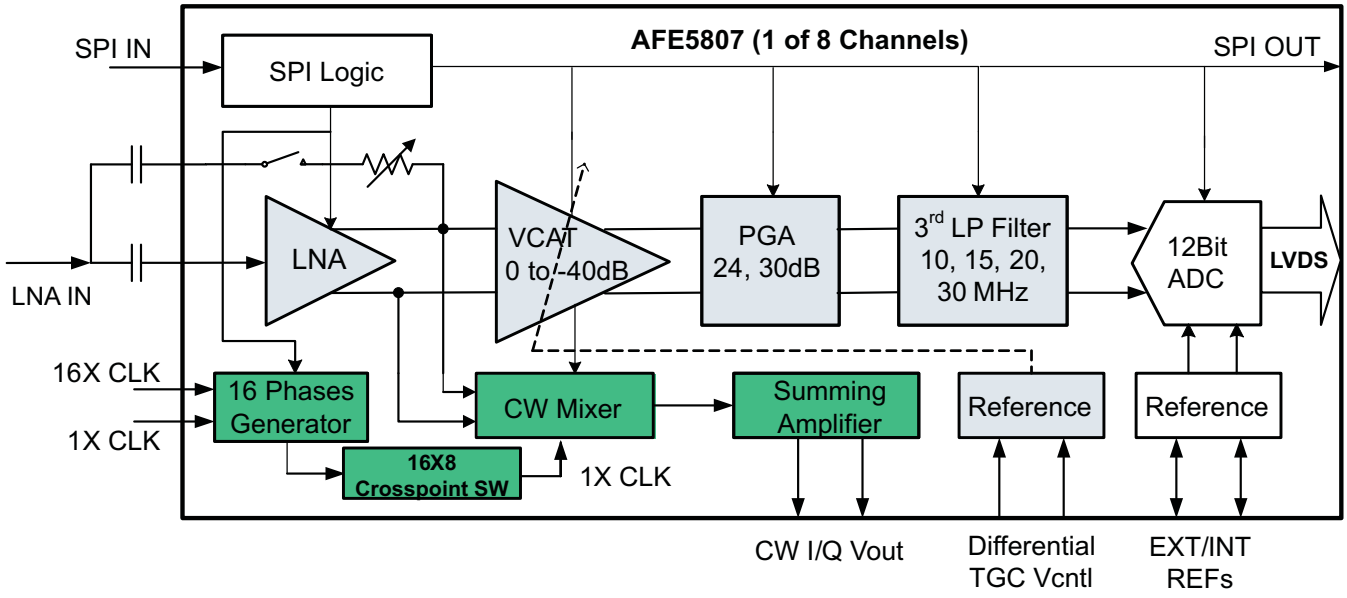


Figure 1. Block Diagram

PACKAGING/ORDERING INFORMATION(1)

PRODUCT	PACKAGE TYPE	OPERATING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
AFE5807	ZCF	0°C to 85°C	AFE5807ZCF	Tray, 160

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE		UNIT
		MIN	MAX	
Supply voltage range	AVDD	–0.3	3.9	V
	AVDD_ADC	–0.3	2.2	V
	AVDD_5V	–0.3	6	V
	DVDD	–0.3	2.2	V
Voltage between AVSS and LVSS		–0.3	0.3	V
Voltage at analog inputs and digital inputs		–0.3	min [3.6,AVDD+0.3]	V
Peak solder temperature(2)			260	°C
Maximum junction temperature (T_J), any condition			105	°C
Storage temperature range		–55	150	°C
Operating temperature range		0	85	°C
ESD Ratings	HBM		2000	V
	CDM		500	V

(1) Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied Exposure to absolute maximum rated conditions for extended periods may degrade device reliability.
(2) Device complies with JSTD-020D.

THERMAL INFORMATION

THERMAL METRIC(1)		AFE5807 BGA 135 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	34.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	5	
θ_{JB}	Junction-to-board thermal resistance	11.5	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	10.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	MAX	UNIT
AVDD	3.15	3.6	V
AVDD_ADC	1.7	1.9	V
DVDD	1.7	1.9	V
AVDD_5V	4.75	5.5	V
Ambient Temperature, T_A	0	85	°C

PINOUT INFORMATION

Top View
ZCF (BGA-135)

	1	2	3	4	5	6	7	8	9
A	AVDD	INP8	INP7	INP6	INP5	INP4	INP3	INP2	INP1
B	CM_BYP	ACT8	ACT7	ACT6	ACT5	ACT4	ACT3	ACT2	ACT1
C	AVSS	INM8	INM7	INM6	INM5	INM4	INM3	INM2	INM1
D	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVDD	AVDD
E	CW_IP_AMPINP	CW_IP_AMPINM	AVSS	AVSS	AVSS	AVSS	AVSS	AVDD	AVDD
F	CW_IP_OUTM	CW_IP_OUTP	AVSS	AVSS	AVSS	AVSS	AVSS	CLKP_16X	CLKM_16X
G	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	CLKP_1X	CLKM_1X
H	CW_QP_OUTM	CW_QP_OUTP	AVSS	AVSS	AVSS	AVSS	AVSS	PDN_GLOBAL	RESET
J	CW_QP_AMPINP	CW_QP_AMPINM	AVSS	AVSS	AVSS	AVDD_ADC	AVDD_ADC	PDN_VCA	SCLK
K	AVDD	AVDD_5V	VCNTLP	VCNTLM	VHIGH	AVSS	DNC	AVDD_ADC	SDATA
L	CLKP_ADC	CLKM_ADC	AVDD_ADC	REFM	DNC	DNC	DNC	PDN_ADC	SEN
M	AVDD_ADC	AVDD_ADC	VREF_IN	REFP	DNC	DNC	DNC	DNC	SDOUT
N	D8P	D8M	DVDD	DNC	DVSS	DNC	DVDD	D1M	D1P
P	D7M	D6M	D5M	FCLKM	DVSS	DCLKM	D4M	D3M	D2M
R	D7P	D6P	D5P	FCLKP	DVSS	DCLKP	D4P	D3P	D2P

PIN FUNCTIONS

PIN		DESCRIPTION
NO.	NAME	
B9~ B2	ACT1...ACT8	Active termination input pins for CH1~8. 1 µF capacitors are recommended. See the APPLICATION INFORMATION section.
A1, D8, D9, E8, E9, K1	AVDD	3.3V Analog supply for LNA, VCAT, PGA, LPF and CWD blocks.
K2	AVDD_5V	5V Analog supply for LNA, VCAT, PGA, LPF and CWD blocks.
J6, J7, K8, L3, M1, M2	AVDD_ADC	1.8V Analog power supply for ADC.
C1, D1~D7, E3~E7, F3~F7, G1~G7, H3~H7,J3~J5, K6	AVSS	Analog ground.
L2	CLKM_ADC	Negative input of differential ADC clock. In the single-end clock mode, it can be tied to GND directly or through a 0.1µF capacitor.
L1	CLKP_ADC	Positive input of differential ADC clock. In the single-end clock mode, it can be tied to clock signal directly or through a 0.1µF capacitor.
F9	CLKM_16X	Negative input of differential CW 16X clock. Tie to GND when the CMOS clock mode is enabled. In the 4X and 8X CW clock modes, this pin becomes the 4X or 8X CLKM input. In the 1X CW clock mode, this pin becomes the quadrature-phase 1X CLKM for the CW mixer. Can be floated if CW mode is not used.
F8	CLKP_16X	Positive input of differential CW 16X clock. In 4X and 8X clock modes, this pin becomes the 4X or 8X CLKP input. In the 1X CW clock mode, this pin becomes the quadrature-phase 1X CLKP for the CW mixer. Can be floated if CW mode is not used.
G9	CLKM_1X	Negative input of differential CW 1X clock. Tie to GND when the CMOS clock mode is enabled (Refer to Figure 89 for details). In the 1X clock mode, this pin is the In-phase 1X CLKM for the CW mixer. Can be floated if CW mode is not used.
G8	CLKP_1X	Positive input of differential CW 1X clock. In the 1X clock mode, this pin is the In-phase 1X CLKP for the CW mixer. Can be floated if CW mode is not used.
B1	CM_BYP	Bias voltage and bypass to ground. ≥ 1µF is recommended. To suppress ultra low frequency noise, 10µF can be used.
E2	CW_IP_AMPINM	Negative differential input of the In-phase summing amplifier. External LPF capacitor has to be connected between CW_IP_AMPINM and CW_IP_OUTP. This pin becomes the CH7 PGA negative output when PGA test mode is enabled. Can be floated if not used.
E1	CW_IP_AMPINP	Positive differential input of the In-phase summing amplifier. External LPF capacitor has to be connected between CW_IP_AMPINP and CW_IP_OUTM. This pin becomes the CH7 PGA positive output when PGA test mode is enabled. Can be floated if not used.
F1	CW_IP_OUTM	Negative differential output for the In-phase summing amplifier. External LPF capacitor has to be connected between CW_IP_AMPINP and CW_IP_OUTPM. Can be floated if not used.
F2	CW_IP_OUTP	Positive differential output for the In-phase summing amplifier. External LPF capacitor has to be connected between CW_IP_AMPINM and CW_IP_OUTP. Can be floated if not used.

PIN FUNCTIONS (continued)

PIN		DESCRIPTION
NO.	NAME	
J2	CW_QP_AMPINM	Negative differential input of the quadrature-phase summing amplifier. External LPF capacitor has to be connected between CW_QP_AMPINM and CW_QP_OUTP. This pin becomes CH8 PGA negative output when PGA test mode is enabled. Can be floated if not used.
J1	CW_QP_AMPINP	Positive differential input of the quadrature-phase summing amplifier. External LPF capacitor has to be connected between CW_QP_AMPINP and CW_QP_OUTM. This pin becomes CH8 PGA positive output when PGA test mode is enabled. Can be floated if not used.
H1	CW_QP_OUTM	Negative differential output for the quadrature-phase summing amplifier. External LPF capacitor has to be connected between CW_QP_AMPINP and CW_QP_OUTM. Can be floated if not used.
H2	CW_QP_OUTP	Positive differential output for the quadrature-phase summing amplifier. External LPF capacitor has to be connected between CW_QP_AMPINM and CW_QP_OUTP. Can be floated if not used.
N8, P9~P7, P3~P1, N2	D1M~D8M	ADC CH1~8 LVDS negative outputs
N9, R9~R7, R3~R1, N1	D1P~D8P	ADC CH1~8 LVDS positive outputs
P6	DCLKM	LVDS bit clock (6x or 7x) negative output
R6	DCLKP	LVDS bit clock (6x or 7x) positive output
K7, L5~L7,M5~M8, N4, N6	DNC	Do not connect. Must leave floated
N3, N7	DVDD	ADC digital and I/O power supply, 1.8V
N5, P5, R5	DVSS	ADC digital ground
P4	FCLKM	LVDS frame clock (1X) negative output
R4	FCLKP	LVDS frame clock (1X) positive output
C9~C2	INM1…INM8	CH1~8 complimentary analog inputs. Bypass to ground with ≥ 0.015µF capacitors. The HPF response of the LNA depends on the capacitors.
A9~A2	INP1...INP8	CH1~8 analog inputs. AC couple to inputs with ≥ 0.1µF capacitors.
L8	PDN_ADC	ADC partial (fast) power down control pin with an internal pull down resistor of 100kΩ. Active High. Either 1.8V or 3.3V logic level can be used.
J8	PDN_VCA	VCA partial (fast) power down control pin with an internal pull down resistor of 20kΩ. Active High, 3.3V logic level is recommended.
H8	PDN_GLOBAL	Global (complete) power-down control pin for the entire chip with an internal pull down resistor of 20kΩ. Active High, 3.3V logic level is recommended.
L4	REFM	0.5V reference output in the internal reference mode. Must leave floated in the internal reference mode. Adding test point on PCB is recommended for monitoring the reference output.
M4	REFP	1.5V reference output in the internal reference mode. Must leave floated in the internal reference mode. Adding test point on PCB is recommended for monitoring the reference output.
H9	RESET	Hardware reset pin with an internal pull-down resistor of 20kΩ. Active high, 3.3V logic level is recommended.
J9	SCLK	Serial interface clock input with an internal pull-down resistor of 20kΩ, 3.3V logic level is recommended.
K9	SDATA	Serial interface data input with an internal pull-down resistor of 20kΩ, 3.3V logic level is recommended.
M9	SDOUT	Serial interface data readout. High impedance when readout is disabled, 1.8V logic.
L9	SEN	Serial interface enable with an internal pull up resistor of 20kΩ. Active low, 3.3V logic level is recommended.
K4	VCNTLM	Negative differential attenuation control pin. Common mode voltage is 0.75V
K3	VCNTLP	Positive differential attenuation control pin. Common mode voltage is 0.75V
K5	VHIGH	Bias voltage; bypass to ground with ≥1µF.
M3	VREF_IN	ADC 1.4V reference input in the external reference mode; bypass to ground with 0.1µF.
K7, L5~L7, M5~M8, N4, N6	DNC	Do not connect. Must leave floated

ELECTRICAL CHARACTERISTICS

AVDD_5V = 5V, AVDD = 3.3V, AVDD_ADC = 1.8V, DVDD = 1.8V, AC-coupled with 0.1µF at INP and bypassed to ground with 15nF at INM, No active termination, V_{CNTL}= 0V, f_{IN} = 5MHz, LNA = 18dB, PGA = 24dB, 12Bit, sample rate = 80MSPS, LPF Filter = 15MHz, low power mode (default power mode), V_{OUT} = –1dBFS, internal 500Ω CW feedback resistor, CMOS CW clocks, ADC configured in internal reference mode, Single-ended VCNTL mode, VCNTLM = GND, at ambient temperature T_A = 25°C, unless otherwise noted. Min and max values are specified across full-temperature range with AVDD_5V = 5V, AVDD = 3.3V, AVDD_ADC = 1.8V, DVDD = 1.8V

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
TGC FULL SIGNAL CHANNEL (LNA+VCAT+LPF+ADC)						
en (RTI)	Input voltage noise over LNA Gain (low noise mode)	Rs = 0Ω, f = 2MHz, LNA = 24/18/12dB, PGA = 24dB		0.80/0.87/1.28		nV/rtHz
		Rs = 0Ω, f = 2MHz,LNA = 24/18/12dB, PGA = 30dB		0.75/0.8/1.1		
	Input voltage noise over LNA Gain (low power mode, i.e. default power mode)	Rs = 0Ω, f = 2MHz,LNA = 24/18/12dB, PGA = 24dB		1.12/1.2/1.47		nV/rtHz
		Rs = 0Ω, f = 2MHz, LNA = 24/18/12dB, PGA = 30dB		1.05/1.1/1.27		
	Input Voltage Noise over LNA Gain(Medium Power Mode)	Rs = 0Ω, f = 2MHz,LNA = 24/18/12dB, PGA = 24dB		1.01/1.1/1.35		nV/rtHz
		Rs = 0Ω, f = 2MHz, LNA = 24/18/12dB, PGA = 30dB		0.95/1.0/1.17		
	Input referred current noise	Low power mode/Medium power mode/Low noise mode		2/2.1/2.7		pA/rtHz
NF	Noise figure	Rs = 200Ω, 200Ω active termination, PGA = 24dB,LNA = 12/18/24dB		4.5/2.95/2.1		dB
		Rs = 100Ω, 100Ω active termination, PGA = 24dB,LNA = 12/18/24dB		6.5/4.3/3.3		dB
		Rs = 200Ω, 200Ω Active Termination , PGA = 24dB, LNA = 12/18/24dB Low noise mode		3.85/2.4/1.8		dB
		Rs = 100Ω, 100Ω Active Termination , PGA=24dB,LNA = 12/18/24dB Low noise mode		5.3/3.6/3.1		dB
V_{MAX}	Maximum Linear Input Voltage	LNA gain = 24/18/12dB		250/500/1000		mVpp
V_{CLAMP}	Clamp Voltage	Reg52[10:9] = 0, LNA = 24/18/12dB		350/600/1150		
	PGA Gain	Low noise mode		24/30		dB
		Medium/Low or default power mode		24/28.5		
	Total gain	LNA = 24dB, PGA = 30dB, Low noise mode		54		dB
		LNA = 24dB, PGA = 30dB, Med power mode		52.5		
		LNA = 24dB, PGA = 30dB, Low power mode (default power mode)		52.5		
	Ch-CH Noise Correlation Factor without Signal (1)	Summing of 8 channels		0		
	Ch-CH Noise Correlation Factor with Signal (1)	Full band (V_{CNTL} = 0/0.8)		0.1/0.2		
		1MHz band over carrier (V_{CNTL}= 0/0.8)		0.1/0.78		
	Signal to Noise Ratio (SNR)	V_{CNTL}= 0.6V (22 dB total channel gain)	64	66.3		dBFS
		V_{CNTL}= 0, LNA = 18dB, PGA = 24dB	57	59.7		
		V_{CNTL}= 0, LNA = 24dB, PGA = 24dB		54.7		
		V_{CNTL} = 0.6V (22 dB total channel gain) Low Noise mode		67.5		
		V_{CNTL} = 0, LNA = 18dB, PGA = 24dB Low Noise mode		62.5		
		V_{CNTL} = 0, LNA = 24dB, PGA = 24dB Low Noise mode		58		
	Narrow Band SNR	SNR over 2MHz band around carrier at V_{CNTL} = 0.6V (22dB total gain)	73	76		dBFS
		SNR over 2MHz band around carrier at V_{CNTL} = 0.6V (22dB total gain) Low Noise mode		77		dBFS
	Input Common-mode Voltage	At INP and INM pins		2.4		V
	Input resistance			8		kΩ
		Preset active termination enabled		50/100/200/400		Ω
	Input capacitance			20		pF
	Input Control Voltage	V_{CNTLP}-V_{CNTLM}	0		1.5	V
	Common-mode voltage	V_{CNTLP} and V_{CNTLM}		0.75		V
	Gain Range			-40		dB
	Gain Slope	V_{CNTL}= 0.1V to 1.1V		35		dB/V
	Input Resistance	Between V_{CNTLP} and V_{CNTLM}		200		KΩ
	Input Capacitance	Between V_{CNTLP} and V_{CNTLM}		1		pF
	TGC Response Time	V_{CNTL}= 0V to 1.5V step function		1.5		µs

(1) Noise correlation factor is defined as Nc/(Nu+Nc), where Nc is the correlated noise power in single channel; and Nu is the uncorrelated noise power in single channel. Its measurement follows the below equation, in which the SNR of single channel signal and the SNR of summed eight channel signal are measured.

$$\frac{N_C}{Nu + N_C} = \frac{10^{-\frac{8CH\_SNR}{10}}}{10^{-\frac{1CH\_SNR}{10}}} \times \frac{1}{56} - \frac{1}{7}$$

ELECTRICAL CHARACTERISTICS (continued)

AVDD_5V = 5V, AVDD = 3.3V, AVDD_ADC = 1.8V, DVDD = 1.8V, AC-coupled with 0.1µF at INP and bypassed to ground with 15nF at INM, No active termination, V_{CNTL}= 0V, f_{IN} = 5MHz, LNA = 18dB, PGA = 24dB, 12Bit, sample rate = 80MSPS, LPF Filter = 15MHz, low power mode (default power mode), V_{OUT} = –1dBFS, internal 500Ω CW feedback resistor, CMOS CW clocks, ADC configured in internal reference mode, Single-ended VCNTL mode, VCNTLM = GND, at ambient temperature T_A = 25°C, unless otherwise noted. Min and max values are specified across full-temperature range with AVDD_5V = 5V, AVDD = 3.3V, AVDD_ADC = 1.8V, DVDD = 1.8V

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
	3rd order-Low-pass Filter			10, 15, 20, 30		MHz
	Settling time for change in LNA gain			14		µs
	Settling time for change in active termination setting			1		µs
AC ACCURACY						
	LPF Bandwidth tolerance			±5%		
	CH-CH group delay variation	2MHz to 15MHz		2		ns
	CH-CH Phase variation	15MHz signal		11		Degree
	Gain matching	0V < V_{CNTL}< 0.1V (Dev-to-Dev)		±0.5		dB
		0.1V < V_{CNTL}<1.1V (Dev-to-Dev)	–1	±0.5	1	
		0.1V < V_{CNTL}<1.1V (Dev-to-Dev) Temp = 0°C and 85°C	–1.2	±0.5	1.2	
		1.1V < V_{CNTL}<1.5V (Dev-to-Dev)		±0.5		
	Gain matching	Channel-to-Channel		±0.25		dB
	Output offset	V_{cntl}= 0, PGA = 30dB, LNA=24dB	–50		50	LSB
AC PERFORMANCE						
HD2	Second-Harmonic Distortion	Fin = 2MHz; V_{OUT} = -1dBFS, low power and low noise modes		–60		dBc
		Fin = 5MHz; V_{OUT} = -1dBFS, low power and low noise modes		–60		
		Fin = 5MHz; V_{IN}= 500mVpp, V_{OUT} = –1dBFS, LNA = 18dB		–55		
		Fin = 5MHz; V_{IN} = 250mVpp, V_{OUT} = –1dBFS, LNA = 24dB, VCNTL = 0.88V, low power and low noise modes		–55		
HD3	Third-Harmonic Distortion	Fin = 2MHz; V_{OUT} = –1dBFS, low power and low noise modes		–53		dBc
		Fin = 5MHz; V_{OUT} = –1dBFS, low power and low noise modes		–54		
		Fin = 5MHz; V_{IN} = 500mVpp, V_{OUT} = –1dBFS, LNA = 18dB, VCNTL = 0.88V, Low power mode/Low Noise Mode		–52/–55		
		Fin = 5MHz; V_{IN} = 250mVpp, V_{OUT} = –1dBFS, LNA = 24dB, VCNT L= 0.88V, Low power mode/Low Noise Mode		–52/–55		
THD	Total Harmonic Distortion	Fin = 2MHz; V_{OUT} = –1dBFS		–52		dBc
		Fin = 5MHz; V_{OUT} = –1dBFS		–52		
IMD3	Intermodulation distortion	f1 = 5MHz at –1dBFS, f2 = 5.01MHz at –27dBFS, low noise mode/low power mode		–60		dBc
XTALK	Cross-talk	Fin = 5MHz; V_{OUT}= –1dBFS		–65		dB
	Phase Noise	1kHz off 5MHz (V_{CNTL}= 0V)		–132		dBc/Hz
LNA						
	Input Referred Voltage Noise	Rs = 0Ω, f = 2MHz, Rin = High Z, Gain = 24/18/12dB, low power mode		0.99/1.0/1.05		nV/rtHz
		Rs = 0Ω, f = 2MHz, Rin = High Z, Gain = 24/18/12dB, Low Noise Mode		0.63/0.70/0.9		
	High-Pass Filter	-3dB Cut-off Frequency		50/100/150/200		KHz
	LNA linear output			4		Vpp
VCAT+ PGA						
	VCAT Input Noise	0dB/-40dB Attenuation		2/10.5		nV/rtHz
	PGA Input Noise	24dB and 30dB, low noise mode/low power mode		1.75/3		nV/rtHz
	-3dB HPF cut-off Frequency			80		KHz

ELECTRICAL CHARACTERISTICS (continued)

AVDD_5V = 5V, AVDD = 3.3V, AVDD_ADC = 1.8V, DVDD = 1.8V, AC-coupled with 0.1µF at INP and bypassed to ground with 15nF at INM, No active termination, V_{CNTL}= 0V, f_{IN} = 5MHz, LNA = 18dB, PGA = 24dB, 12Bit, sample rate = 80MSPS, LPF Filter = 15MHz, low power mode (default power mode), V_{OUT} = –1dBFS, internal 500Ω CW feedback resistor, CMOS CW clocks, ADC configured in internal reference mode, Single-ended VCNTL mode, VCNTLM = GND, at ambient temperature T_A = 25°C, unless otherwise noted. Min and max values are specified across full-temperature range with AVDD_5V = 5V, AVDD = 3.3V, AVDD_ADC = 1.8V, DVDD = 1.8V

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
CW DOPPLER (2)						
en (RTI)	Input voltage noise (CW)	1 channel mixer, LNA = 24dB, 500Ω feedback resistor		0.8		nV/rtHz
		8 channel mixer, LNA = 24dB, 62.5Ω feedback resistor		0.33		
en (RTO)	Output voltage noise (CW)	1 channel mixer, LNA = 24dB, 500Ω feedback resistor		12		nV/rtHz
		8 channel mixer, LNA = 24dB, 62.5Ω feedback resistor		5		
en (RTI)	Input voltage noise (CW)	1 channel mixer, LNA = 18dB, 500Ω feedback resistor		1.1		nV/rtHz
		8 channel mixer, LNA = 18dB, 62.5Ω feedback resistor		0.5		
en (RTO)	Output voltage noise (CW)	1 channel mixer, LNA = 18dB, 500Ω feedback resistor		8.1		nV/rtHz
		8 channel mixer, LNA = 18dB, 62.5Ω feedback resistor		4.0		
NF	Noise figure	Rs = 100Ω,R_{IN} = High Z, fin = 2MHz (LNA, I/Q mixer and summing amplifier/filter)		1.8		dB
f_{CW}	CW Operation Range	CW signal carrier frequency (3)		8		MHz
	CW Clock frequency	1X CLK (16X mode)			8	MHz
		16X CLK(16X mode)			128	
		4X CLK(4X mode)		32		
	AC coupled LVDS clock amplitude(3)	CLKM_16X-CLKP_16X; CLKM_1X-CLKP_1X		0.7		Vpp
	AC coupled LVPECL clock amplitude(3)			1.6		
	CLK duty cycle	1X and 16X CLKs	35%		65%	
	Common-mode voltage	Internal provided		2.5		V
V_{CMOS}	CMOS Input clock amplitude		4		5	V
	CW Mixer conversion loss			4		dB
	CW Mixer phase noise	1kHz off 2MHz carrier		156		dBc/Hz
DR	Input dynamic range	FIN = 2MHz, LNA = 24/18/12dB, low noise mode		160/164/165		dBFS/Hz
IMD3	Intermodulation distortion	f1 = 5 MHz, f2 = 5.01 MHz, both tones at -8.5dBm amplitude, 8 channels summed up in-phase, CW feedback resistor = 87 Ω		–50		dBc
		f1 = 5 MHz, F2 = 5.01 MHz, both tones at –8.5dBm amplitude, Single channel case, CW feed back resistor = 500Ω		–60		dBc
	I/Q Channel gain matching	16X mode		±0.04		dB
	I/Q Channel phase matching	16X mode		±0.1		Degree
	I/Q Channel gain matching	4X mode		±0.04		dB
	I/Q Channel phase matching	4X mode		±0.1		Degree
	Image rejection ratio	fin = 2.01MHz, 300mV input amplitude, CW clock frequency = 2.00MHz		–50		dBc

(2) During CW mode, the LNA is programmed as low noise mode through Reg0x35[10].
(3) In the 16X operation mode, the CW operation range is limited to 8MHz due to the 16X CLK. The maximum clock frequency for the 16X CLK is 128MHz. In the 8X, 4X, and 1X modes, higher CW signal frequencies up to 15 MHz can be supported with small degradation in performance. In addtion, clock amplitude can influence phase noise as well and >0.7Vpp is recommended when differential clocks are used. Please see the application information: CW Clock selection.

ELECTRICAL CHARACTERISTICS (continued)

AVDD_5V = 5V, AVDD = 3.3V, AVDD_ADC = 1.8V, DVDD = 1.8V, AC-coupled with 0.1µF at INP and bypassed to ground with 15nF at INM, No active termination, V_{CNTL}= 0V, f_{IN} = 5MHz, LNA = 18dB, PGA = 24dB, 12Bit, sample rate = 80MSPS, LPF Filter = 15MHz, low power mode (default power mode), V_{OUT} = –1dBFS, internal 500Ω CW feedback resistor, CMOS CW clocks, ADC configured in internal reference mode, Single-ended VCNTL mode, VCNTLM = GND, at ambient temperature T_A = 25°C, unless otherwise noted. Min and max values are specified across full-temperature range with AVDD_5V = 5V, AVDD = 3.3V, AVDD_ADC = 1.8V, DVDD = 1.8V

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
CW SUMMING AMPLIFIER						
V_{CMO}	Common-mode voltage	Summing amplifier inputs/outputs		1.5		V
	Summing amplifier output			4		Vpp
	Input referred voltage noise	100Hz		2		nV/rtHz
		1kHz		1.2		nV/rtHz
		2KHz-100MHz		1		nV/rtHz
	Input referred current noise			2.5		pA/rtHz
	Unit gain bandwidth			200		MHz
	Max output current	Linear operation range		20		mApp
ADC SPECIFICATIONS						
	Sample rate		10		80	MSPS
SNR	Signal-to-noise ratio	Idle channel SNR of ADC 12bit		70		dBFS
		Idle channel SNR of ADC 14bit		72		dBFS
	Internal reference mode	REFP		1.5		V
		REFM		0.5		V
	External reference mode	VREF_IN Voltage		1.4		V
		VREF_IN Current		50		µA
	ADC input full-scale range			2		Vpp
	LVDS Rate	80MSPS at 12 bit		960		Mbps
POWER DISSIPATION (4)						
	AVDD Voltage		3.15	3.3	3.6	V
	AVDD_ADC Voltage		1.7	1.8	1.9	V
	AVDD_5V Voltage		4.75	5	5.5	V
	DVDD Voltage		1.7	1.8	1.9	V
	Total power dissipation per channel	TGC Default power mode (Low power), 80MSPS/12bit		117	148	mW/CH
		TGC Default power mode (Low power), 65MSPS/12bit		109.5		
		TGC medium power mode, 80MSPS/12bit		128.5		
		TGC mode Low noise mode, 80MSPS/12bit		159.5		
		TGC Default power mode (Low power), 40MSPS/12bit		97		
	AVDD (3.3V) Current	TGC low noise mode, no signal		99	130	mA
		TGC medium power mode, no signal		126		
		TGC low noise mode, no signal		202		
		CW-mode, no signal		147	170	
		TGC low noise mode, 500mVpp Input,1% duty cycle		210		
		TGC medium power mode, 500mVpp Input, 1% duty cycle		133		
		TGC default power mode (low power), 500mVpp Input, 1% duty cycle		105		
		CW-mode, 500mVpp Input		375		
	AVDD_5V Current	TGC mode no signal		25	37	mA
		CW Mode no signal, 16X clock = 32MHz		32		
		TGC mode, 500 mVpp Input,1% duty cycle		25		
		CW-mode, 500 mVpp Input, low noise mode		42.5		
	VCA Power dissipation	TGC low noise mode, no signal		99		mW/CH
		TGC medium power mode, no signal		68		
		TGC low power mode, no signal		56.5	77	
		TGC low noise mode, 500 mVpp input,1% duty cycle		102.5		
		TGC medium power mode, 500 mVpp Input, 1% duty cycle		70.5		
		TGC low power mode (default power mode), 500 mVpp input,1% duty cycle		59		

(4) The default power mode of the AFE5807 is low power mode.

ELECTRICAL CHARACTERISTICS (continued)

AVDD_5V = 5V, AVDD = 3.3V, AVDD_ADC = 1.8V, DVDD = 1.8V, AC-coupled with 0.1µF at INP and bypassed to ground with 15nF at INM, No active termination, V_{CNTL}= 0V, f_{IN} = 5MHz, LNA = 18dB, PGA = 24dB, 12Bit, sample rate = 80MSPS, LPF Filter = 15MHz, low power mode (default power mode), V_{OUT} = –1dBFS, internal 500Ω CW feedback resistor, CMOS CW clocks, ADC configured in internal reference mode, Single-ended VCNTL mode, VCNTLM = GND, at ambient temperature T_A = 25°C, unless otherwise noted. Min and max values are specified across full-temperature range with AVDD_5V = 5V, AVDD = 3.3V, AVDD_ADC = 1.8V, DVDD = 1.8V

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
CW Power dissipation	No signal, ADC shutdown CW Mode no signal, low noise mode 16X clock = 32MHz		80		mW/CH
	500 mVpp input, ADC shutdown , 16X clock = 32MHz, low noise mode		173		
AVDD_ADC(1.8V) Current	80 MSPS		167	183	mA
DVDD (1.8V) Current	80 MSPS		102	125	mA
ADC Power dissipation/CH	80 MSPS		60.5	71	mW/CH
	65 MSPS		53		
	40 MSPS		40		
Power dissipation in power down mode	PDN_VCA = High, PDN_ADC = High		25		mW/CH
	Complete power-down PDN_Global=High		0.6		
Power-down response time	Time taken to enter power down		1		µs
Power-up response time	VCA power down		2µs+1% of PDN time		µs
	ADC power down		1		
	Complete power down		2.5		ms
Power supply modulation ratio, AVDD and AVDD_5V	fin = 5MHz, at 50mVpp noise at 1KHz on supply(5)		–65		dBc
	fin = 5MHz, at 50mVpp noise at 50KHz on supply(5)		–65		dBc
Power supply rejection ratio	f = 10kHz,V_{CNTL} = 0V (high gain), AVDD		–40		dBc
	f = 10kHz,V_{CNTL} = 0V (high gain), AVDD_5V		–55		dBc
	f = 10kHz,V_{CNTL} = 1V (low gain), AVDD		–50		dBc

(5) PSMR specification is with respect to input signal amplitude.

DIGITAL CHARACTERISTICS

Typical values are at +25°C, AVDD = 3.3V, AVDD_5 = 5V and AVDD_ADC = 1.8V, DVDD = 1.8V, 12bit / 80MSPS unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = 0°C to T_{MAX} = +85°C.

PARAMETER		CONDITION	MIN	TYP	MAX	UNITS (1)
DIGITAL INPUTS/OUTPUTS						
V_{IH}	Logic high input voltage		2		3.3	V
V_{IL}	Logic low input voltage		0		0.3	V
	Logic high input current			200		µA
	Logic low input current			200		µA
	Input capacitance			5		pF
V_{OH}	Logic high output voltage	SDOUT pin		DVDD		V
V_{OL}	Logic low output voltage	SDOUT pin		0		V
LVDS OUTPUTS						
	Output differential voltage	with 100 Ω external differential termination		400		mV
	Output offset voltage	Common-mode voltage		1100		mV
	FCLKP and FCLKM	1X clock rate	10		80	MHz
	DCLKP and DCLKM	7X clock rate (65MSPS)	70		455	MHz
		6X clock rate (80MSPS)	60		480	MHz
t_{su}	Data setup time (2)			350		ps
t_h	Data hold time (2)			350		ps
ADC INPUT CLOCK						
	CLOCK frequency		10		80	MSPS
	Clock duty cycle		45%	50%	55%	
	Clock input amplitude, differential(V_{CLKP_ADC}–V_{CLKM_ADC})	Sine-wave, ac-coupled	0.5			Vpp
		LVPECL, ac-coupled (3)		1.6		Vpp
		LVDS, ac-coupled (3)		0.7		Vpp
	Common-mode voltage	biased internally		1		V
	Clock input amplitude V_{CLKP_ADC} (single-ended)	CMOS CLOCK		1.8		Vpp

(1) The DC specifications refer to the condition where the LVDS outputs are not switching, but are permanently at a valid logic level 0 or 1 with 100Ω external termination.
(2) Setup and hold time specifications take into account the effect of jitter on the output data and clock. These specifications also assume that the data and clock paths are perfectly matched within the receiver. Any mismatch in these paths within the receiver would appear as reduced timing margins
(3) According to design and characterization, LVDS and LVPECL CLK input amplitude can be as low as 0.2Vpp

TYPICAL CHARACTERISTICS

AVDD_5V =5.0V, AVDD=3.3V, AVDD_ADC=1.8V, DVDD=1.8V, ac-coupled with 0.1uF caps at INP and 15nF caps at INM, No active termination, VCNTL=0V, FIN=5MHz, LNA=18dB, PGA=24dB, 12Bit, sample rate=80MSPS, LPF Filter=15MHz, low noise mode, VOUT= -1dBFS, 500Ω CW feedback resistor, CMOS 16X clock, Single-ended VCNTL mode, VCNTLM = GND, ADC is configured in internal reference mode, at ambient temperature T_A = +25C, unless otherwise noted.

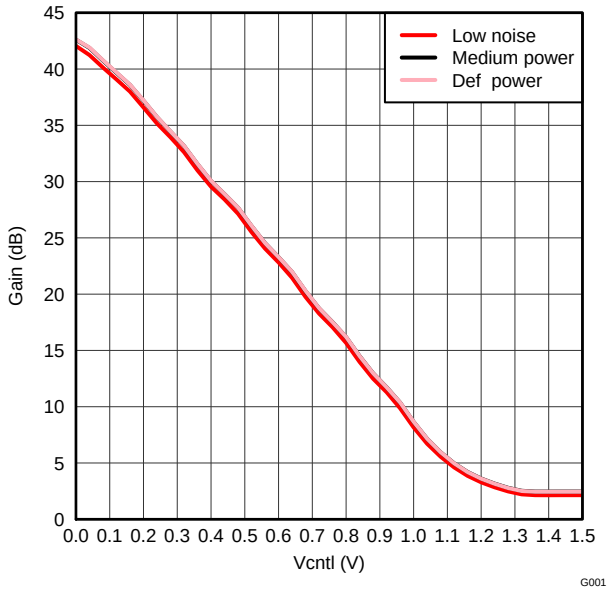


Figure 2. Gain vs. VCNTL, LNA = 18dB and PGA = 24dB

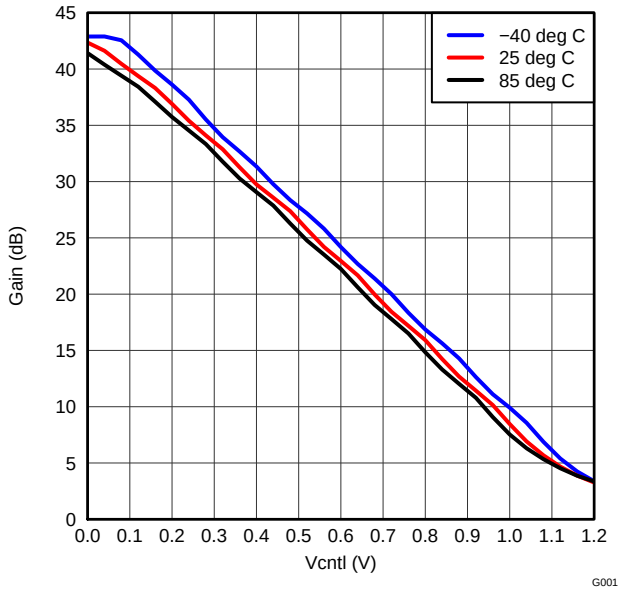


Figure 3. Gain Variation vs. Temperature, LNA = 18dB and PGA = 24dB

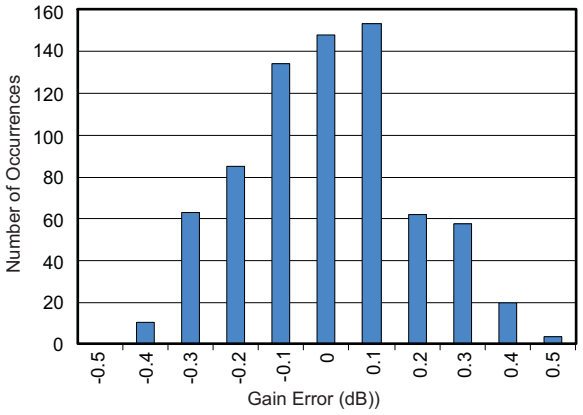


Figure 4. Gain Matching Histogram, V_{CNTL} = 0.3V (936 Channels)

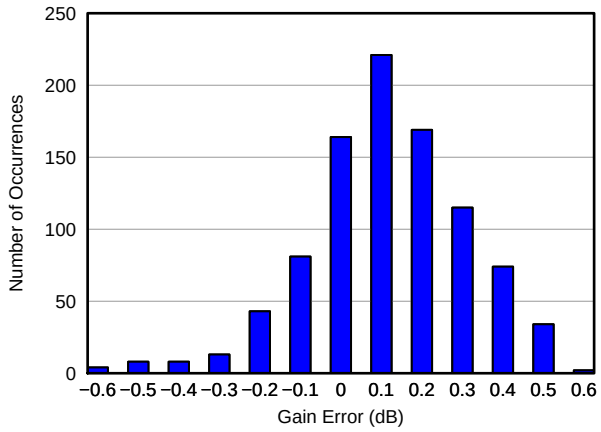


Figure 5. Gain Matching Histogram, V_{CNTL} = 0.6V (936 Channels)

TYPICAL CHARACTERISTICS (continued)

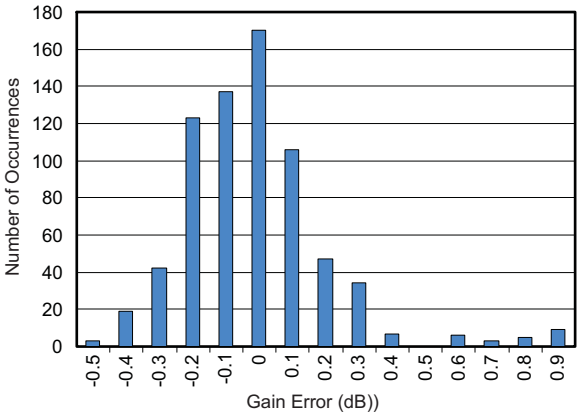


Figure 6. Gain Matching Histogram, V_{CNTL} = 0.9V (936 Channels)

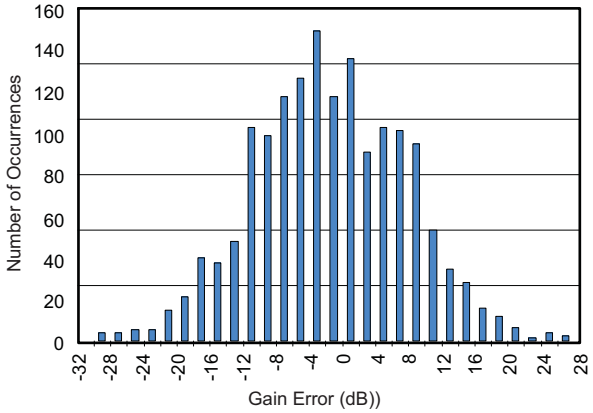


Figure 7. Output Offset Histogram, V_{CNTL} = 0V (936 Channels)

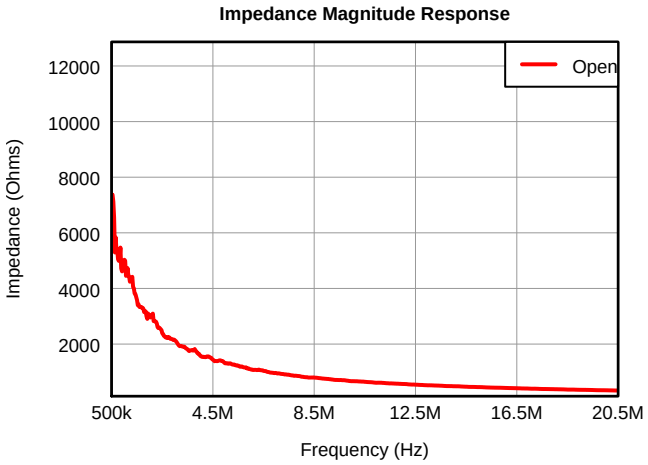


Figure 8. Input Impedance without Active Termination (Magnitude)

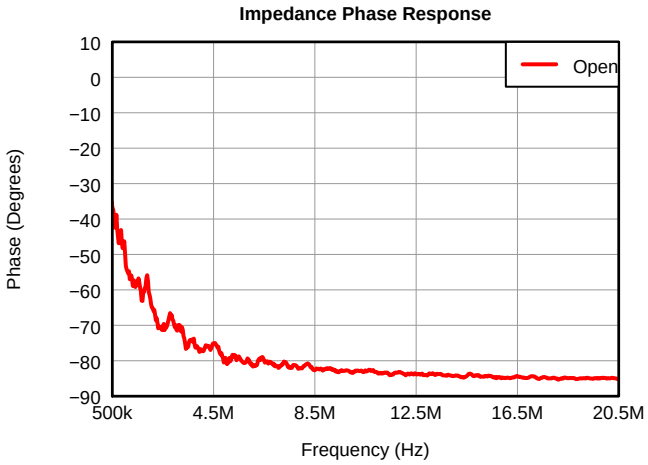


Figure 9. Input Impedance without Active Termination (Phase)

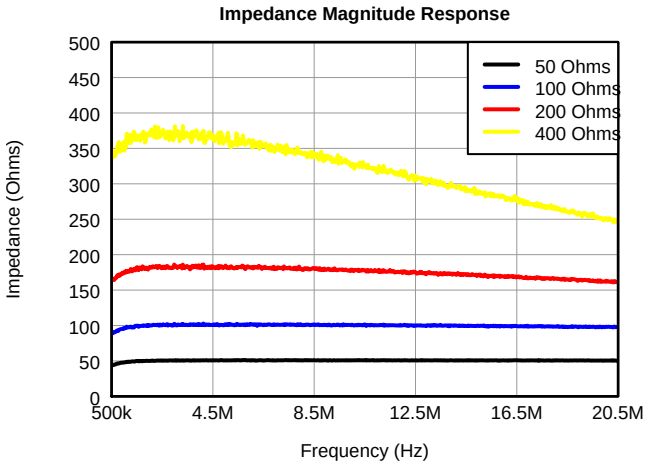


Figure 10. Input Impedance with Active Termination (Magnitude)

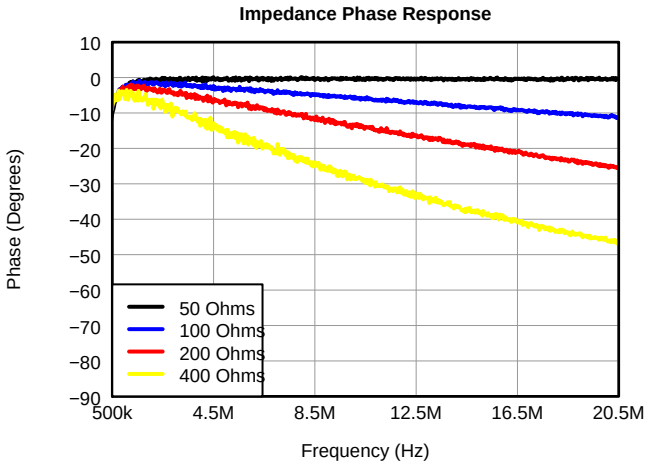


Figure 11. Input Impedance with Active Termination (Phase)

TYPICAL CHARACTERISTICS (continued)

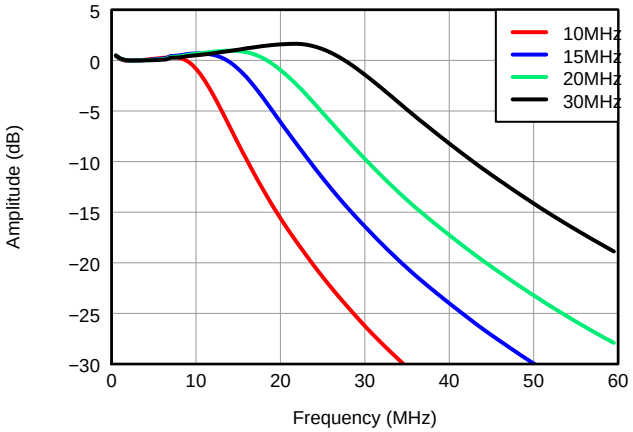


Figure 12. Low-Pass Filter Response

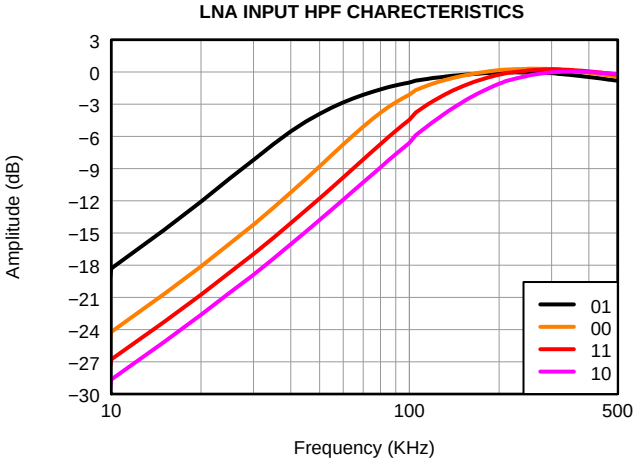


Figure 13. LNA High-Pass Filter Response vs. Reg59[3:2]

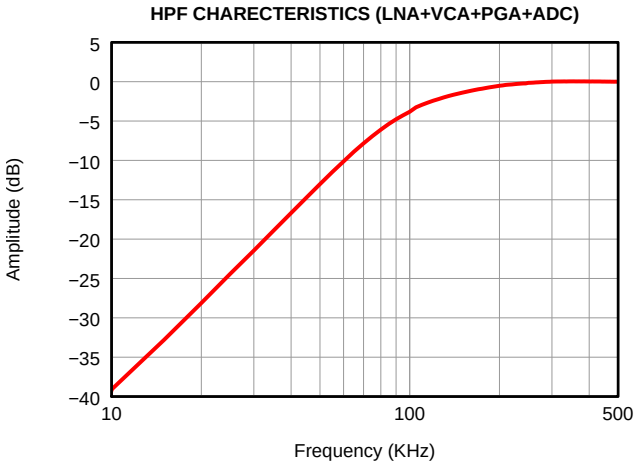


Figure 14. Full Channel High-Pass Filter Response at Default Register Setting

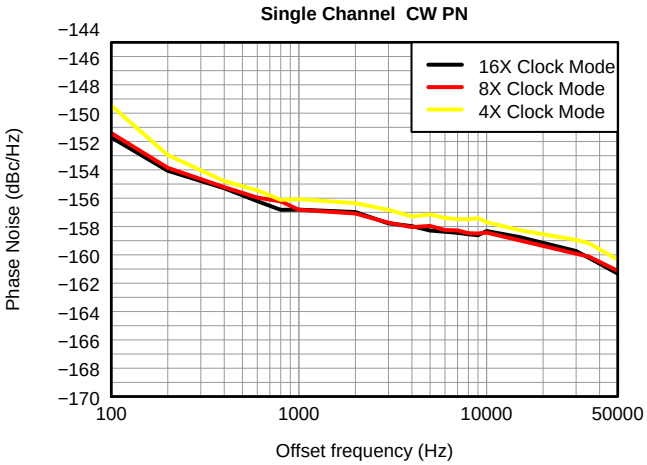


Figure 15. CW Phase Noise, Fin = 2MHz

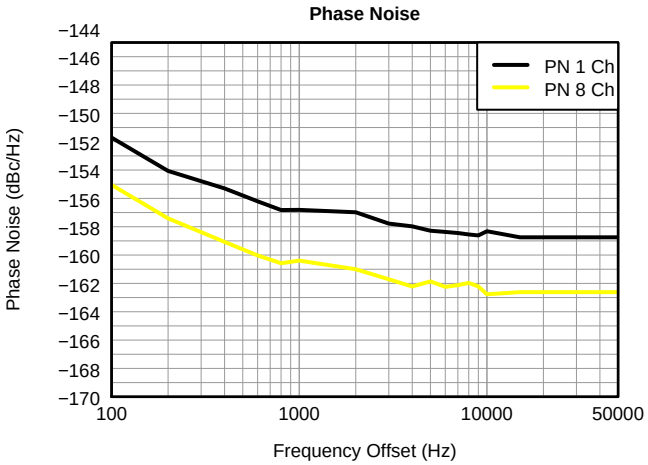


Figure 16. CW Phase Noise, Fin = 2MHz, 1 Channel vs. 8 Channel

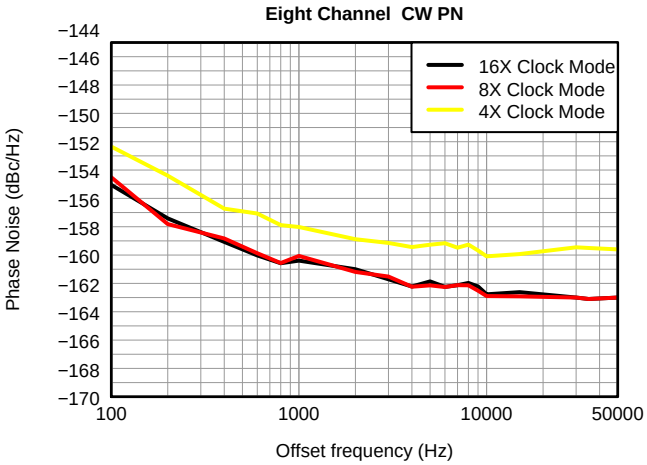


Figure 17. CW Phase Noise vs. Clock Modes, Fin = 2MHz

TYPICAL CHARACTERISTICS (continued)

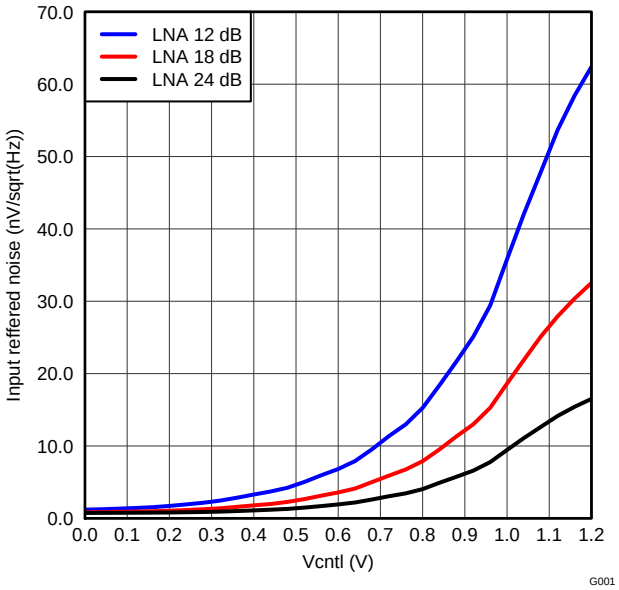


Figure 18. IRN, PGA = 24dB and Low Noise Mode

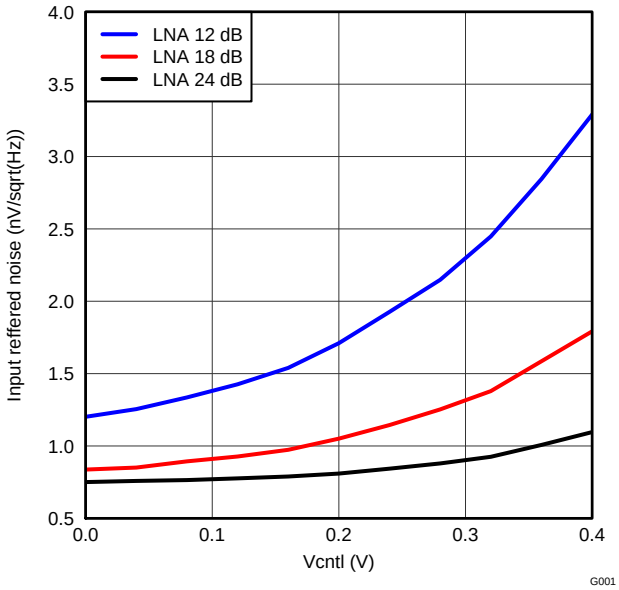


Figure 19. IRN, PGA = 24dB and Low Noise Mode

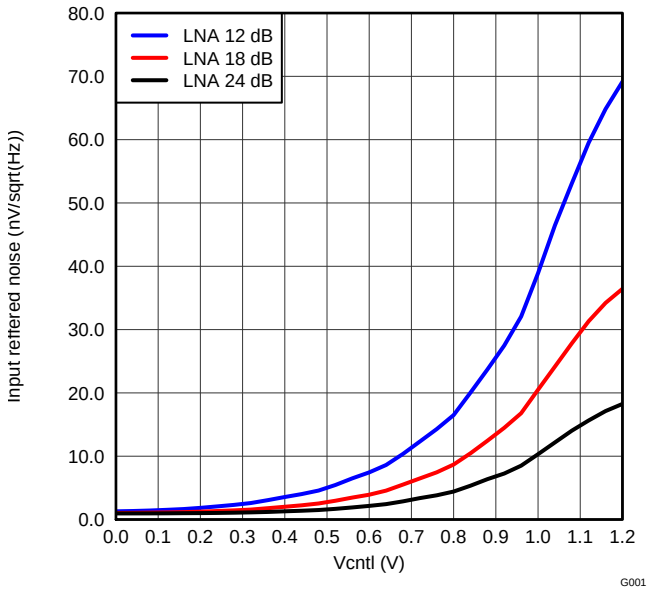


Figure 20. IRN, PGA = 24dB and Medium Power Mode

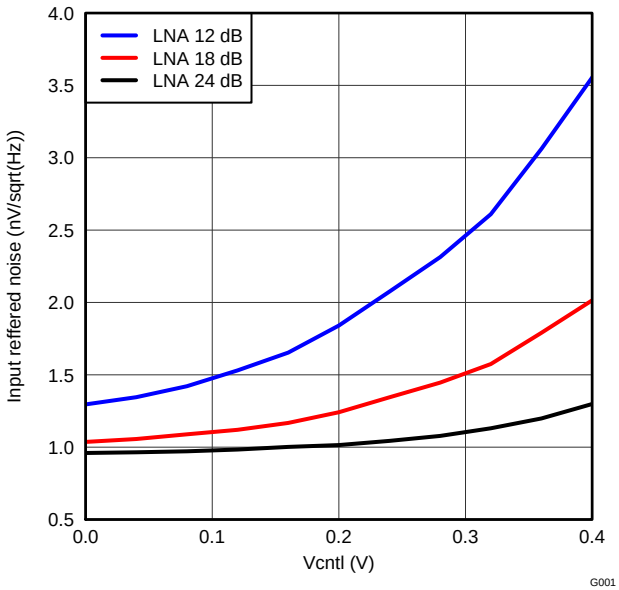


Figure 21. IRN, PGA = 24dB and Medium Power Mode

TYPICAL CHARACTERISTICS (continued)

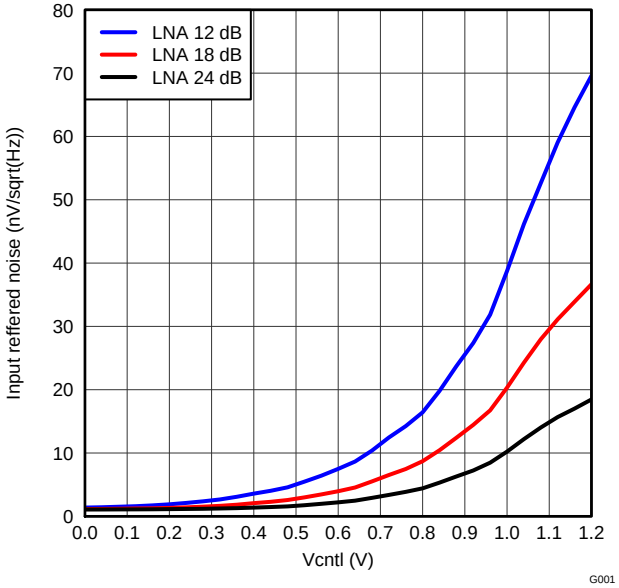


Figure 22. IRN, PGA = 24dB and Low Power Mode

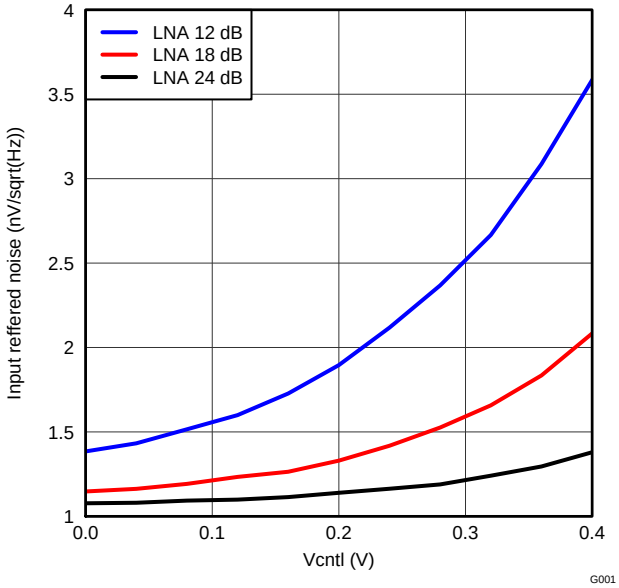


Figure 23. IRN, PGA = 24dB and Low Power Mode

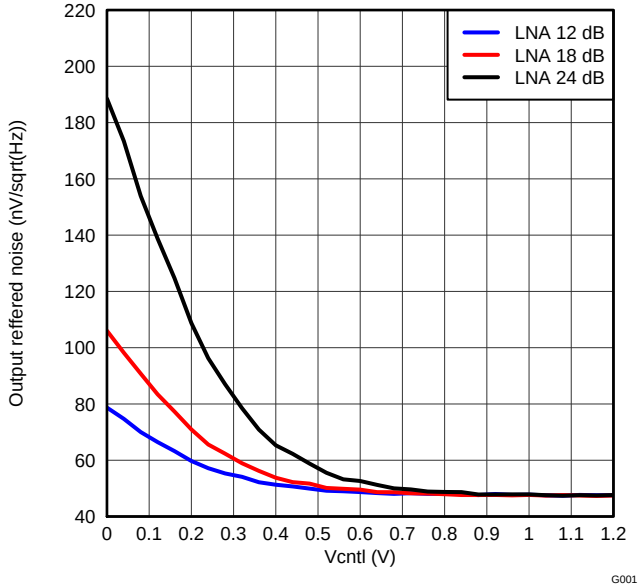


Figure 24. ORN, PGA = 24dB and Low Noise Mode

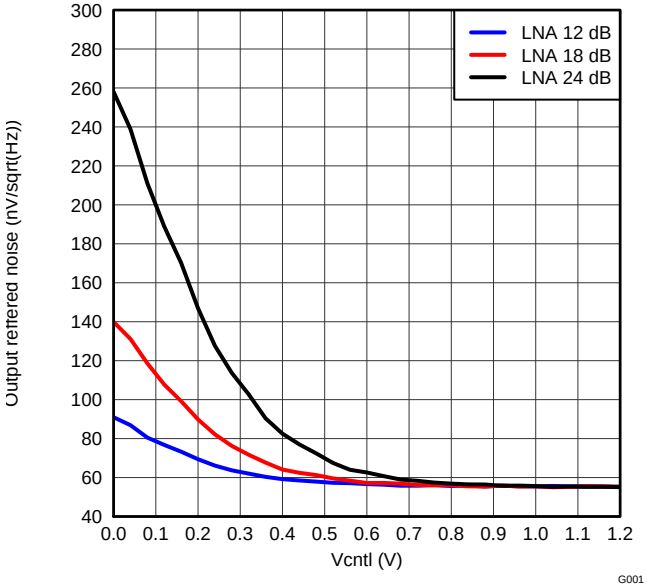


Figure 25. ORN, PGA = 24 dB and Medium Power Mode

TYPICAL CHARACTERISTICS (continued)

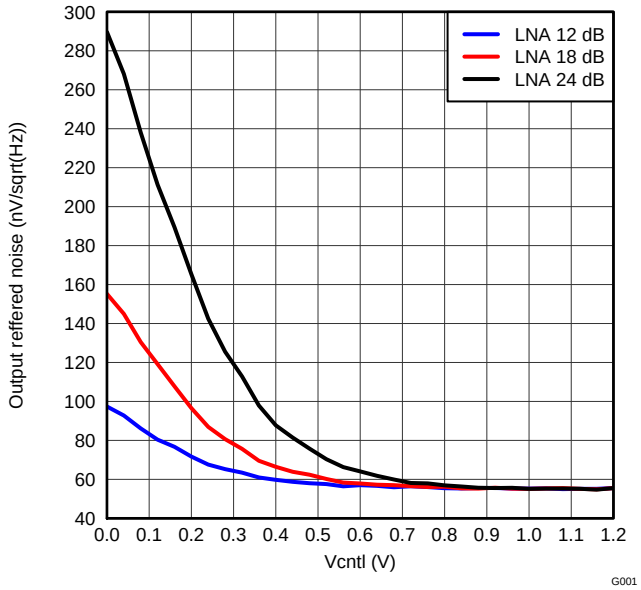


Figure 26. ORN, PGA = 24 dB and Low Power Mode

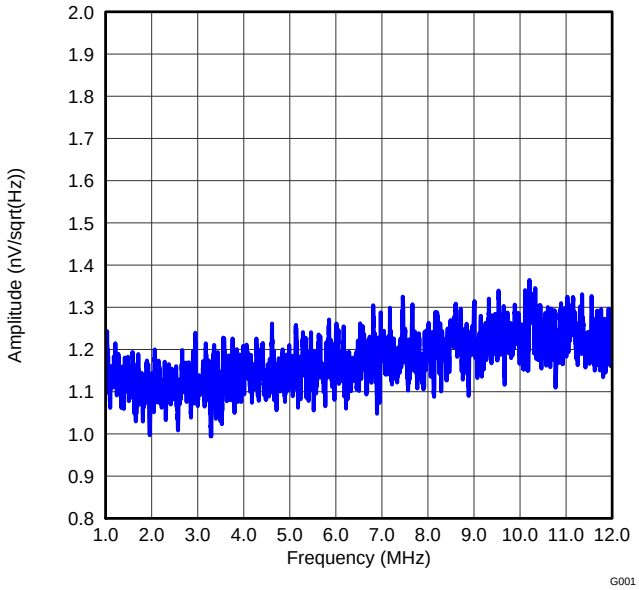


Figure 27. IRN, PGA = 24dB and Low Power Mode

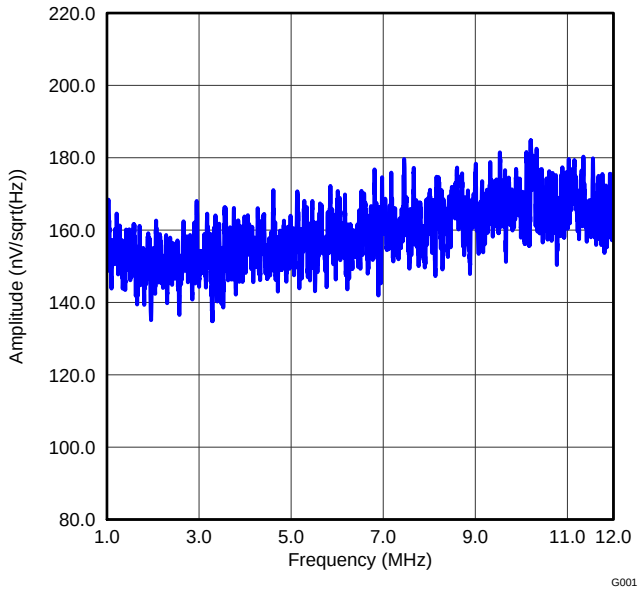


Figure 28. ORN, PGA = 24dB and Low Power Mode

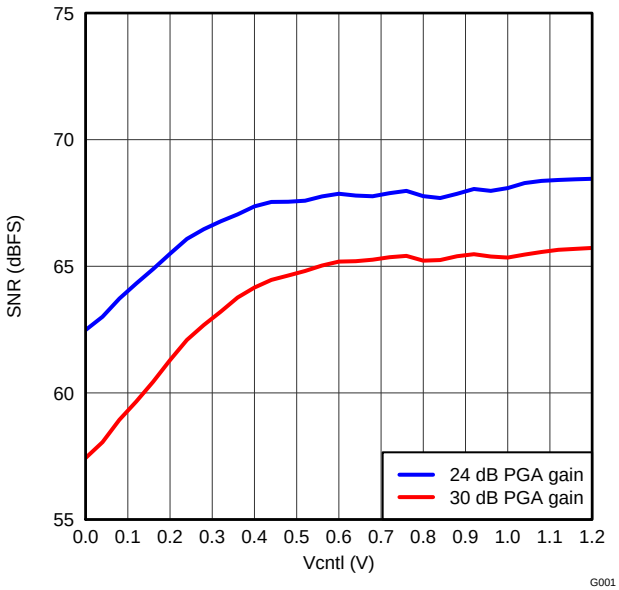


Figure 29. SNR, LNA = 18dB and Low Noise Mode

TYPICAL CHARACTERISTICS (continued)

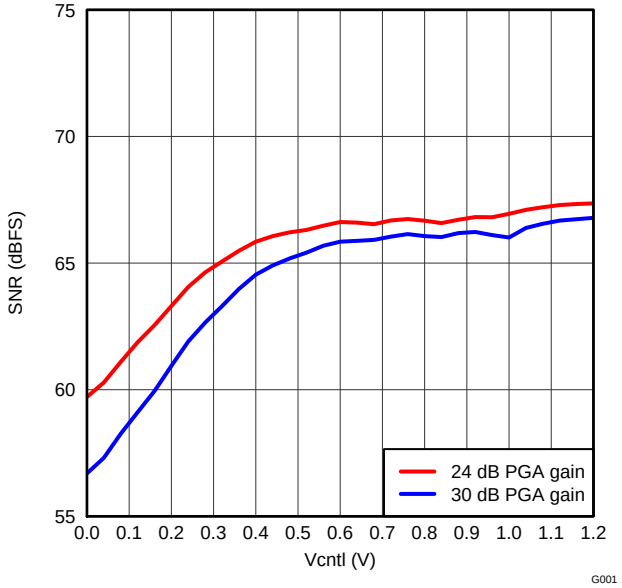


Figure 30. SNR vs. Different PGA Gain (Low Power Mode)

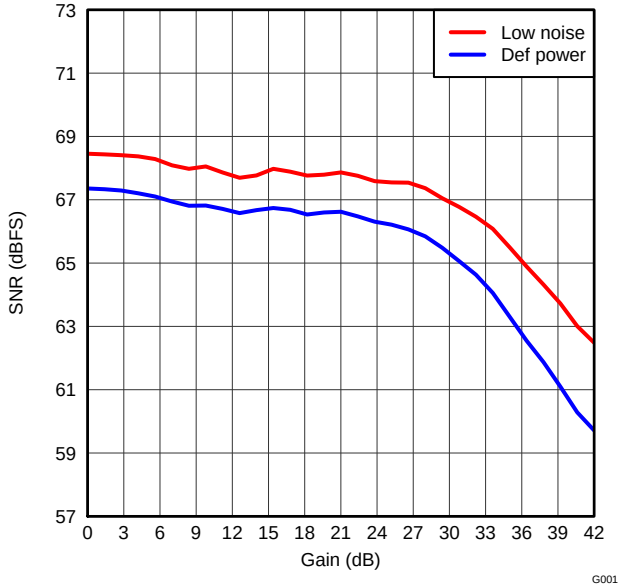


Figure 31. SNR vs. Different Power Modes

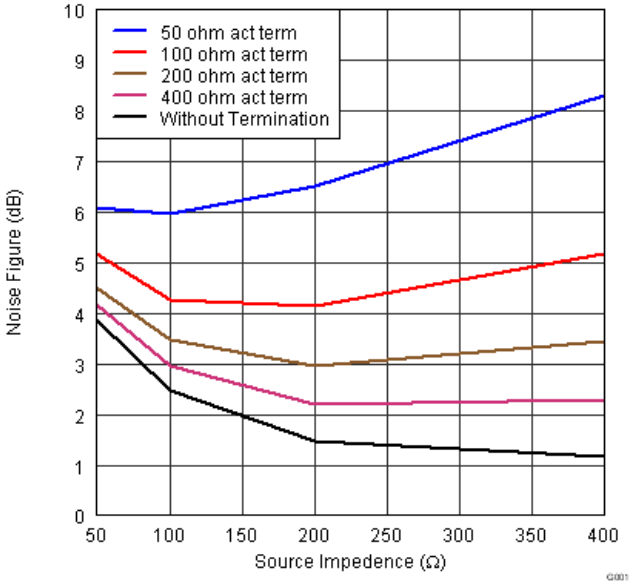


Figure 32. Noise Figure, LNA = 18dB and Low Power Mode

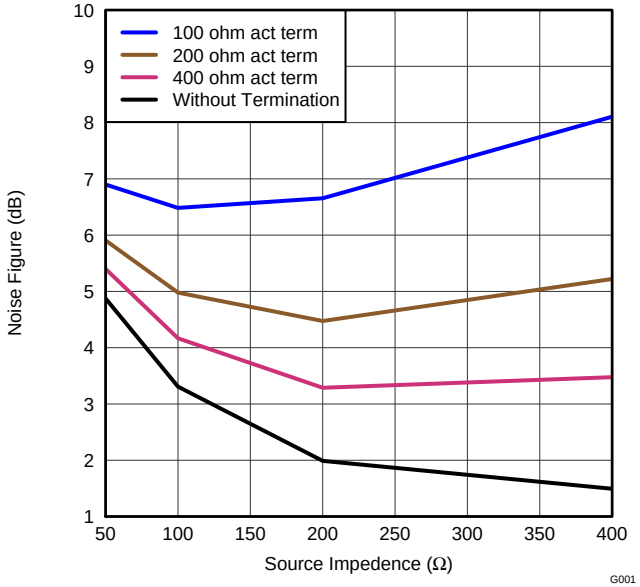


Figure 33. Noise Figure, LNA = 12dB and Low Power Mode

TYPICAL CHARACTERISTICS (continued)

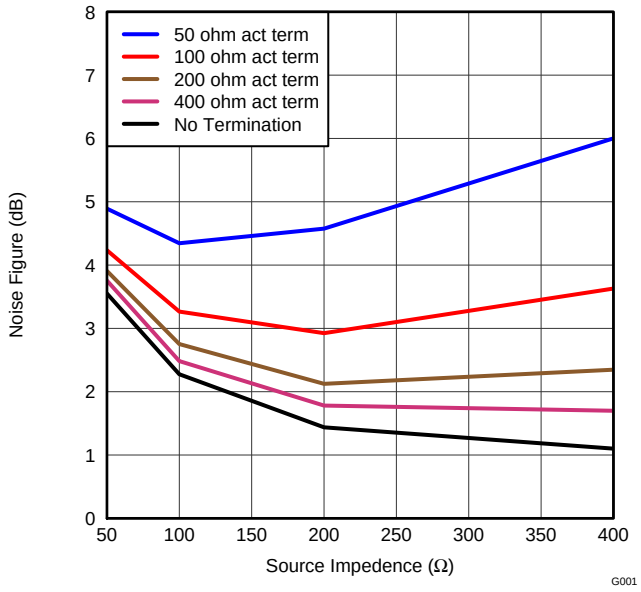


Figure 34. Noise Figure, LNA = 24dB and Low Power Mode

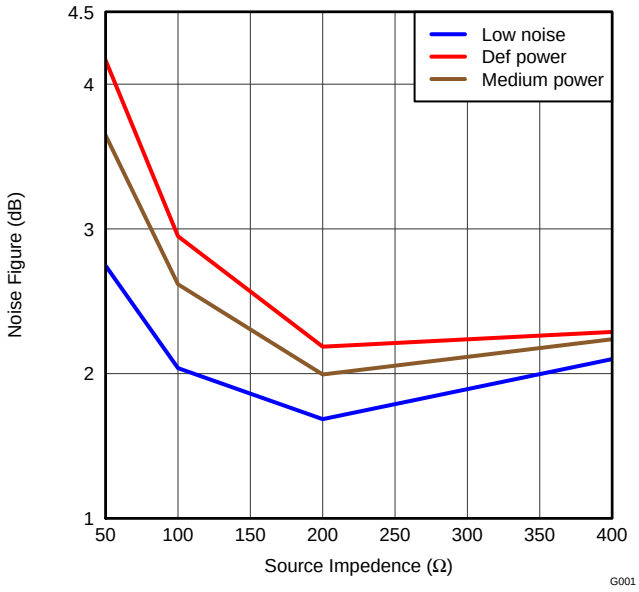


Figure 35. Noise Figure vs. Power Modes with 400Ω Termination

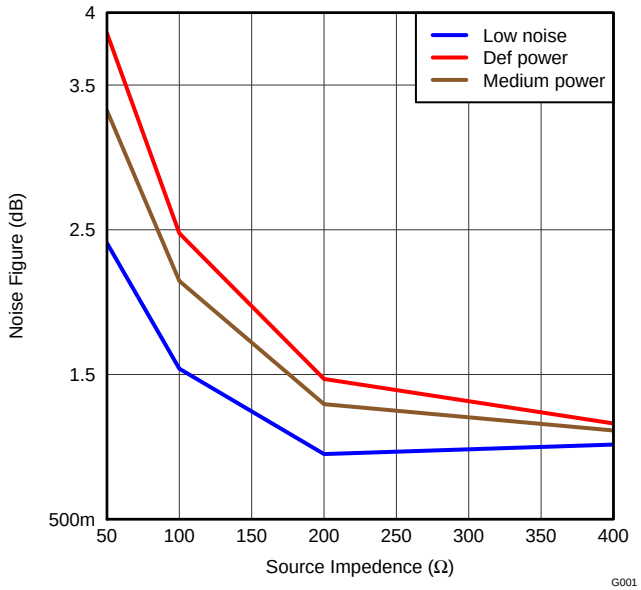


Figure 36. Noise Figure vs. Power Modes without Termination

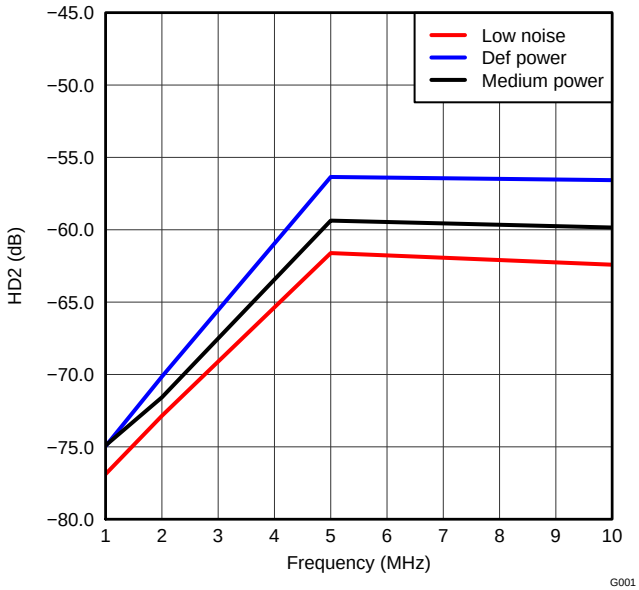


Figure 37. HD2 vs. Frequency, V_{IN} = 500 mVpp and V_{OUT} = -1dBFS

TYPICAL CHARACTERISTICS (continued)

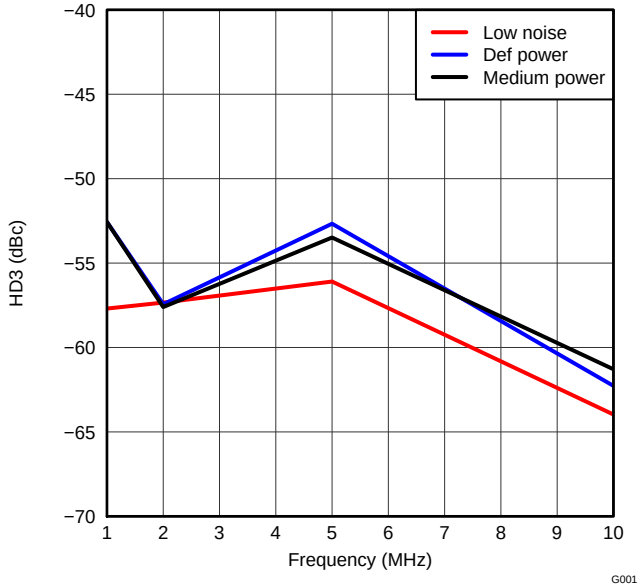


Figure 38. HD3 vs. Frequency, V_{IN} = 500mVpp and V_{OUT} = -1dBFS

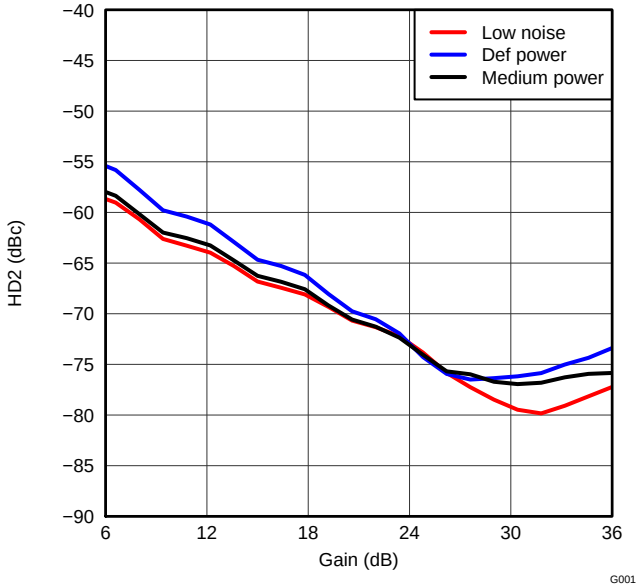


Figure 39. HD2 vs. Gain, LNA = 12dB and PGA = 24dB and V_{OUT} = -1dBFS

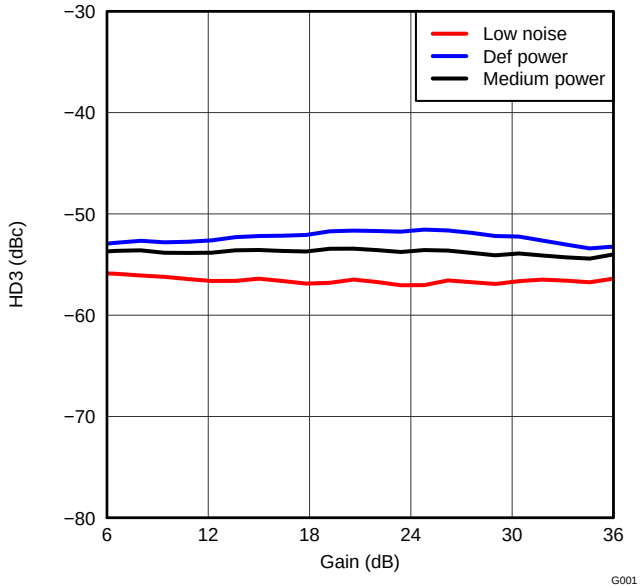


Figure 40. HD3 vs. Gain, LNA = 12dB and PGA = 24dB and V_{OUT} = -1dBFS

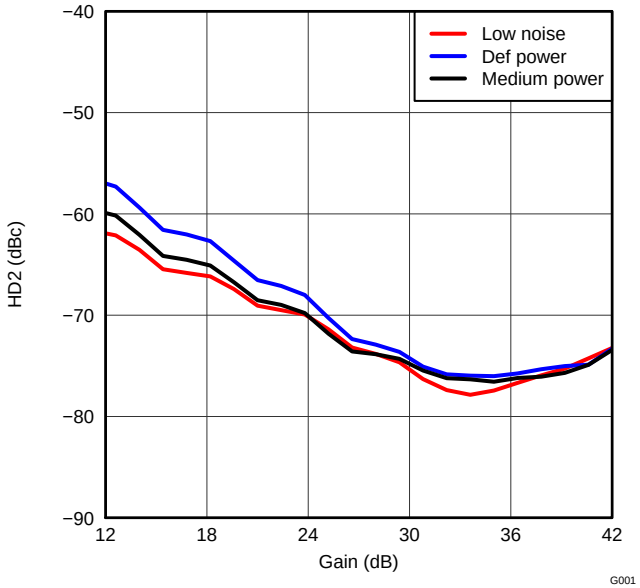


Figure 41. HD2 vs. Gain, LNA = 18dB and PGA = 24dB and V_{OUT} = -1dBFS

TYPICAL CHARACTERISTICS (continued)

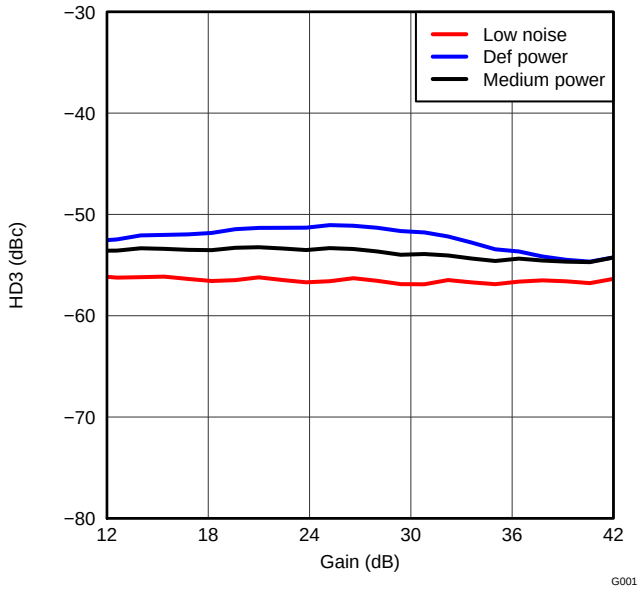


Figure 42. HD3 vs. Gain, LNA = 18dB and PGA = 24dB and V_{OUT} = -1dBFS

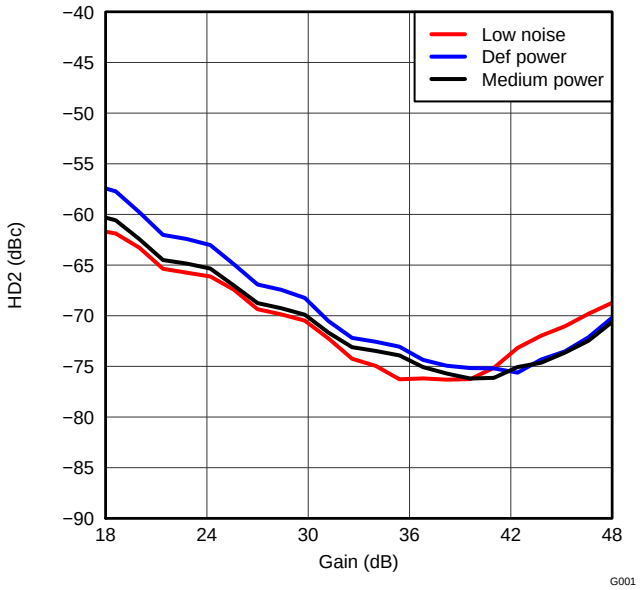


Figure 43. HD2 vs. Gain, LNA = 24dB and PGA = 24dB and V_{OUT} = -1dBFS

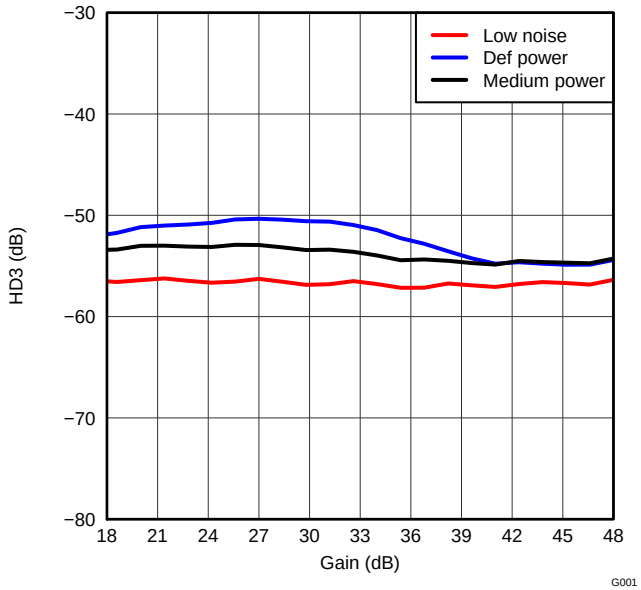


Figure 44. HD3 vs. Gain, LNA = 24dB and PGA = 24dB and V_{OUT} = -1dBFS

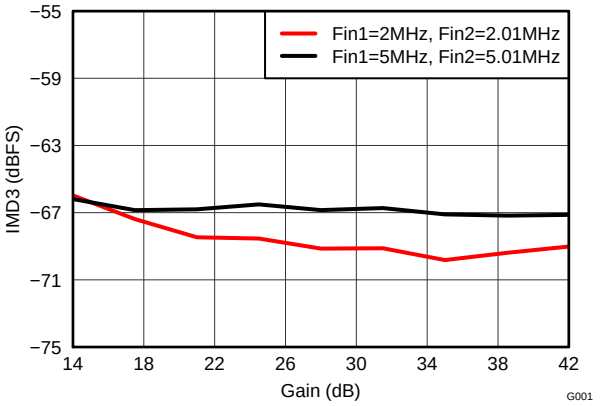


Figure 45. IMD3, Fout1 = -7dBFS and Fout2 = -21dBFS

TYPICAL CHARACTERISTICS (continued)

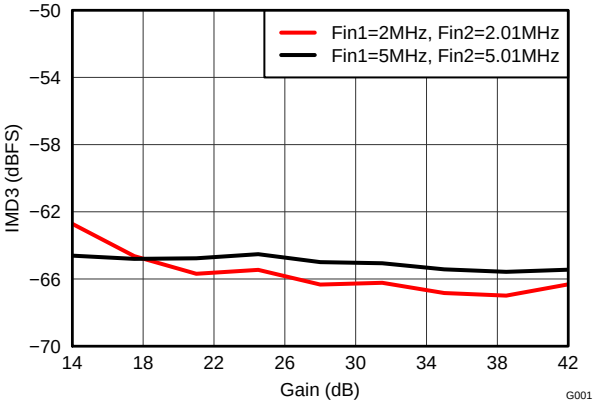


Figure 46. IMD3, Fout1 = -7dBFS and Fout2 = -7dBFS

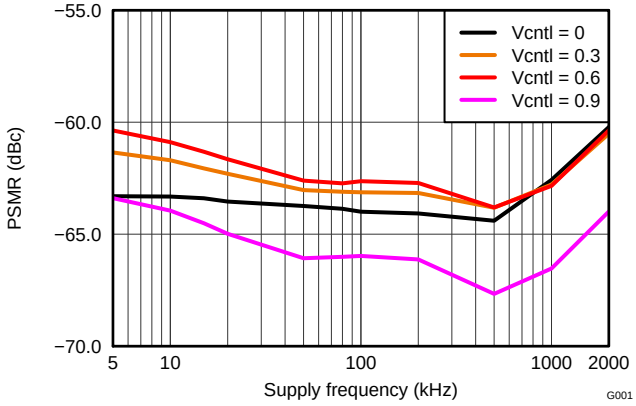


Figure 47. AVDD Power Supply Modulation Ratio, 100 mVpp Supply Noise with Different Frequencies

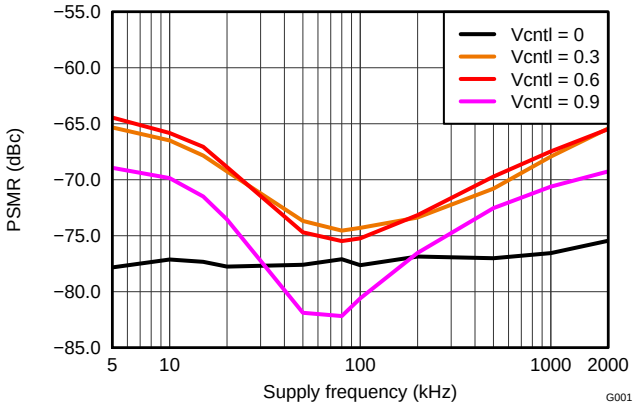


Figure 48. AVDD_5V Power Supply Modulation Ratio, 100 mVpp Supply Noise with Different Frequencies

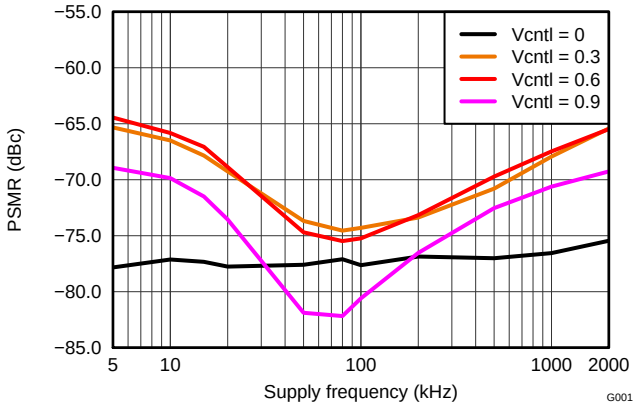


Figure 49. AVDD Power Supply Rejection Ratio, 100 mVpp Supply Noise with Different Frequencies

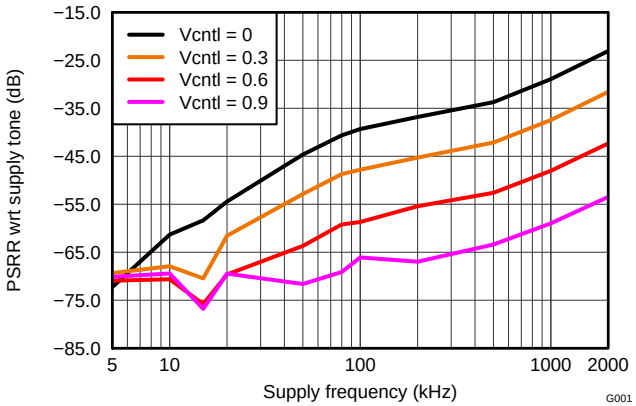


Figure 50. AVDD_5V Power Supply Rejection Ratio, 100mVpp Supply Noise with Different Frequencies

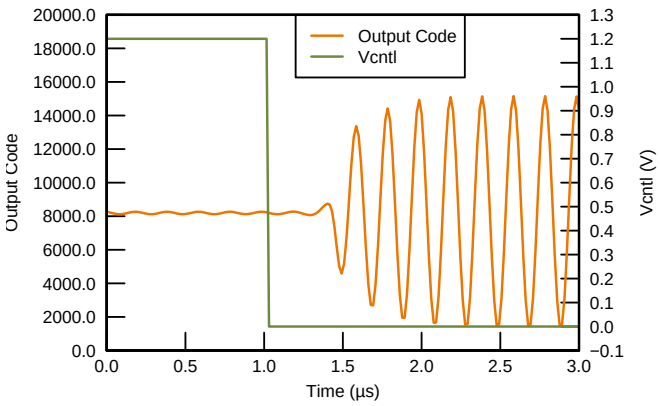


Figure 51. V_{CNTL} Response Time, LNA = 18dB and PGA = 24dB

TYPICAL CHARACTERISTICS (continued)

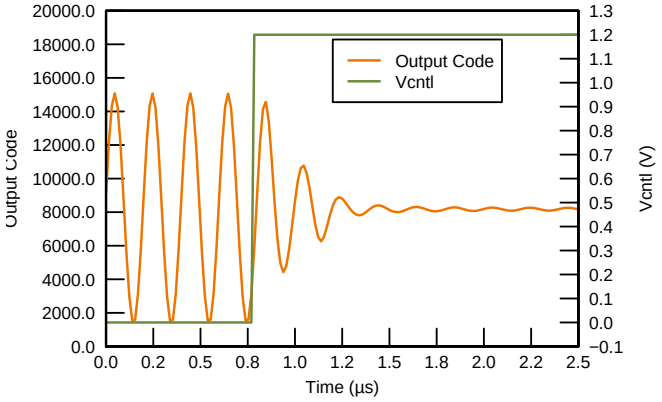


Figure 52. V_{CNTL} Response Time, LNA = 18dB and PGA = 24dB

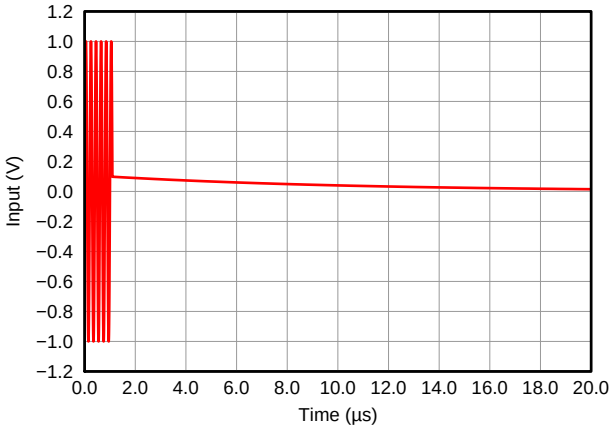


Figure 53. Pulse Inversion Asymmetrical Positive Input

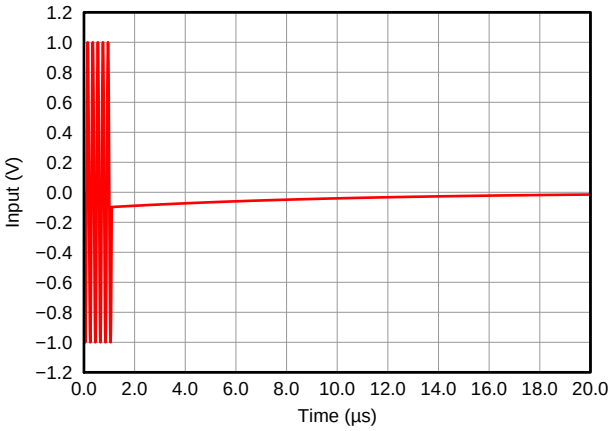


Figure 54. Pulse Inversion Asymmetrical Negative Input

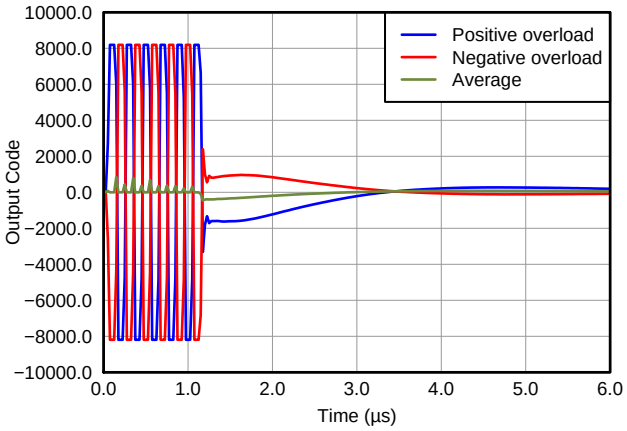


Figure 55. Pulse Inversion, V_{IN} = 2Vpp, PRF = 1KHz, Gain = 21dB

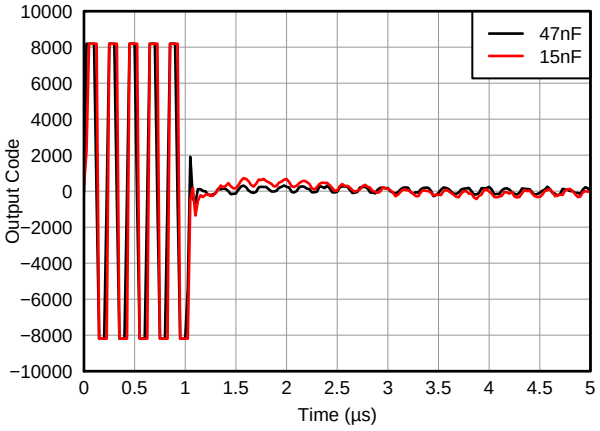


Figure 56. Overload Recovery Response vs. INM capacitor, V_{IN} = 50 mVpp/100 µVpp, Max Gain

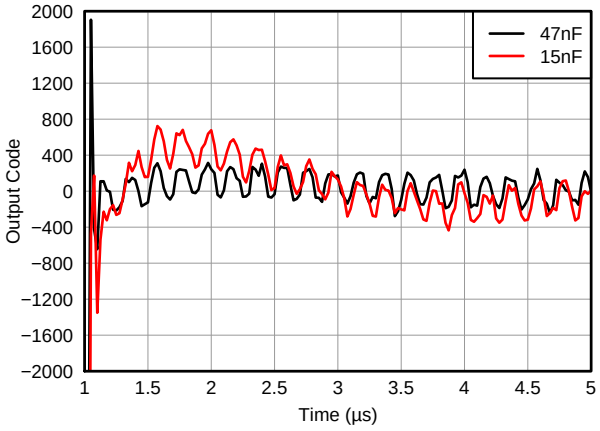


Figure 57. Overload Recovery Response vs. INM Capacitor (Zoomed), V_{IN} = 50 mVpp/100 µVpp, Max Gain

TYPICAL CHARACTERISTICS (continued)

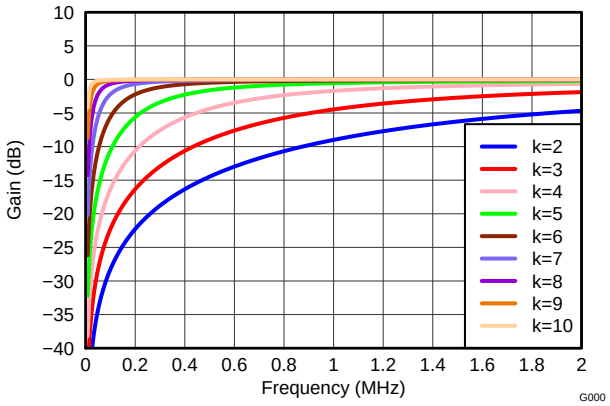


Figure 58. Gain vs Frequency (Fs = 65MSPS)

TIMING CHARACTERISTICS(1)

Typical values are at 25°C, AVDD_5V =5.0V, AVDD = 3.3V, AVDD_ADC = 1.8V, DVDD = 1.8V, Differential clock, C_{LOAD} = 5pF, R_{LOAD} =100Ω, 12Bit, sample rate=80MSPS, unless otherwise noted. Minimum and maximum values are across the full temperature range T_{MIN} = 0°C to T_{MAX} = 85°C with AVDD_5V = 5V, AVDD = 3.3V, AVDD_ADC = 1.8V, DVDD = 1.8V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ta	Aperture delay	The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs	0.7	3		ns
	Aperture delay matching	Across channels within the same device		±150		ps
t_j	Aperture jitter			450		Fs rms
	ADC latency	Default after reset or 0 x 2 [12] = 1, LOW_LATENCY = 1		11 or 8		Input clock cycles
t_{PROG}	Data and frame clock delay	Input clock rising edge (zero cross) to frame clock rising edge (zero cross) minus 3/7 of the input clock period (T).	See the *OUTPUT INTERFACE TIMING* table			
Δt_{delay}	Delay variation	At fixed supply and 20°C T difference. Device to device	–1		1	ns
t_{RISE}	Data rise time Data fall time	Rise time measured from –100mV to 100mV Fall time measured from 100mV to –100mV 10MHz < f_{CLKIN} < 80MHz		0.14		ns
t_{FALL}				0.15		
$t_{FCLKRISE}$	Frame clock rise time Frame clock fall time	Rise time measured from –100mV to 100mV Fall time measured from 100mV to –100mV 10MHz < f_{CLKIN} < 80MHz		0.14		ns
$t_{FCLKFALL}$				0.15		
	Frame clock duty cycle	Zero crossing of the rising edge to zero crossing of the falling edge	48	50	52	%
$t_{DCLKRISE}$	Bit clock rise time Bit clock fall time	Rise time measured from –100mV to 100mV Fall time measured from 100mV to –100mV 10MHz < f_{CLKIN} < 80MHz		0.13		ns
$t_{DCLKFALL}$				0.12		
	Bit clock duty cycle	Zero crossing of the rising edge to zero crossing of the falling edge 10MHz < f_{CLKIN} < 80MHz	46		54	%

(1) Timing parameters are ensured by design and characterization; not production tested.

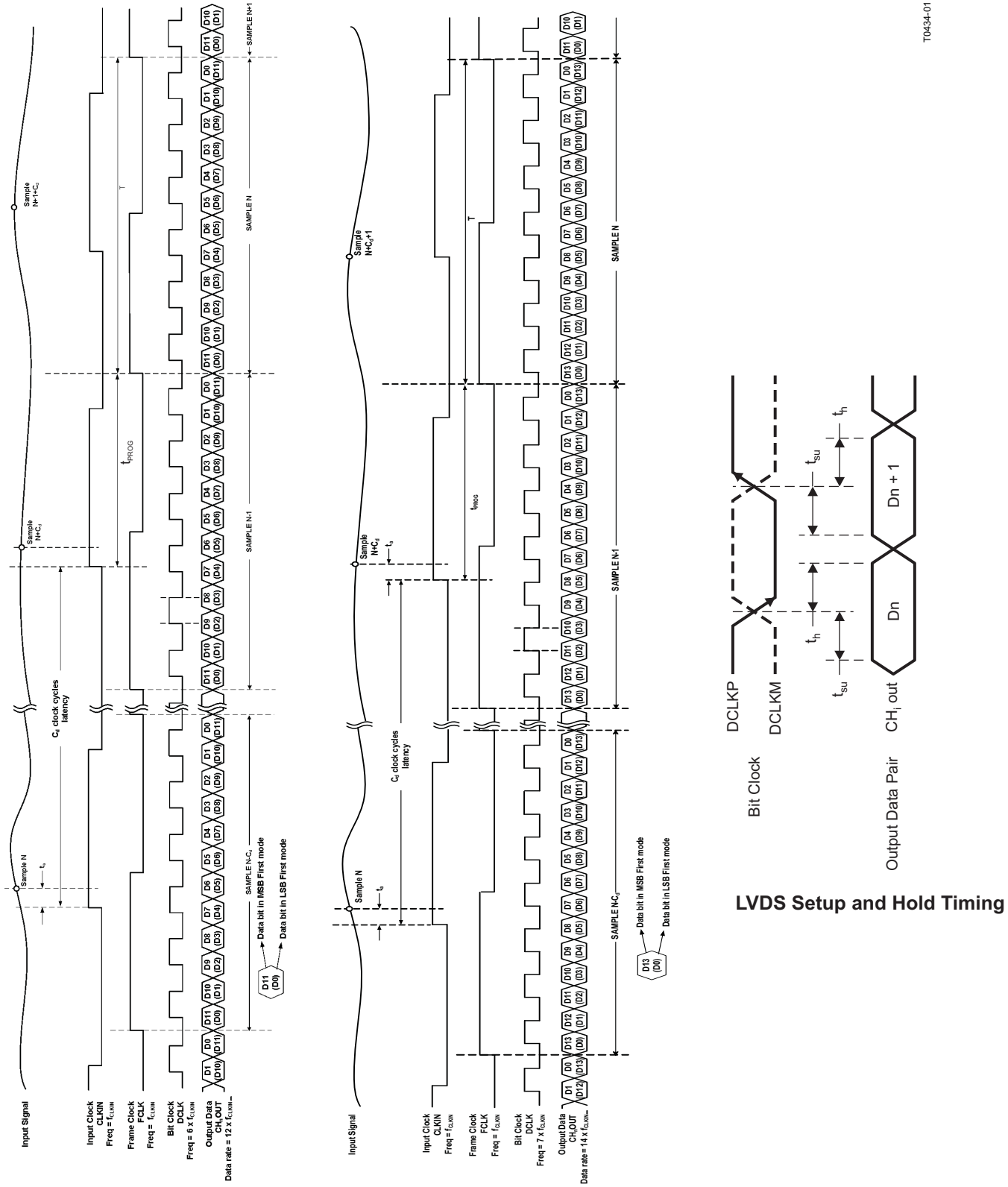
OUTPUT INTERFACE TIMING (12Bit)(1)(2)(3)

f_{CLKIN}, Input Clock Frequency	Setup Time (t_{su}), ns (for output data and frame clock)			Hold Time (t_h), ns (for output data and frame clock)			t_{PROG} = (3/7)x T + t_{delay}, ns		
	Data Valid to DCLK Zero-Crossing			DCLK Zero-Crossing to Data Invalid			Input Clock Zero-Cross (rising edge) to Frame Clock Zero-Cross (rising edge)		
MHz	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
80	0.31	0.41		0.18	0.39		10.3	11.4	12
65	0.48	0.55		0.37	0.51		11.6	12.8	13.4
50	0.67	0.74		0.58	0.71		13.9	15.1	15.7
40	0.86	0.93		0.79	0.92		16.2	17.55	18.5
30	1.2	1.28		1.12	1.26		20.3	21.75	22.7
20	1.79	1.94		1.8	1.94		28.3	29.95	30.9

(1) FCLK timing is the same as for the output data lines. It has the same relation to DCLK as the data pins. Setup and hold are the same for the data and the frame clock.
(2) Data valid is logic HIGH = +100mV and logic LOW = -100mV
(3) Timing parameters are ensured by design and characterization; not production tested.

NOTE

The above timing data can be applied to 14-bit or 16-bit LVDS rates as well. For example, the maximum LVDS output rate at 80MHz and 12-bit is equal to 960 MSPS, which is approximately equivalent to the rate at 68.5 MHz and 14-bit.



12-Bit 6x serialization mode **14-Bit 7x serialization mode** **LVDS Setup and Hold Timing**

Figure 59. LVDS Timing Diagrams

LVDS Output Interface Description

AFE5807 has LVDS output interface which supports multiple output formats. The ADC resolutions can be configured as 12bit or 14bit as shown in the LVDS timing diagrams Figure 59. The ADCs in the AFE5807 are running at 14bit; 2 LSBs are removed when 12-bit output is selected in the default mode, and two 0s are added at LSBs when 16-bit output is selected. Appropriate ADC resolutions can be selected for optimizing system performance-cost effectiveness. When the devices run at 16bit mode, higher end FPGAs are required to process higher rate of LVDS data. Corresponding register settings are listed in Table 1.

Table 1. Corresponding Register Settings

LVDS Rate	10 bit (5X DCLK)	12 bit (6X DCLK)	14 bit (7X DCLK)	16 bit (8X DCLK)
Reg 3 [14:13]	01	00	11	10
Reg 4 [2:0]	100	000	010	000
Description	4LSBs removed	2 LSBs removed	N/A	2 0s added at LSBs

Serial Peripheral Interface (SPI) Operation

Serial Register Write Description

Programming of different modes can be done through the serial interface formed by pins SEN (serial interface enable), SCLK (serial interface clock), SDATA (serial interface data) and RESET. All these pins have a pull-down resistor to GND of 20kΩ. Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA is latched at every rising edge of SCLK when SEN is active (low). The serial data is loaded into the register at every 24th SCLK rising edge when SEN is low. If the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiple of 24-bit words within a single active SEN pulse (there is an internal counter that counts groups of 24 clocks after the falling edge of SEN). The interface can work with the SCLK frequency from 20 MHz down to low speeds (few Hertz) and even with non-50% duty cycle SCLK. The data is divided into two main portions: a register address (8 bits) and the data itself (16 bits), to load on the addressed register. When writing to a register with unused bits, these should be set to 0. Figure 60 illustrates this process.

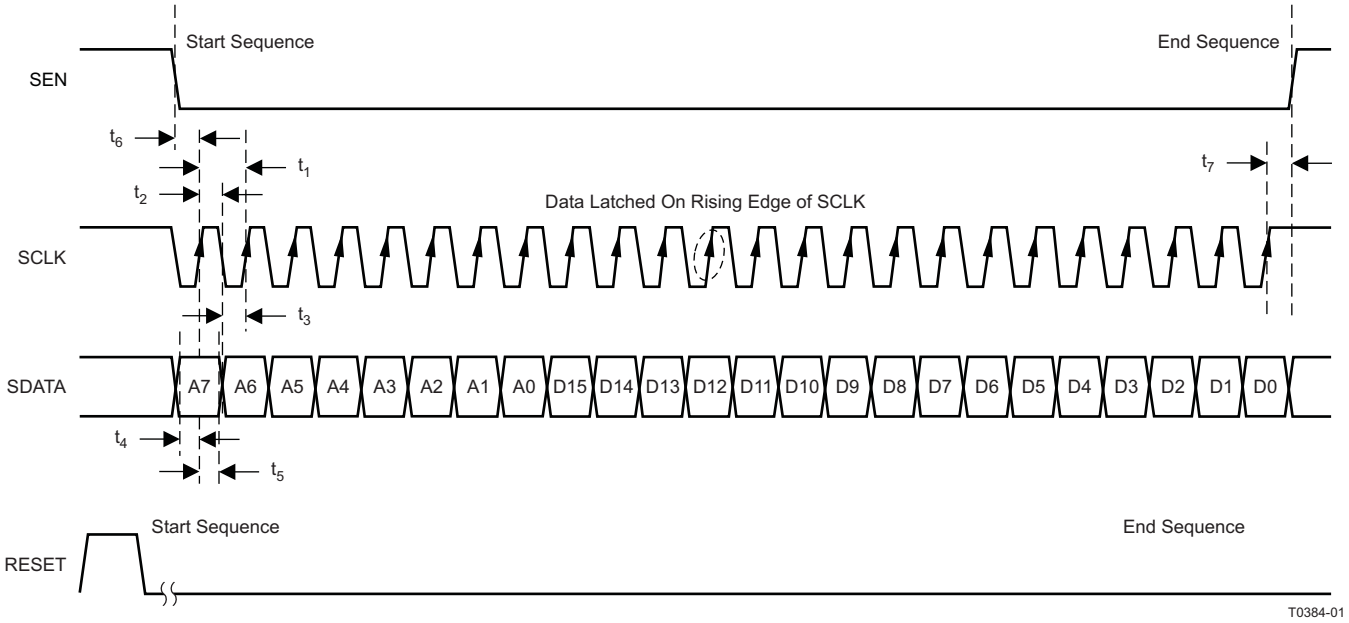


Figure 60. SPI Timing

SPI Timing Characteristics

Minimum values across full temperature range t_{MIN} = 0°C to t_{MAX} = 85°C, AVDD_5V =5.0V, AVDD=3.3V, AVDD_ADC=1.8V, DVDD=1.8V

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_1	SCLK period	50			ns
t_2	SCLK high time	20			ns
t_3	SCLK low time	20			ns
t_4	Data setup time	5			ns
t_5	Data hold time	5			ns
t_6	$\overline{SEN}$ fall to SCLK rise	8			ns
t_7	Time between last SCLK rising edge to $\overline{SEN}$ rising edge	8			ns
t_8	SDOUT Delay	12	20	28	ns

Register Readout

The device includes an option where the contents of the internal registers can be read back. This may be useful as a diagnostic test to verify the serial interface communication between the external controller and the AFE. First, the <REGISTER READOUT ENABLE> bit (Reg0[1]) needs to be set to '1'. Then user should initiate a serial interface cycle specifying the address of the register (A7-A0) whose content has to be read. The data bits are "don't care". The device will output the contents (D15-D0) of the selected register on the SDOUT pin. The SDOUT has a typical delay, t_8, of 20nS from the fallin edge of the SCLK. For lower speed SCLK, SDOUT can be latched on the rising edge of SCLK. For higher speed SCLK, e.g. the SCLK period less than 60 nS, it is better to latch the SDOUT at the next falling edge of SCLK. The following timing diagram shows this operation (the time specifications follow the same information provided. In the readout mode, users still can access the <REGISTER READOUT ENABLE> through SDATA/SCLK/SEN. To enable serial register writes, set the <REGISTER READOUT ENABLE> bit back to '0'.

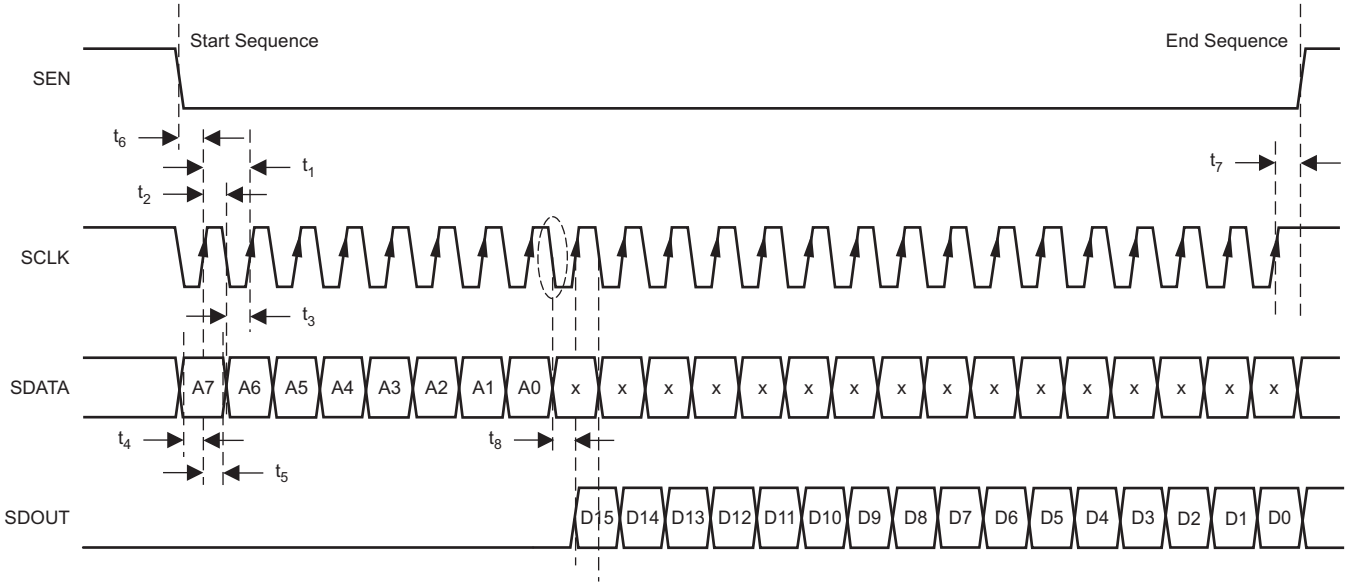
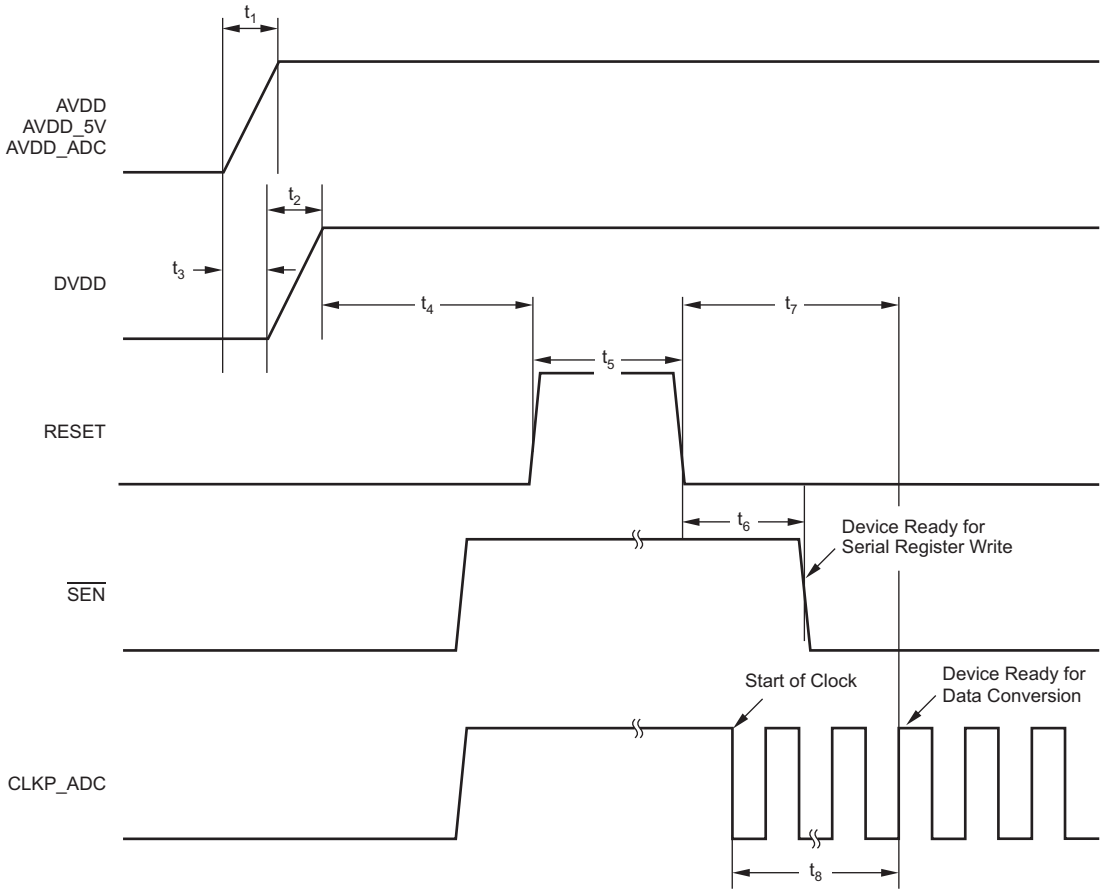


Figure 61. Serial Interface Register Read

The AFE5807 SDOUT buffer is 3-stated and will get enabled only when 0[1] (REGISTER READOUT ENABLE) is enabled. SDOUT pins from multiple AFE5807s can be tied together without any pull-up resistors. Level shifter SN74AUP1T04 can be used to convert 1.8V logic to 2.5V/3.3V logics if needed.



10µs< t1 < 50ms, 10µs<t2<50ms, –10ms<t3 < 10ms, t4>10ms, t5>100ns, t6>100ns, t7>10ms, and t8>100µs. The AVDDx and DVDD power-on sequence does not matter as long as –10ms < t3 < 10ms. Similar considerations apply while shutting down the device.

Figure 62. Recommended Power-up Sequencing and Reset Timing

Register Map

A reset process is required at the AFE5807 initialization stage. Initialization can be done in one of two ways:

1. Through a hardware reset, by applying a positive pulse in the RESET pin
2. Through a software reset, using the serial interface, by setting the SOFTWARE RESET bit to high. Setting this bit initializes the internal registers to the respective default values (all zeros) and then self-resets the SOFTWARE RESET bit to low. In this case, the RESET pin can stay low (inactive).

After reset, all ADC and VCA registers are set to '0', i.e. default settings. During register programming, all reserved/unlisted register bits need to be set as '0'. Register settings are maintained when the AFE5807 is in either partial power down mode or complete power down mode.

ADC Register Map

Table 2. ADC Register Map

ADDRESS (DEC)	ADDRESS (HEX)	Default Value	FUNCTION	DESCRIPTION
0[0]	0x0[0]	0	SOFTWARE_RESET	0: Normal operation; 1: Resets the device and self-clears the bit to '0'
0[1]	0x0[1]	0	REGISTER_READOUT_ENABLE	0:Disables readout; 1: enables readout of register at SDOUT Pin
1[0]	0x1[0]	0	ADC_COMPLETE_PDN	0: Normal 1: Complete Power down
1[1]	0x1[1]	0	LVDS_OUTPUT_DISABLE	0: Output Enabled; 1: Output disabled
1[9:2]	0x1[9:2]	0	ADC_PDN_CH<7:0>	0: Normal operation; 1: Power down. Power down Individual ADC channels. 1[9]→CH8…1[2]→CH1
1[10]	0x1[10]	0	PARTIAL_PDN	0: Normal Operation; 1: Partial Power Down ADC
1[11]	0x1[11]	0	LOW_FREQUENCY_ NOISE_SUPPRESSION	0: No suppression; 1: Suppression Enabled
1[13]	0x1[13]	0	EXT_REF	0: Internal Reference; 1: External Reference. VREF_IN is used. Both 3[15] and 1[13] should be set as 1 in the external reference mode
1[14]	0x1[14]	0	LVDS_OUTPUT_RATE_2X	0: 1x rate; 1: 2x rate. Combines data from 2 channels on 1 LVDS pair. When ADC clock rate is low, this feature can be used
1[15]	0x1[15]	0	SINGLE-ENDED_CLK_MODE	0: Differential clock input; 1: Single-ended clock input
2[2:0]	0x2[2:0]	0	RESERVED	Set to 0
2[10:3]	0x2[10:3]	0	POWER-DOWN_LVDS	0: Normal operation; 1: PDN Individual LVDS outputs. 2[10]→CH8…2[3]→CH1
2[11]	0x2[11]	0	AVERAGING_ENABLE	0: No averaging; 1: Average 2 channels to increase SNR
2[12]	0x2[12]	0	LOW_LATENCY	0: Default Latency with digital features supported, 11 cycle latency 1: Low Latency with digital features bypassed, 8 cycle latency
2[15:13]	0x2[15:3]	0	TEST_PATTERN_MODES	000: Normal operation; 001: Sync; 010: De-skew; 011: Custom; 100:All 1's; 101: Toggle; 110: All 0's; 111: Ramp
3[7:0]	0x3[7:0]	0	INVERT_CHANNELS	0: No inverting; 1:Invert channel digital output. 3[7]→CH8;3[0]→CH1
3[8]	0x3[8]	0	CHANNEL_OFFSET_ SUBSTRACTION_ENABLE	0: No offset subtraction; 1: Offset value Subtract Enabled
3[9:11]	0x3[9:11]	0	RESERVED	Set to 0
3[12]	0x3[12]	0	DIGITAL_GAIN_ENABLE	0: No digital gain; 1: Digital gain Enabled

Table 2. ADC Register Map (continued)

ADDRESS (DEC)	ADDRESS (HEX)	Default Value	FUNCTION	DESCRIPTION
3[14:13]	0x3[14:13]	0	SERIALIZED_DATA_RATE	Serialization factor 00: 12x 01: 10x, two LSBs are dropped 10: 16x, **Note:** Reg4[2:0]=0, The data output is 12bit ADC data with 4 additional padded 0s 11: 14x (see Table 1)
3[15]	0x3[15]	0	ENABLE_EXTERNAL_ REFERENCE_MODE	0: Internal reference mode; 1: Set to external reference mode Note: both 3[15] and 1[13] should be set as 1 when configuring the device in the external reference mode
4[2:0]	0x4[2:0]	0	ADC_RESOLUTION_SELECT	000: 12bit; 010: 14bit; 100: 10bit (see Table 1)
4[3]	0x4[3]	0	ADC_OUTPUT_FORMAT	0: 2's complement; 1: Offset binary
4[4]	0x4[4]	0	LSB_MSB_FIRST	0: LSB first; 1: MSB first
5[13:0]	0x5[13:0]	0	CUSTOM_PATTERN	Custom pattern data for LVDS output (2[15:13]=011)
10[8]	0xA[8]	0	SYNC_PATTERN	0: Test pattern outputs of 8 channels are NOT synchronized. 1: Test pattern outputs of 8 channels are synchronized.
13[9:0]	0xD[9:0]	0	OFFSET_CH1	Value to be subtracted from channel 1 code
13[15:11]	0xD[15:11]	0	DIGITAL_GAIN_CH1	0dB to 6dB in 0.2dB steps
15[9:0]	0xF[9:0]	0	OFFSET_CH2	value to be subtracted from channel 2 code
15[15:11]	0xF[15:11]	0	DIGITAL_GAIN_CH2	0dB to 6dB in 0.2dB steps
17[9:0]	0x11[9:0]	0	OFFSET_CH3	value to be subtracted from channel 3 code
17[15:11]	0x11[15:11]	0	DIGITAL_GAIN_CH3	0dB to 6dB in 0.2dB steps
19[9:0]	0x13[9:0]	0	OFFSET_CH4	value to be subtracted from channel 4 code
19[15:11]	0x13[15:11]	0	DIGITAL_GAIN_CH4	0dB to 6dB in 0.2dB steps
21[0]	0x15[0]	0	DIGITAL_HPF_FILTER_ENABLE _ CH1-4	0: Disable the digital HPF filter; 1: Enable for 1-4 channels
21[4:1]	0x15[4:1]	0	DIGITAL_HPF_FILTER_K_CH1-4	Set K for the high-pass filter (k from 2 to 10, i.e. 0010B to 1010B). This group of four registers controls the characteristics of a digital high-pass transfer function applied to the output data, following the formula: $y(n) = 2^k/(2^k + 1) [x(n) – x(n – 1) + y(n – 1)]$ (please see Table 3)
25[9:0]	0x19[9:0]	0	OFFSET_CH8	value to be subtracted from channel 8 code
25[15:11]	0x19[15:11]	0	DIGITAL_GAIN_CH8	0dB to 6dB in 0.2dB steps
27[9:0]	0x1B[9:0]	0	OFFSET_CH7	value to be subtracted from channel 7 code
27[15:11]	0x1B[15:11]	0	DIGITAL_GAIN_CH7	0dB to 6dB in 0.2dB steps
29[9:0]	0x1D[9:0]	0	OFFSET_CH6	value to be subtracted from channel 6 code
29[15:11]	0x1D[15:11]	0	DIGITAL_GAIN_CH6	0dB to 6dB in 0.2dB steps
31[9:0]	0x1F[9:0]	0	OFFSET_CH5	value to be subtracted from channel 5 code
31[15:11]	0x1F[15:11]	0	DIGITAL_GAIN_CH5	0dB to 6dB in 0.2dB steps
33[0]	0x21[0]	0	DIGITAL_HPF_FILTER_ENABLE _ CH5-8	0: Disable the digital HPF filter; 1: Enable for 5-8 channels
33[4:1]	0x21[4:1]	0	DIGITAL_HPF_FILTER_K_CH5-8	Set K for the high-pass filter (k from 2 to 10, 0010B to 1010B) This group of four registers controls the characteristics of a digital high-pass transfer function applied to the output data, following the formula: $y(n) = 2^k/(2^k + 1) [x(n) – x(n – 1) + y(n – 1)]$ (please see Table 3)
66[15]	0x42[15]	0	DITHER	0: Enable dither function. Improve the ADC linearity with slightly noise degradation. 1:Disable dither function.

ADC Register/Digital Processing Description

The ADC in the AFE5807 has extensive digital processing functionalities which can be used to enhance ultrasound system performance. The digital processing blocks are arranged as in Figure 63.

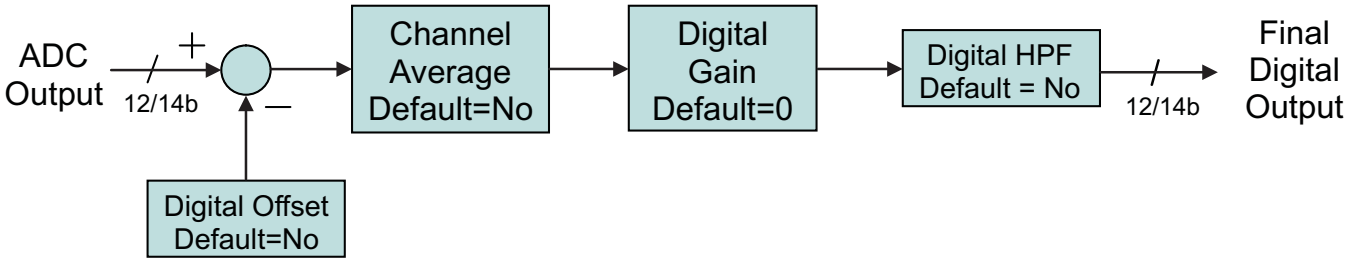


Figure 63. ADC Digital Block Diagram

AVERAGING_ENABLE: Address: 2[11]

When set to 1, two samples, corresponding to two consecutive channels, are averaged (channel 1 with 2, 3 with 4, 5 with 6, and 7 with 8). If both channels receive the same input, the net effect is an improvement in SNR. The averaging is performed as:

- Channel 1 + channel 2 comes out on channel 3
- Channel 3 + channel 4 comes out on channel 4
- Channel 5 + channel 6 comes out on channel 5
- Channel 7 + channel 8 comes out on channel 6

ADC_OUTPUT_FORMAT: Address: 4[3]

The ADC output, by default, is in 2's-complement mode. Programming the ADC_OUTPUT_FORMAT bit to 1 inverts the MSB, and the output becomes straight-offset binary mode.

DIGITAL_GAIN_ENABLE: Address: 3[12]

Setting this bit to 1 applies to each channel i the corresponding gain given by DIGTAL_GAIN_CHi <15:11>. The gain is given as 0dB + 0.2dB × DIGTAL_GAIN_CHi<15:11>. For instance, if DIGTAL_GAIN_CH5<15:11> = 3, channel 5 is increased by 0.6dB gain. DIGTAL_GAIN_CHi <15:11> = 31 produces the same effect as DIGTAL_GAIN_CHi <15:11> = 30, setting the gain of channel i to 6dB.

DIGITAL_HPF_ENABLE

- CH1-4: Address 21[0]
- CH5-8: Address 33[0]

DIGITAL_HPF_FILTER_K_CHX

- CH1-4: Address 21[4:1]
- CH5-8: Address 33[4:1]

This group of registers controls the characteristics of a digital high-pass transfer function applied to the output data, following Equation 1.

$$y(n) = \frac{2^k}{2^k + 1}\left[x(n) - x(n-1) + y(n-1)\right] \quad (1)$$

These digital HPF registers (one for the first four channels and one for the second group of four channels) describe the setting of K. The digital high pass filter can be used to suppress low frequency noise which commonly exists in ultrasound echo signals. The digital filter can significantly benefit near field recovery time due to T/R switch low frequency response. Table 3 shows the cut-off frequency vs K.

Table 3. Digital HPF –1dB Corner Frequency vs. K and Fs

k	40 MSPS	50 MSPS	65 MSPS
2	2780 KHz	3480 KHz	4520 KHz
3	1490 KHz	1860 KHz	2420 KHz
4	770 KHz	960 KHz	1250 KHz

LOW_FREQUENCY_NOISE_SUPPRESSION: Address: 1[11]

The low-frequency noise suppression mode is especially useful in applications where good noise performance is desired in the frequency band of 0MHz to 1MHz (around dc). Setting this mode shifts the low-frequency noise of the AFE5807 to approximately Fs/2, thereby moving the noise floor around dc to a much lower value. Register bit 1[11] is used for enabling or disabling this feature. When this feature is enabled, power consumption of the device will be increased slightly by approximate 1mW/CH.

LVDS_OUTPUT_RATE_2X: Address: 1[14]

The output data always uses a DDR format, with valid/different bits on the positive as well as the negative edges of the LVDS bit clock, DCLK. The output rate is set by default to 1X (LVDS_OUTPUT_RATE_2X = 0), where each ADC has one LVDS stream associated with it. If the sampling rate is low enough, two ADCs can share one LVDS stream, in this way lowering the power consumption devoted to the interface. The unused outputs will output zero. To avoid consumption from those outputs, no termination should be connected to them. The distribution on the used output pairs is done in the following way:

- Channel 1 and channel 2 come out on channel 3. Channel 1 comes out first.
- Channel 3 and channel 4 come out on channel 4. Channel 3 comes out first.
- Channel 5 and channel 6 come out on channel 5. Channel 5 comes out first.
- Channel 7 and channel 8 come out on channel 6. Channel 7 comes out first

CHANNEL_OFFSET_SUBSTRACTION_ENABLE: Address: 3[8]

Setting this bit to 1 enables the subtraction of the value on the corresponding OFFSET_CHx<9:0> (offset for channel i) from the ADC output. The number is specified in 2s-complement format. For example, OFFSET_CHx<9:0> = 11 1000 0000 means subtract –128. For OFFSET_CHx<9:0> = 00 0111 1111 the effect is to subtract 127. In effect, both addition and subtraction can be performed. Note that the offset is applied before the digital gain (see DIGITAL_GAIN_ENABLE). The whole data path is 2s-complement throughout internally, with digital gain being the last step. Only when ADC_OUTPUT_FORMAT = 1 (straight binary output format) is the 2s-complement word translated into offset binary at the end.

SERIALIZED_DATA_RATE: Address: 3[14:13]

Please see Table 1 for detail description.

TEST_PATTERN_MODES: Address: 2[15:13]

The AFE5807 can output a variety of test patterns on the LVDS outputs. These test patterns replace the normal ADC data output. The device may also be made to output 6 preset patterns:

1. **Ramp:** Setting Register 2[15:13]=111causes all the channels to output a repeating full-scale ramp pattern. The ramp increments from zero code to full-scale code in steps of 1LSB every clock cycle. After hitting the full-scale code, it returns back to zero code and ramps again.
2. **Zeros:** The device can be programmed to output all zeros by setting Register 2[15:13]=110;
3. **Ones:** The device can be programmed to output all 1s by setting Register 2[15:13]=100;
4. **Deskew Patten:** When 2[15:13]= 010; this mode replaces the 14-bit ADC output with the 01010101010101 word.
5. **Sync Pattern:** When 2[15:13]= 001, the normal ADC output is replaced by a fixed 11111110000000 word.
6. **Toggle:** When 2[15:13]=101, the normal ADC output is alternating between 1's and 0's. The start state of ADC word can be either 1's or 0's.
7. **Custom Pattern:** It can be enabled when 2[15:13]= 011;. Users can write the required VALUE into register bits <CUSTOM PATTERN> which is Register 5[13:0]. Then the device will output VALUE at its outputs, about 3 to 4 ADC clock cycles after the 24th rising edge of SCLK. So, the time taken to write one value is 24

SCLK clock cycles + 4 ADC clock cycles. To change the customer pattern value, users can repeat writing Register 5[13:0] with a new value. Due to the speed limit of SPI, the refresh rate of the custom pattern may not be high. For example, 128 points custom pattern will take approximately 128 x (24 SCLK clock cycles + 4 ADC clock cycles).

NOTE

only one of the above patterns can be active at any given instant.

SYNC: Address: 10[8]

By enabling this bit, all channels' test pattern outputs are synchronized. When 10[8] is set as 1, the ramp patterns of all 8 channels start simultaneously.

VCA Register Map

Table 4. VCA Register Map

ADDRESS (DEC)	ADDRESS (HEX)	Default Value	FUNCTION	DESCRIPTION
51[0]	0x33[0]	0	RESERVED	0
51[3:1]	0x33[3:1]	0	LPF_PROGRAMMABILITY	000: 15MHz, 010: 20MHz, 011: 30MHz, 100: 10MHz
51[4]	0x33[4]	0	PGA_INTEGRATOR_DISABLE (PGA_HPF_DISABLE)	0: Enable 1: Disables offset integrator for PGA. Please see explanation for the PGA integrator function in APPLICATION INFORMATION section
51[7:5]	0x33[7:5]	0	PGA_CLAMP_LEVEL	Low power mode/medium power mode: 53[11:10]=00/10 100: –2 dBFS 110: 0 dBFS 0XX: Clamp is disabled Low noise mode; 53[11:10]=01 000: –2 dBFS 010: 0 dBFS 1XX: clamp is disabled Note: the clamp circuit makes sure that PGA output is in linear range. For example, at 000 setting, PGA output HD3 will be worsen by 3 dB at –2 dBFS ADC input. In normal operation, clamp function can be set as 000 in the low noise mode. The maximum PGA output level can exceed 2Vpp with the clamp circuit enabled. Note: in the low power and medium power modes, PGA_CLAMP is disabled for saving power if 51[7]=0.
51[13]	0x33[13]	0	PGA_GAIN_CONTROL	0:24dB; 1:30dB.
52[4:0]	0x34[4:0]	0	ACTIVE_TERMINATION_ INDIVIDUAL_RESISTOR_CNTL	SeeTable 6 Reg 52[5] should be set as '1' to access these bits
52[5]	0x34[5]	0	ACTIVE_TERMINATION_ INDIVIDUAL_RESISTOR_ENABLE	0: Disables; 1: Enables internal active termination individual resistor control
52[7:6]	0x34[7:6]	0	PRESET_ACTIVE_ TERMINATIONS	00: 50ohm, 01: 100ohm, 10: 200ohm, 11: 400ohm. (Note: the device will adjust resistor mapping (52[4:0]) automatically. 50ohm active termination is NOT supported in 12dB LNA setting. Instead, '00' represents high impedance mode when LNA gain is 12dB)
52[8]	0x34[8]	0	ACTIVE TERMINATION ENABLE	0: Disables; 1: Enables active termination
52[10:9]	0x34[10:9]	0	LNA_INPUT_CLAMP_SETTING	00: Auto setting, 01: 1.5Vpp, 10: 1.15Vpp and 11: 0.6Vpp
52[11]	0x34[11]	0	RESERVED	Set to 0
52[12]	0x34[12]	0	LNA_INTEGRATOR_DISABLE (LNA_HPF_DISABLE)	0: Enables; 1: Disables offset integrator for LNA. Please see the explanation for this function in the following section
52[14:13]	0x34[14:13]	0	LNA_GAIN	00: 18dB; 01: 24dB; 10: 12dB; 11: Reserved
52[15]	0x34[15]	0	LNA_INDIVIDUAL_CH_CNTL	0: Disable; 1: Enable LNA individual channel control. See Register 57 for details

Table 4. VCA Register Map (continued)

ADDRESS (DEC)	ADDRESS (HEX)	Default Value	FUNCTION	DESCRIPTION
53[7:0]	0x35[7:0]	0	PDN_CH<7:0>	0: Normal operation; 1: Powers down corresponding channels. Bit7→CH8, Bit6→CH7…Bit0→CH1. PDN_CH will shut down whichever blocks are active depending on TGC mode or CW mode
53[8]	0x35[8]	0	RESERVED	Set to 0
53[9]	0x35[9]	0	RESERVED	Set to 0
53[11:10]	0x35[11:10]	0	POWER_MODES	00: Low power mode. At 30dB PGA, total chain gain may slightly change. See typical characteristics 01: Low noise mode. 10:Medium power mode.At 30dB PGA, total chain gain may slightly change. See typical characteristics 11: Reserved
53[12]	0x35[12]	0	PDN_VCAT_PGA	0: Normal operation; 1: Powers down VCAT (voltage-controlled-attenuator) and PGA
53[13]	0x35[13]	0	PDN_LNA	0: Normal operation; 1: Powers down LNA only
53[14]	0x35[14]	0	VCA_PARTIAL_PDN	0: Normal operation; 1: Powers down LNA, VCAT, and PGA partially(fast wake response)
53[15]	0x35[15]	0	VCA_COMPLETE_PDN	0: Normal operation; 1: Powers down LNA, VCAT, and PGA completely (slow wake response). This bit can overwrite 53[14].
54[4:0]	0x36[4:0]	0	CW_SUM_AMP_GAIN_CNTL	Selects Feedback resistor for the CW Amplifier as per Table 6 below
54[5]	0x36[5]	0	CW_16X_CLK_SEL	0: Accepts differential clock; 1: Accepts CMOS clock
54[6]	0x36[6]	0	CW_1X_CLK_SEL	0: Accepts CMOS clock; 1: Accepts differential clock
54[7]	0x36[7]	0	RESERVED	Set to 0
54[8]	0x36[8]	0	CW_TGC_SEL	0: TGC Mode; 1 : CW Mode Note : VCAT and PGA are still working in CW mode. They should be powered down separately through 53[12]. In addition, it is recommended to program the AFE5807 as low noise mode in the CW mode through the register 53[10:11].
54[9]	0x36[9]	0	CW_SUM_AMP_ENABLE	0: enables CW summing amplifier; 1: disables CW summing amplifier Note: 54[9] is only effective in CW mode.
54[11:10]	0x36[11:10]	0	CW_CLK_MODE_SEL	00: 16X mode; 01: 8X mode; 10: 4X mode; 11: 1X mode
55[3:0]	0x37[3:0]	0	CH1_CW_MIXER_PHASE	0000→1111, 16 different phase delays, see Table 9
55[7:4]	0x37[7:4]	0	CH2_CW_MIXER_PHASE	
55[11:8]	0x37[11:8]	0	CH3_CW_MIXER_PHASE	
55[15:12]	0x37[15:12]	0	CH4_CW_MIXER_PHASE	
56[3:0]	0x38[3:0]	0	CH5_CW_MIXER_PHASE	
56[7:4]	0x38[7:4]	0	CH6_CW_MIXER_PHASE	
56[11:8]	0x38[11:8]	0	CH7_CW_MIXER_PHASE	
56[15:12]	0x38[15:12]	0	CH8_CW_MIXER_PHASE	

Table 4. VCA Register Map (continued)

ADDRESS (DEC)	ADDRESS (HEX)	Default Value	FUNCTION	DESCRIPTION
57[1:0]	0x39[1:0]	0	CH1_LNA_GAIN_CNTL	00: 18dB; 01: 24dB; 10: 12dB; 11: Reserved REG52[15] should be set as '1'
57[3:2]	0x39[3:2]	0	CH2_LNA_GAIN_CNTL	
57[5:4]	0x39[5:4]	0	CH3_LNA_GAIN_CNTL	00: 18dB; 01: 24dB; 10: 12dB; 11: Reserved REG52[15] should be set as '1'
57[7:6]	0x39[7:6]	0	CH4_LNA_GAIN_CNTL	
57[9:8]	0x39[9:8]	0	CH5_LNA_GAIN_CNTL	
57[11:10]	0x39[11:10]	0	CH6_LNA_GAIN_CNTL	
57[13:12]	0x39[13:12]	0	CH7_LNA_GAIN_CNTL	
57[15:14]	0x39[15:14]	0	CH8_LNA_GAIN_CNTL	
59[3:2]	0x3B[3:2]	0	HPF_LNA	00: 100KHz; 01: 50Khz; 10: 200Khz; 11: 150KHz with 0.015uF on INMx
59[6:4]	0x3B[6:4]	0	DIG_TGC_ATT_GAIN	000: 0dB attenuation; 001: 6dB attenuation; N: ~N×6dB attenuation when 59[7] = 1
59[7]	0x3B[7]	0	DIG_TGC_ATT	0: disable digital TGC attenuator; 1: enable digital TGC attenuator
59[8]	0x3B[8]	0	CW_SUM_AMP_PDN	0: Power down; 1: Normal operation Note: 59[8] is only effective in TGC test mode.
59[9]	0x3B[9]	0	PGA_TEST_MODE	0: Normal CW operation; 1: PGA outputs appear at CW outputs

VCA Register Description

LNA Input Impedances Configuration (Active Termination Programmability)

Different LNA input impedances can be configured through the register 52[4:0]. By enabling and disabling the feedback resistors between LNA outputs and ACTx pins, LNA input impedance is adjustable accordingly. Table 5 describes the relationship between LNA gain and 52[4:0] settings. The input impedance settings are the same for both TGC and CW paths.

The AFE5807 also has 4 preset active termination impedances as described in 52[7:6]. An internal decoder is used to select appropriate resistors corresponding to different LNA gain.

Table 5. Register 52[4:0] Description

52[4:0]/0x34[4:0]	FUNCTION
00000	No feedback resistor enabled
00001	Enables 450 Ω feedback resistor
00010	Enables 900 Ω feedback resistor
00100	Enables 1800 Ω feedback resistor
01000	Enables 3600 Ω feedback resistor
10000	Enables 4500 Ω feedback resistor

Table 6. Register 52[4:0] vs LNA Input Impedances

52[4:0]/0x34[4:0]	00000	00001	00010	00011	00100	00101	00110	00111
LNA:12dB	High Z	150 Ω	300 Ω	100 Ω	600 Ω	120 Ω	200 Ω	86 Ω
LNA:18dB	High Z	90 Ω	180 Ω	60 Ω	360 Ω	72 Ω	120 Ω	51 Ω
LNA:24dB	High Z	50 Ω	100 Ω	33 Ω	200 Ω	40 Ω	66.67 Ω	29 Ω
52[4:0]/0x34[4:0]	01000	01001	01010	01011	01100	01101	01110	01111
LNA:12dB	1200 Ω	133 Ω	240 Ω	92 Ω	400 Ω	109 Ω	171 Ω	80 Ω
LNA:18dB	720 Ω	80 Ω	144 Ω	55 Ω	240 Ω	65 Ω	103 Ω	48 Ω
LNA:24dB	400 Ω	44 Ω	80 Ω	31 Ω	133 Ω	36 Ω	57 Ω	27 Ω
52[4:0]/0x34[4:0]	10000	10001	10010	10011	10100	10101	10110	10111
LNA:12dB	1500 Ω	136 Ω	250 Ω	94 Ω	429 Ω	111 Ω	176 Ω	81 Ω
LNA:18dB	900 Ω	82 Ω	150 Ω	56 Ω	257 Ω	67 Ω	106 Ω	49 Ω
LNA:24dB	500 Ω	45 Ω	83 Ω	31 Ω	143 Ω	37 Ω	59 Ω	27 Ω
52[4:0]/0x34[4:0]	11000	11001	11010	11011	11100	11101	11110	11111
LNA:12dB	667 Ω	122 Ω	207 Ω	87 Ω	316 Ω	102 Ω	154 Ω	76 Ω
LNA:18dB	400 Ω	73 Ω	124 Ω	52 Ω	189 Ω	61 Ω	92 Ω	46 Ω
LNA:24dB	222 Ω	41 Ω	69 Ω	29 Ω	105 Ω	34 Ω	51 Ω	25 Ω

Programmable Gain for CW Summing Amplifier

Different gain can be configured for the CW summing amplifier through the register 54[4:0]. By enabling and disabling the feedback resistors between the summing amplifier inputs and outputs, the gain is adjustable accordingly to maximize the dynamic range of CW path. Table 7 describes the relationship between the summing amplifier gain and 54[4:0] settings.

Table 7. Register 54[4:0] Description

54[4:0]/0x36[4:0]	FUNCTION
00000	No feedback resistor
00001	Enables 250 Ω feedback resistor
00010	Enables 250 Ω feedback resistor
00100	Enables 500 Ω feedback resistor
01000	Enables 1000 Ω feedback resistor
10000	Enables 2000 Ω feedback resistor

Table 8. Register 54[4:0] vs Summing Amplifier Gain

54[4:0]/0x36[4:0]	**00000**	**00001**	**00010**	**00011**	**00100**	**00101**	**00110**	**00111**
CW I/V Gain	N/A	0.50	0.50	0.25	1.00	0.33	0.33	0.20
54[4:0]/0x36[4:0]	**01000**	**01001**	**01010**	**01011**	**01100**	**01101**	**01110**	**01111**
CW I/V Gain	2.00	0.40	0.40	0.22	0.67	0.29	0.29	0.18
54[4:0]/0x36[4:0]	**10000**	**10001**	**10010**	**10011**	**10100**	**10101**	**10110**	**10111**
CW I/V Gain	4.00	0.44	0.44	0.24	0.80	0.31	0.31	0.19
54[4:0]/0x36[4:0]	**11000**	**11001**	**11010**	**11011**	**11100**	**11101**	**11110**	**11111**
CW I/V Gain	1.33	0.36	0.36	0.21	0.57	0.27	0.27	0.17

Programmable Phase Delay for CW Mixer

Accurate CW beamforming is achieved through adjusting the phase delay of each channel. In the AFE5807, 16 different phase delays can be applied to each LNA output; and it meets the standard requirement of typical ultrasound beamformer, i.e. $\frac{1}{16}\lambda$ beamformer resolution. Table 7 describes the relationship between the phase delays and the register 55 and 56 settings.

Table 9. CW Mixer Phase Delay vs Register Settings
CH1 - 55[3:0], CH2 - 55[7:4], CH3 - 55[11:8], CH4 - 55[15:12],
CH5- 56[3:0], CH6 - 56[7:4], CH7 - 56[11:8], CH8 - 56[15:12],

CHX_CW_MIXER_PHASE	0000	0001	0010	0011	0100	0101	0110	0111
PHASE SHIFT	0	22.5°	45°	67.5°	90°	112.5°	135°	157.5°
CHX_CW_MIXER_PHASE	1000	1001	1010	1011	1100	1101	1110	1111
PHASE SHIFT	180°	202.5°	225°	247.5°	270°	292.5°	315°	337.5°

THEORY OF OPERATION

AFE5807 OVERVIEW

The AFE5807 is an integrated Analog Front-End (AFE) solution specifically designed for ultrasound systems in which high performance and small size are required. The AFE5807 integrates a complete time-gain-control (TGC) imaging path and a continuous wave Doppler (CWD) path. It also enables users to select one of various power/noise combinations to optimize system performance. The AFE5807 contains eight channels; each channels includes a Low-Noise Amplifier (LNA), a Voltage Controlled Attenuator (VCAT), a Programmable Gain Amplifier (PGA), a Low-pass Filter (LPF), a 12-bit Analog-to-Digital Converter (ADC), and a CW mixer.

In addition, multiple features in the AFE5807 are suitable for ultrasound applications, such as active termination, individual channel control, fast power up/down response, programmable clamp voltage control, fast and consistent overload recovery, etc. Therefore, the AFE5807 brings premium image quality to ultra–portable, handheld systems all the way up to high-end ultrasound systems. Its simplified function block diagram is listed in Figure 64.

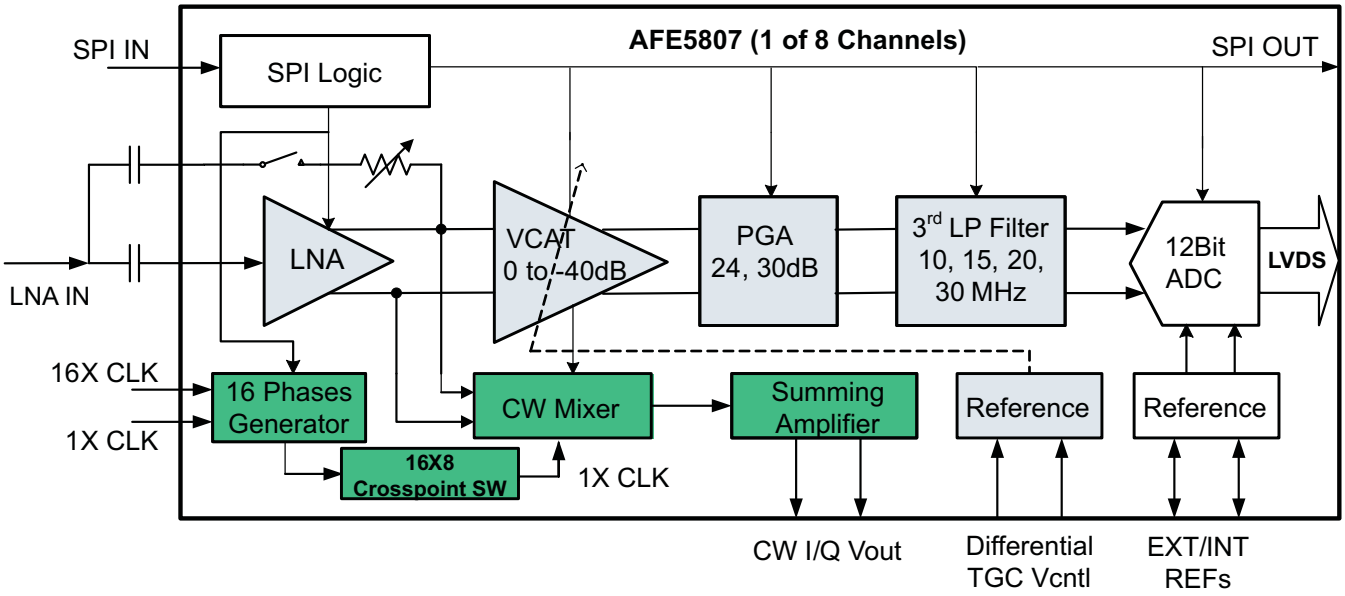


Figure 64. Functional Block Diagram

LOW-NOISE AMPLIFIER (LNA)

In many high-gain systems, a low noise amplifier is critical to achieve overall performance. Using a new proprietary architecture, the LNA in the AFE5807 delivers exceptional low-noise performance, while operating on a very low quiescent current compared to CMOS-based architectures with similar noise performance. The LNA performs single-ended input to differential output voltage conversion. It is configurable for a programmable gain of 24/18/12dB and its input-referred noise is only 0.63/0.70/0.9nV/√Hz respectively. Programmable gain settings result in a flexible linear input range up to 1Vpp, realizing high signal handling capability demanded by new transducer technologies. Larger input signal can be accepted by the LNA; however the signal can be distorted since it exceeds the LNA's linear operation region. Combining the low noise and high input range, a wide input dynamic range is achieved consequently for supporting the high demands from various ultrasound imaging modes.

The LNA input is internally biased at approximately +2.4V; the signal source should be ac-coupled to the LNA input by an adequately-sized capacitor, e.g. ≥0.1uF. To achieve low DC offset drift, the AFE5807 incorporates a DC offset correction circuit for each amplifier stage. To improve the overload recovery, an integrator circuit is used to extract the DC component of the LNA output and then fed back to the LNA's complementary input for DC offset correction. This DC offset correction circuit has a high-pass response and can be treated as a high-pass

filter. The effective corner frequency is determined by the capacitor C_{BYPASS} connected at INM. With larger capacitors, the corner frequency is lower. For stable operation at the highest HP filer cut-off frequency, a ≥15nF capacitor can be selected. This corner frequency scales almost linearly with the value of the C_{BYPASS}. For example, 15nF gives a corner frequency of approximately 100 kHz, while 47nF can give an effective corner frequency of 33 KHz. The DC offset correction circuit can also be disabled/enabled through register 52[12].

The AFE5807 can be terminated passively or actively. Active termination is preferred in ultrasound application for reducing reflection from mismatches and achieving better axial resolution without degrading noise figure too much. Active termination values can be preset to 50, 100, 200, 400Ω; other values also can be programmed by users through register 52[4:0]. A feedback capacitor is required between ACTx and the signal source as Figure 65 shows. On the active termination path, a clamping circuit is also used to create a low impedance path when overload signal is seen by the AFE5807. The clamp circuit limits large input signals at the LNA inputs and improves the overload recovery performance of the AFE5807. The clamp level can be set to 350mVpp, 600mVpp, 1.15Vpp automatically depending on the LNA gain settings when register 52[10:9]=0. Other clamp voltages, such as 1.15Vpp, 0.6Vpp, and 1.5Vpp, are also achievable by setting register 52[10:9]. This clamping circuit is also designed to obtain good pulse inversion performance and reduce the impact from asymmetric inputs.

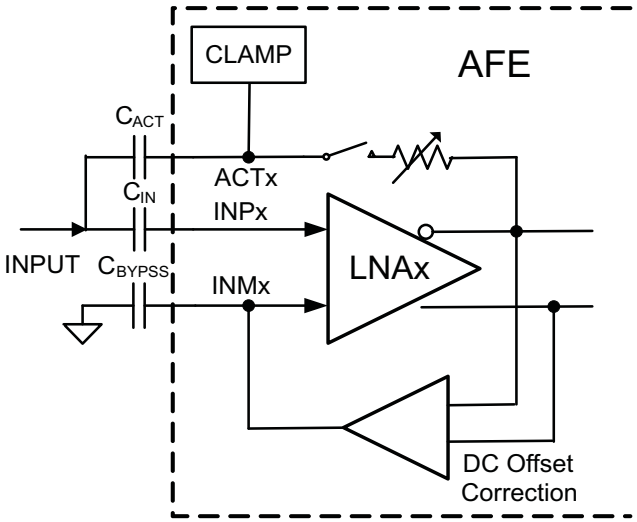


Figure 65. AFE5807 LNA with DC Offset Correction Circuit

VOLTAGE-CONTROLLED ATTENUATOR

The voltage-controlled attenuator is designed to have a linear-in-dB attenuation characteristic; that is, the average gain loss in dB (see Figure 2) is constant for each equal increment of the control voltage (VCNTL) as shown in Figure 66. A differential control structure is used to reduce common mode noise. A simplified attenuator structure is shown in the following Figure 66 and Figure 67.

The attenuator is essentially a variable voltage divider that consists of the series input resistor (RS) and seven shunt FETs placed in parallel and controlled by sequentially activated clipping amplifiers (A1 through A7). VCNTL is the effective difference between VCNTLP and VCNTLM. Each clipping amplifier can be understood as a specialized voltage comparator with a soft transfer characteristic and well-controlled output limit voltage. Reference voltages V1 through V7 are equally spaced over the 0V to 1.5V control voltage range. As the control voltage increases through the input range of each clipping amplifier, the amplifier output rises from a voltage where the FET is nearly OFF to VHIGH where the FET is completely ON. As each FET approaches its ON state and the control voltage continues to rise, the next clipping amplifier/FET combination takes over for the next portion of the piecewise-linear attenuation characteristic. Thus, low control voltages have most of the FETs turned OFF, producing minimum signal attenuation. Similarly, high control voltages turn the FETs ON, leading to maximum signal attenuation. Therefore, each FET acts to decrease the shunt resistance of the voltage divider formed by Rs and the parallel FET network.

Additionally, a digitally controlled TGC mode is implemented to achieve better phase-noise performance in the AFE5807. The attenuator can be controlled digitally instead of the analog control voltage V_{CNTL}. This mode can be set by the register bit 59[7]. The variable voltage divider is implemented as a fixed series resistance and FET as the shunt resistance. Each FET can be turned ON by connecting the switches SW1-7. Turning on each of the switches can give approximately 6dB of attenuation. This can be controlled by the register bits 59[6:4]. This digital control feature can eliminate the noise from the VCNTL circuit and ensure the better SNR and phase noise for the TGC path.

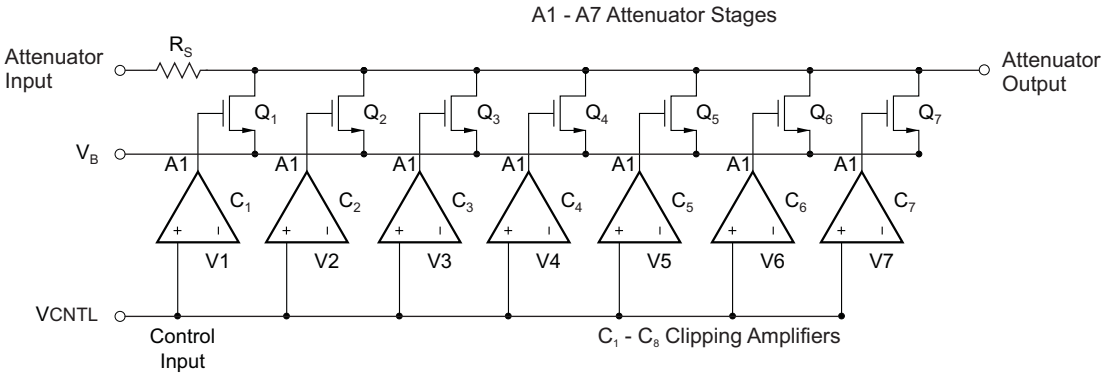


Figure 66. Simplified Voltage Controlled Attenuator (Analog Structure)

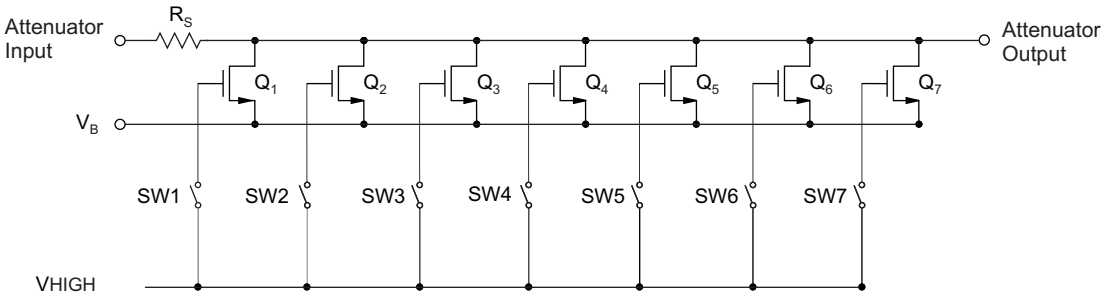


Figure 67. Simplified Voltage Controlled Attenuator (Digital Structure)

The voltage controlled attenuator's noise follows a monotonic relationship to the attenuation coefficient. AAt higher attenuation, the input-referred noise is higher and vice-versa. The attenuator's noise is then amplified by the PGA and becomes the noise floor at ADC input. In the attenuator's high attenuation operating range, i.e. VCNTL is high, the attenuator's input noise may exceed the LNA's output noise; the attenuator then becomes the dominant noise source for the following PGA stage and ADC. Therefore the attenuator's noise should be minimized compared to the LNA output noise. The AFE5807's attenuator is designed for achieving very low noise even at high attenuation (low channel gain) and realizing better SNR in near field. The input referred noise for different attenuations is listed in the below table:

Table 10. Voltage-Controlled-Attenuator noise vs Attenuation

Attenuation (dB)	Attenuator Input Referred noise (nV/rtHz)
–40	10.5
–36	10
–30	9
–24	8.5
–18	6
–12	4
–6	3
0	2

PROGRAMMABLE GAIN AMPLIFIER (PGA)

After the voltage controlled attenuator, a programmable gain amplifier can be configured as 24dB or 30dB with a constant input referred noise of 1.75nV/rtHz. The PGA structure consists of a differential voltage-to-current converter with programmable gain, current clamp(bias control) circuits, a transimpedance amplifier with a programmable low-pass filter, and a DC offset correction circuit. Its simplified block diagram is shown below:

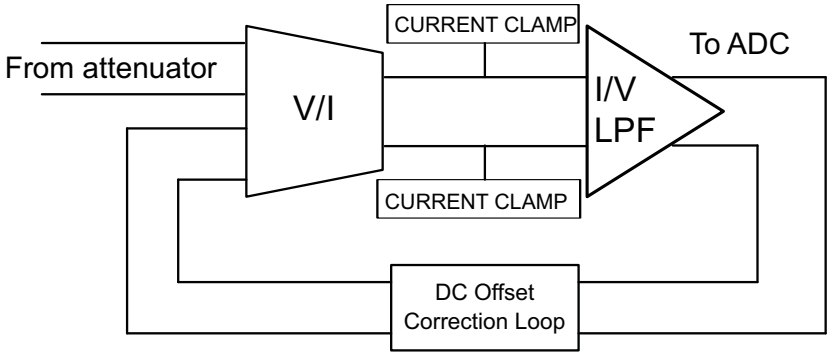


Figure 68. Simplified Block Diagram of PGA

Low input noise is always preferred in a PGA and its noise contribution should not degrade the ADC SNR too much after the attenuator. At the minimum attenuation (used for small input signals), the LNA noise dominates; at the maximum attenuation (large input signals), the PGA and ADC noise dominates. Thus 24dB gain of PGA achieves better SNR as long as the amplified signals can exceed the noise floor of the ADC.

The PGA current clamp circuit can be enabled (register 51) to improve the overload recovery performance of the AFE. If we measure the standard deviation of the output just after overload, for 0.5V V_{CNTL}, it is about 3.2 LSBs in normal case, i.e the output is stable in about 1 clock cycle after overload. With the current clamp circuit disabled, the value approaches 4 LSBs meaning a longer time duration before the output stabilizes; however, with the current clamp circuit enabled, there will be degradation in HD3 for PGA output levels > -2dBFS. For example, for a –2dBFS output level, the HD3 degrades by approximately 3dB.the ADC in the AFE has excellent overload recovery performance to detect small signals right after the overload. In order to maximize the output dynamic range, the maximum PGA output level can be above 2Vpp even with the clamp circuit enabled; the ADC in the AFE has excellent overload recovery performance to detect small signals right after the overload.

NOTE

In the low power and medium power modes, PGA_CLAMP is disabled for saving power if 51[7]=0

The AFE5807 integrates an anti-aliasing filter in the form of a programmable butterworth low-pass filter (LPF) in the transimpedance amplifier . The LPF is designed as a differential, active, 3rd order filter with a typical 18dB per octave roll-off. Programmable through the serial interface, the –1dB frequency corner can be set to one of 10MHz, 15MHz, 20MHz, and 30MHz. The filter bandwidth is set for all channels simultaneously.

A selectable DC offset correction circuit is implemented in the PGA as well. This correction circuit is similar to the one used in the LNA. It extracts the DC component of the PGA outputs and feeds back to the PGA's complimentary inputs for DC offset correction. This DC offset correction circuit also has a high-pass response with a cut-off frequency of 80KHz.

ANALOG TO DIGITAL CONVERTER

The analog-to-digital converter (ADC) of the AFE5807 employs a pipelined converter architecture that consists of a combination of multi-bit and single-bit internal stages. Each stage feeds its data into the digital error correction logic, ensuring excellent differential linearity and no missing codes at the 14-bit level. The 14 bits given out by each channel are serialized and sent out on a single pair of pins in LVDS format. All eight channels of the AFE5807 operate from a common input clock (CLKP/M). The sampling clocks for each of the eight channels are generated from the input clock using a carefully matched clock buffer tree. The 14x clock required for the

serializer is generated internally from the CLKP/M pins. A 7x and a 1x clock are also given out in LVDS format, along with the data, to enable easy data capture. The AFE5807 operates from internally-generated reference voltages that are trimmed to improve the gain matching across devices. The nominal values of REFP and REFM are 1.5V and 0.5V, respectively. Alternately, the device also supports an external reference mode that can be enabled using the serial interface.

Using serialized LVDS transmission has multiple advantages, such as a reduced number of output pins (saving routing space on the board), reduced power consumption, and reduced effects of digital noise coupling to the analog circuit inside the AFE5807.

CONTINUOUS-WAVE (CW) BEAMFORMER

Continuous-wave Doppler is a key function in mid-end to high-end ultrasound systems. Compared to the TGC mode, the CW path needs to handle high dynamic range along with strict phase noise performance. CW beamforming is often implemented in analog domain due to the mentioned strict requirements. Multiple beamforming methods are being implemented in ultrasound systems, including passive delay line, active mixer, and passive mixer. Among all of them, the passive mixer approach achieves optimized power and noise. It satisfies the CW processing requirements, such as wide dynamic range, low phase noise, accurate gain and phase matching.

A simplified CW path block diagram and an In-phase or Quadrature (I/Q) channel block diagram are illustrated below respectively. Each CW channel includes a LNA, a voltage-to-current converter, a switch-based mixer, a shared summing amplifier with a low-pass filter, and clocking circuits.

NOTE

The local oscillator inputs of the passive mixer are cos(ωt) for I-CH and sin(ωt) for Q-CH respectively. Depending on users' CW Doppler complex FFT processing, swapping I/Q channels in FPGA or DSP may be needed in order to get correct blood flow directions.

All blocks include well-matched in-phase and quadrature channels to achieve good image frequency rejection as well as beamforming accuracy. As a result, the image rejection ratio from an I/Q channel is better than -46dBc which is desired in ultrasound systems.

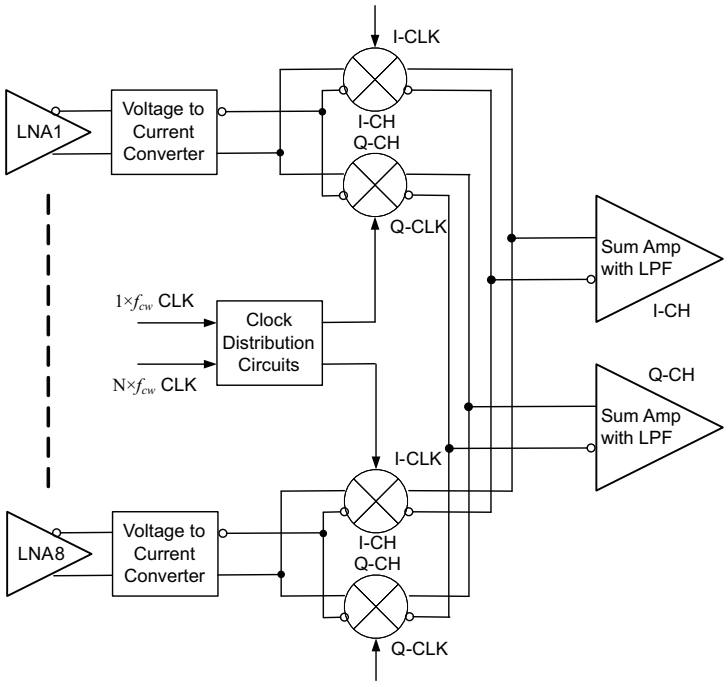
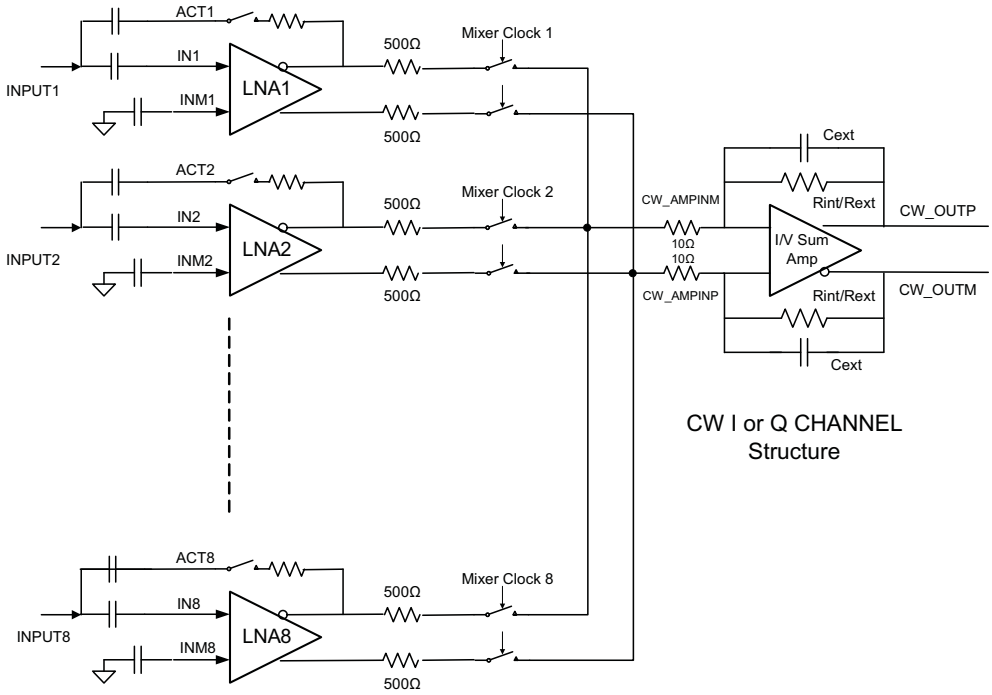


Figure 69. Simplified Block Diagram of CW Path



Note: the 10~15 Ω parasitic resistors at CW_AMPINM/P are due to internal IC routing and can create slight attenuation.

Figure 70. A Complete In-phase or Quadrature Phase Channel

The CW mixer in the AFE5807 is passive and switch based; passive mixer adds less noise than active mixers. It achieves good performance at low power. The below illustration and equations describe the principles of mixer operation, where Vi(t), Vo(t) and LO(t) are input, output and local oscillator (LO) signals for a mixer respectively. The LO(t) is square-wave based and includes odd harmonic components as the below equation expresses:

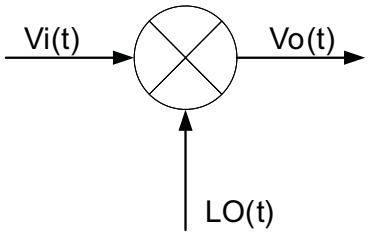


Figure 71. Block Diagram of Mixer Operation

$$Vi(t) = \sin\left(\omega_0 t + \omega_d t + \varphi\right) + f\left(\omega_0 t\right)$$

$$LO(t) = \frac{4}{\pi}\left[\sin\left(\omega_0 t\right) + \frac{1}{3}\sin\left(3\omega_0 t\right) + \frac{1}{5}\sin\left(5\omega_0 t\right)...\right]$$

$$Vo(t) = \frac{2}{\pi}\left[\cos\left(\omega_d t + \phi\right) - \cos\left(2\omega_0 t - \omega_d t + \phi\right)...\right] \quad (2)$$

From the above equations, the 3rd and 5th order harmonics from the LO can interface with the 3rd and 5th order harmonic signals in the Vi(t); or the noise around the 3rd and 5th order harmonics in the Vi(t). Therefore the mixer's performance is degraded. In order to eliminate this side effect due to the square-wave demodulation, a proprietary harmonic suppression circuit is implemented in the AFE5807. The 3rd and 5th harmonic components from the LO can be suppressed by over 12dB. Thus the LNA output noise around the 3rd and 5th order harmonic bands will not be down-converted to base band. Hence, better noise figure is achieved. The conversion loss of the mixer is about -4dB which is derived from $20\log_{10}\frac{2}{\pi}$

The mixed current outputs of the 8 channels are summed together internally. An internal low noise operational amplifier is used to convert the summed current to a voltage output. The internal summing amplifier is designed to accomplish low power consumption, low noise, and ease of use. CW outputs from multiple AFE5807s can be further combined on system board to implement a CW beamformer with more than 8 channels. More detail information can be found in the application information section.

Multiple clock options are supported in the AFE5807 CW path. Two CW clock inputs are required: N×f_{cw} clock and 1 × f_{cw} clock, where f_{cw} is the CW transmitting frequency and N could be 16, 8, 4, or 1. Users have the flexibility to select the most convenient system clock solution for the AFE5807. In the 16 × f_{cw} and 8×fcw modes, the 3rd and 5th harmonic suppression feature can be supported. Thus, the 16 × f_{cw} and 8 × f_{cw} modes achieves better performance than the 4 × f_{cw} and 1 × f_{cw} modes

16 × f_{cw} Mode

The 16 × f_{cw} mode achieves the best phase accuracy compared to other modes. It is the default mode for CW operation. In this mode, 16 × f_{cw} and 1 × f_{cw} clocks are required. 16×fcw generates LO signals with 16 accurate phases. Multiple AFE5807s can be synchronized by the 1 × f_{cw} , i.e. LO signals in multiple AFEs can have the same starting phase. The phase noise spec is critical only for 16X clock. 1X clock is for synchronization only and doesn't require low phase noise. Please see the phase noise requirement in the section of application information.

The top level clock distribution diagram is shown in the below Figure 72. Each mixer's clock is distributed through a 16 × 8 cross-point switch. The inputs of the cross-point switch are 16 different phases of the 1x clock. It is recommended to align the rising edges of the 1 x f_{cw} and 16 x f_{cw} clocks.

The cross-point switch distributes the clocks with appropriate phase delay to each mixer. For example, Vi(t) is a received signal with a delay of $\frac{1}{16}T$, a delayed LO(t) should be applied to the mixer in order to compensate for the $\frac{1}{16}T$ delay. Thus a 22.5º delayed clock, i.e. $\frac{2\pi}{16}$, is selected for this channel. The mathematic calculation is expressed in the following equations:

$$\mathrm{Vi}(t)=\sin\left[\omega_0\left(t+\frac{1}{16f_0}\right)+\omega_d t\right]=\sin\left[\omega_0 t+22.5^\circ+\omega_d t\right]$$

$$\mathrm{LO}(t)=\frac{4}{\pi}\sin\left[\omega_0\left(t+\frac{1}{16f_0}\right)\right]=\frac{4}{\pi}\sin\left[\omega_0 t+22.5^\circ\right]$$

$$\mathrm{Vo}(t)=\frac{2}{\pi}\cos\left(\omega_d t\right)+f\left(\omega_n t\right) \quad (3)$$

Vo(t) represents the demodulated Doppler signal of each channel. When the doppler signals from N channels are summed, the signal to noise ratio improves.

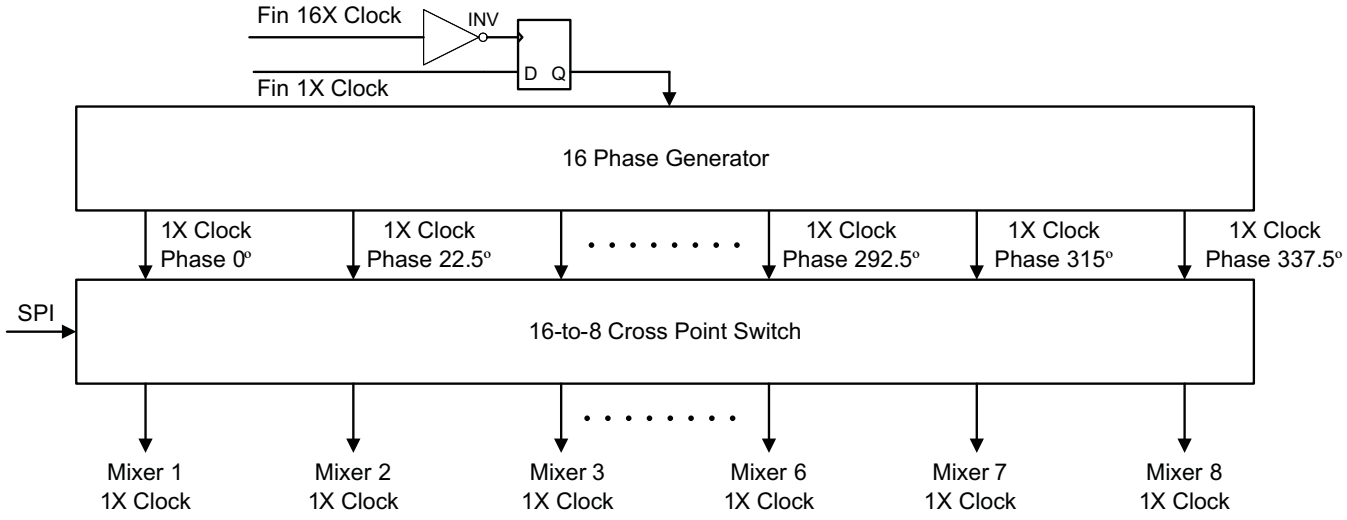


Figure 72.

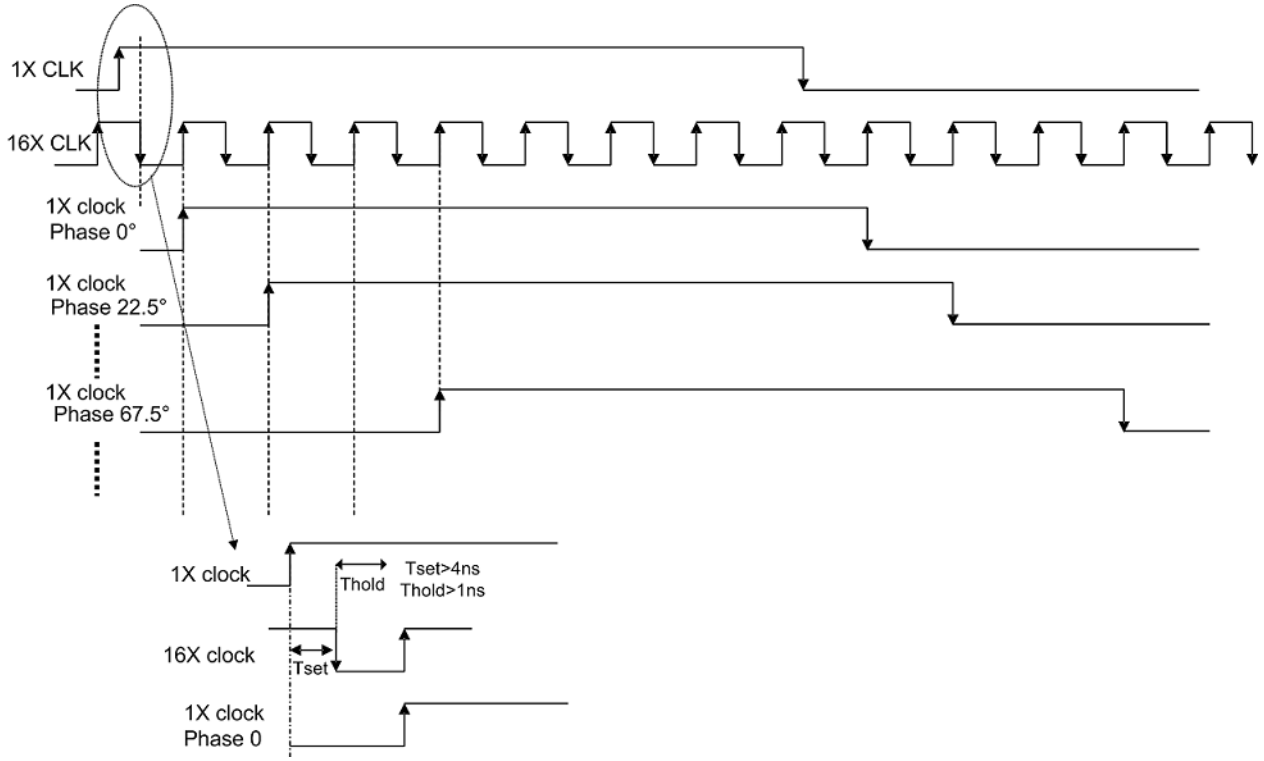


Figure 73. 1x and 16x CW Clock Timing

8 × f_{cw} and 4 × f_{cw} Modes

8 × f_{cw} and 4 × f_{cw} modes are alternative modes when higher frequency clock solution (i.e. 16 × f_{cw} clock) is not available in system. The block diagram of these two modes is shown below.

Good phase accuracy and matching are also maintained. Quadature clock generator is used to create in-phase and quadrature clocks with exact 90° phase difference. The only difference between 8 × f_{cw} and 4 × f_{cw} modes is the accessibility of the 3rd and 5th harmonic suppression filter. In the 8 × f_{cw} mode, the suppression filter can be supported. In both modes, $\frac{1}{16}T$ phase delay resolution is achieved by weighting the in-phase and quadrature paths correspondingly. For example, if a delay of $\frac{1}{16}T$ or 22.5° is targeted, the weighting coefficients should follow the below equations, assuming I_{in} and Q_{in} are sin($\omega_0 t$) and cos($\omega_0 t$) respectively:

$$I_{delayed}(t) = I_{in}\cos\left(\frac{2\pi}{16}\right) + Q_{in}\sin\left(\frac{2\pi}{16}\right) = I_{in}\left(t + \frac{1}{16 f_0}\right)$$

$$Q_{delayed}(t) = Q_{in}\cos\left(\frac{2\pi}{16}\right) - I_{in}\sin\left(\frac{2\pi}{16}\right) = Q_{in}\left(t + \frac{1}{16 f_0}\right) \quad (4)$$

Therefore after I/Q mixers, phase delay in the received signals is compensated. The mixers outputs from all channels are aligned and added linearly to improve the signal to noise ratio. It is preferred to have the 4 × f_{cw} or 8 × f_{cw} and 1 × f_{cw} clocks aligned both at the rising edge.

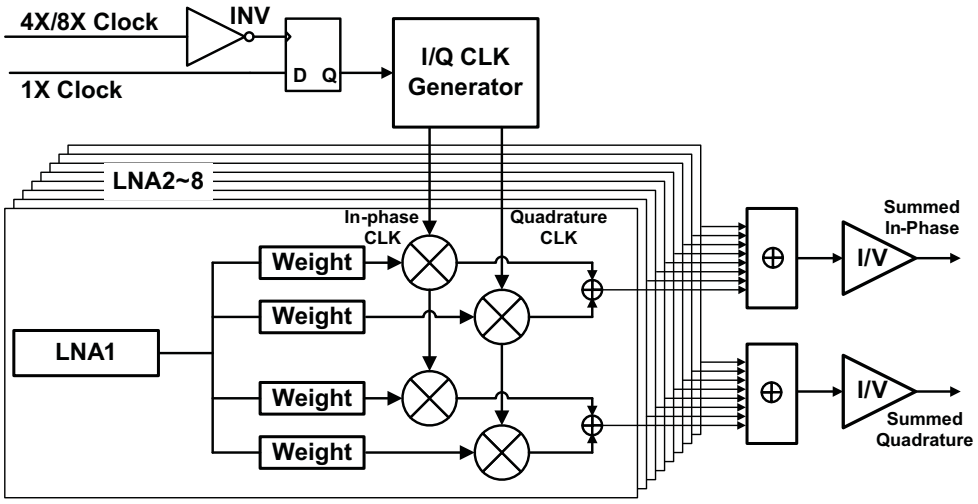


Figure 74. 8 X f_{cw} and 4 X f_{cw} Block Diagram

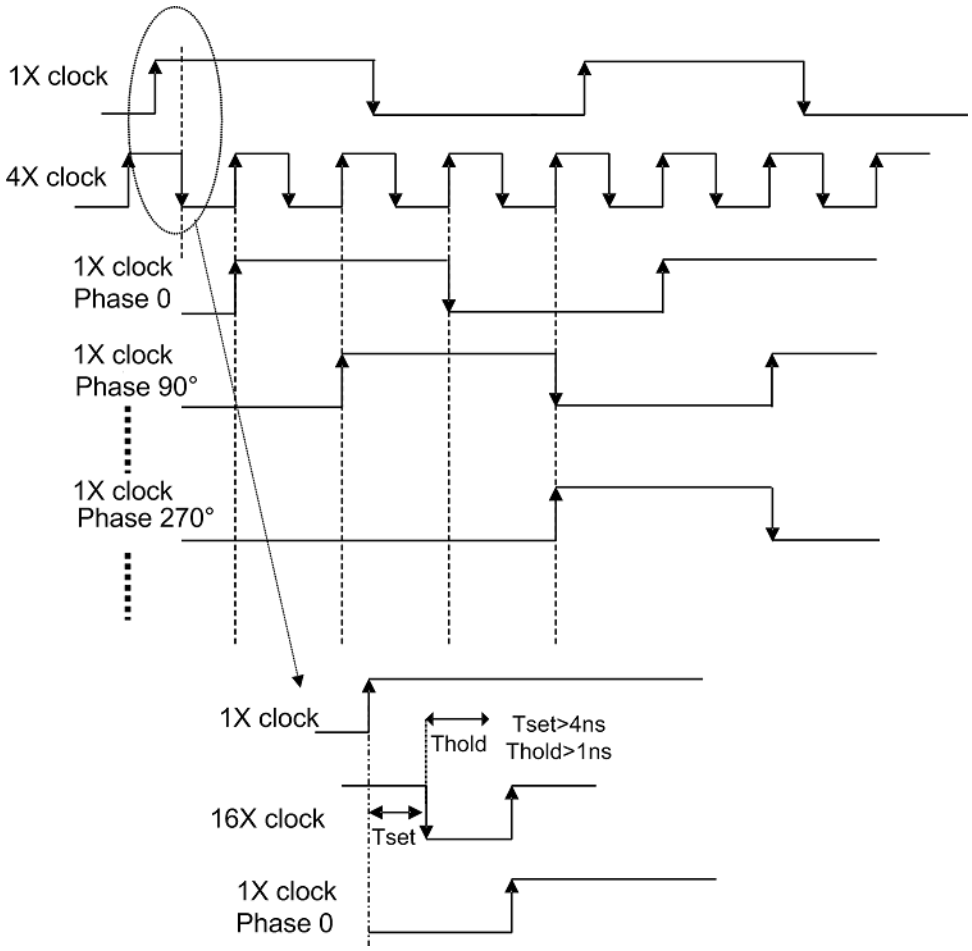


Figure 75. 8 x f_{cw} and 4 x f_{cw} Timing Diagram

1 × f_{cw} Mode

The 1x f_{cw} mode requires in-phase and quadrature clocks with low phase noise specifications. The $\frac{1}{16}T$ phase delay resolution is also achieved by weighting the in-phase and quadrature signals as described in the 8 × f_{cw} and 4 × f_{cw} modes.

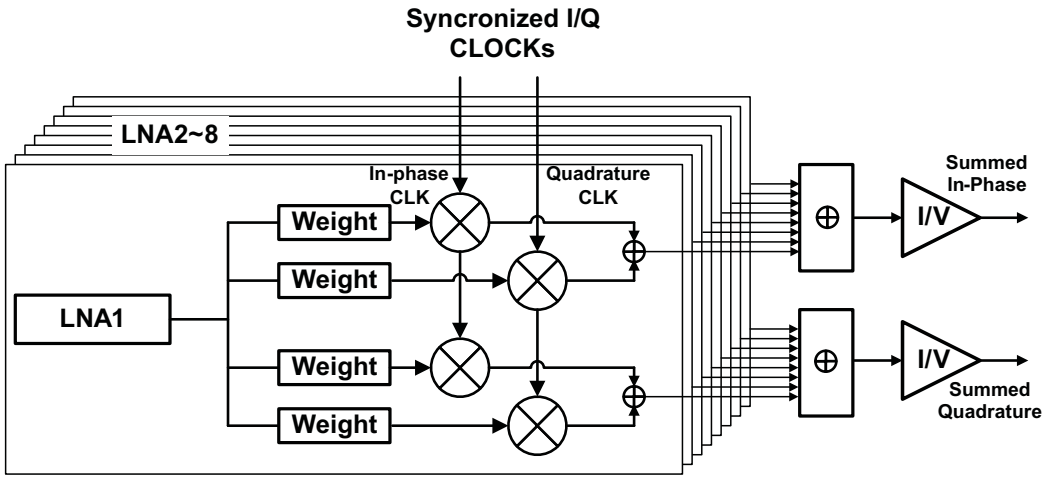


Figure 76. Block Diagram of 1 x f_{cw} mode

EQUIVALENT CIRCUITS

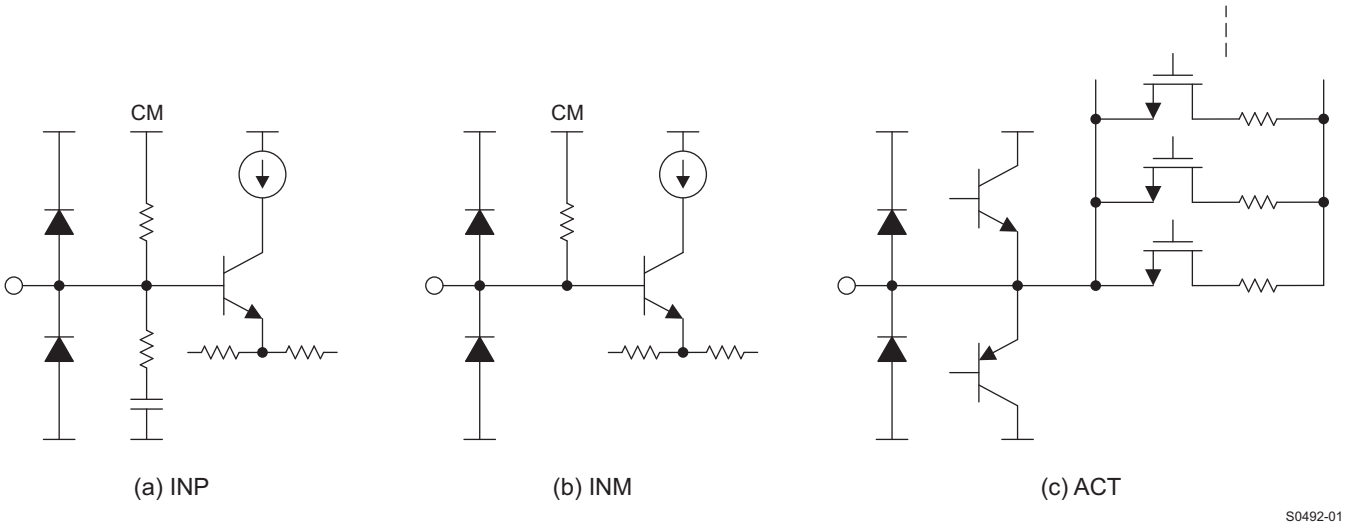


Figure 77. Equivalent Circuits of LNA inputs

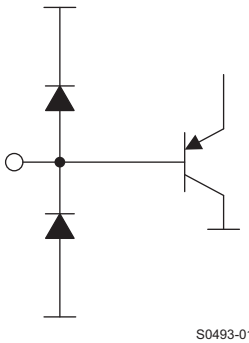


Figure 78. Equivalent Circuits of $V_{CNTLP/M}$

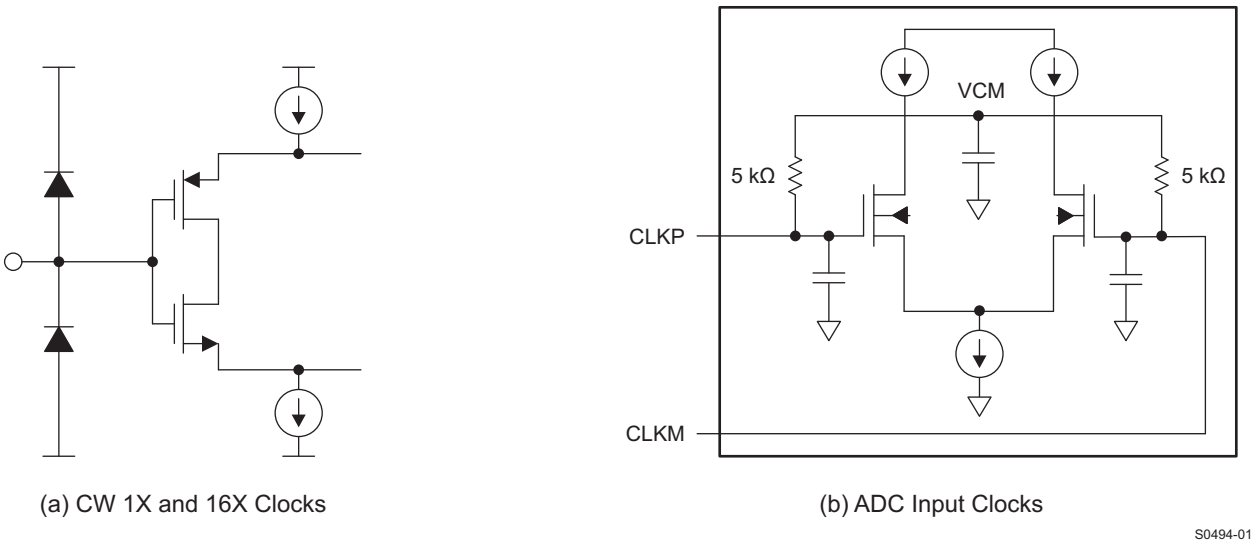


Figure 79. Equivalent Circuits of Clock Inputs

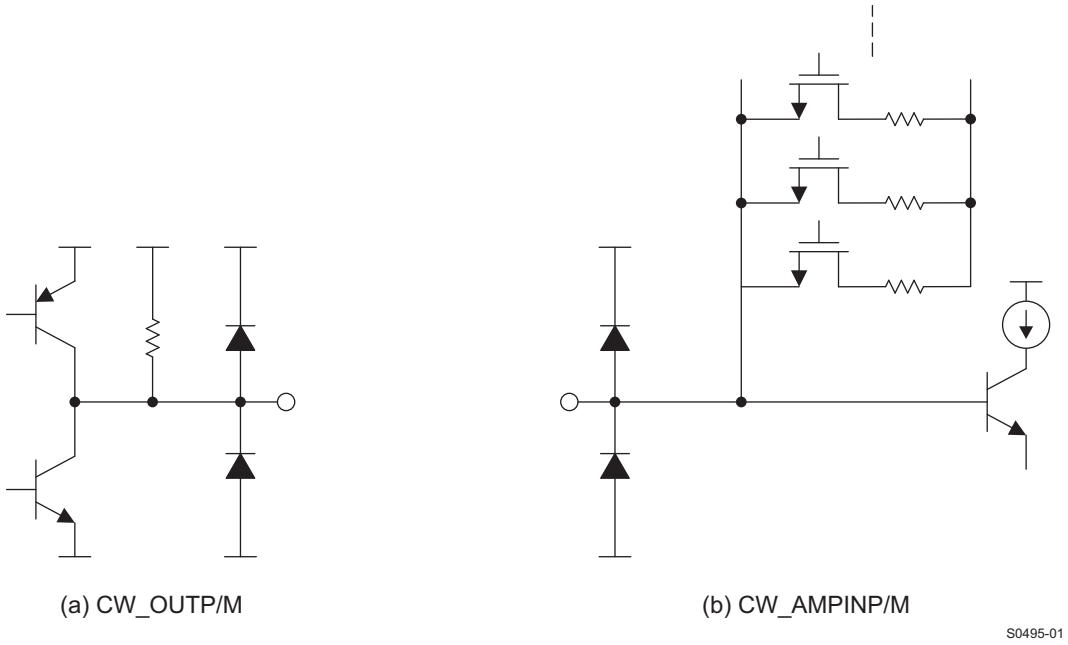


Figure 80. Equivalent Circuits of CW Summing Amplifier Inputs and Outputs

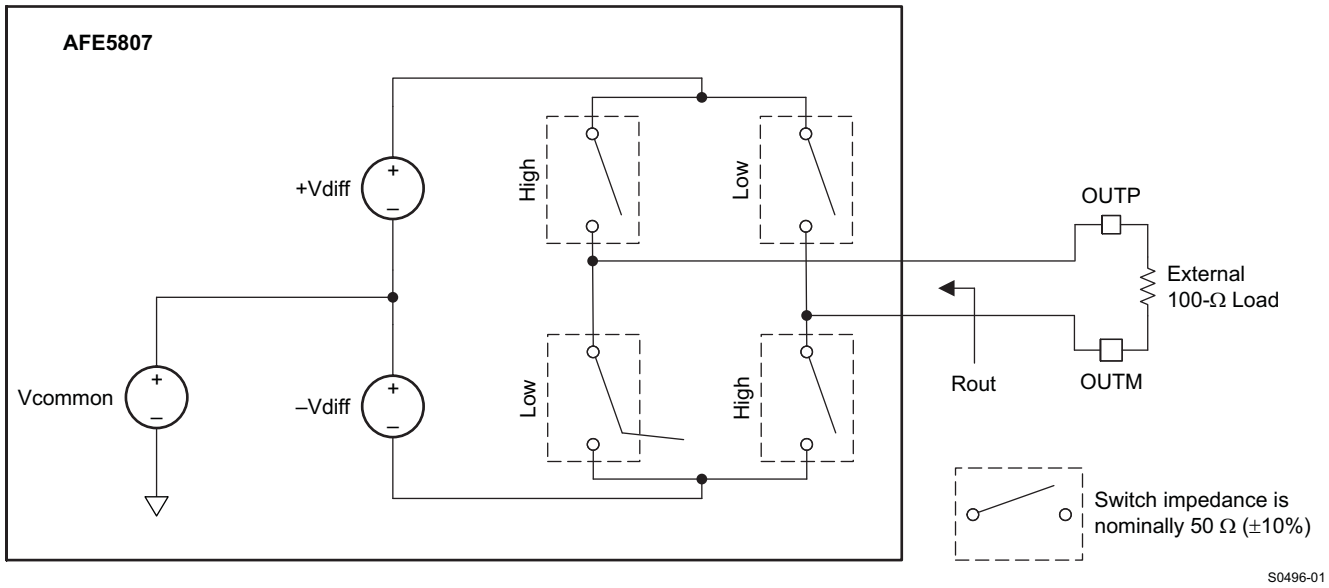


Figure 81. Equivalent Circuits of LVDS Outputs

APPLICATION INFORMATION

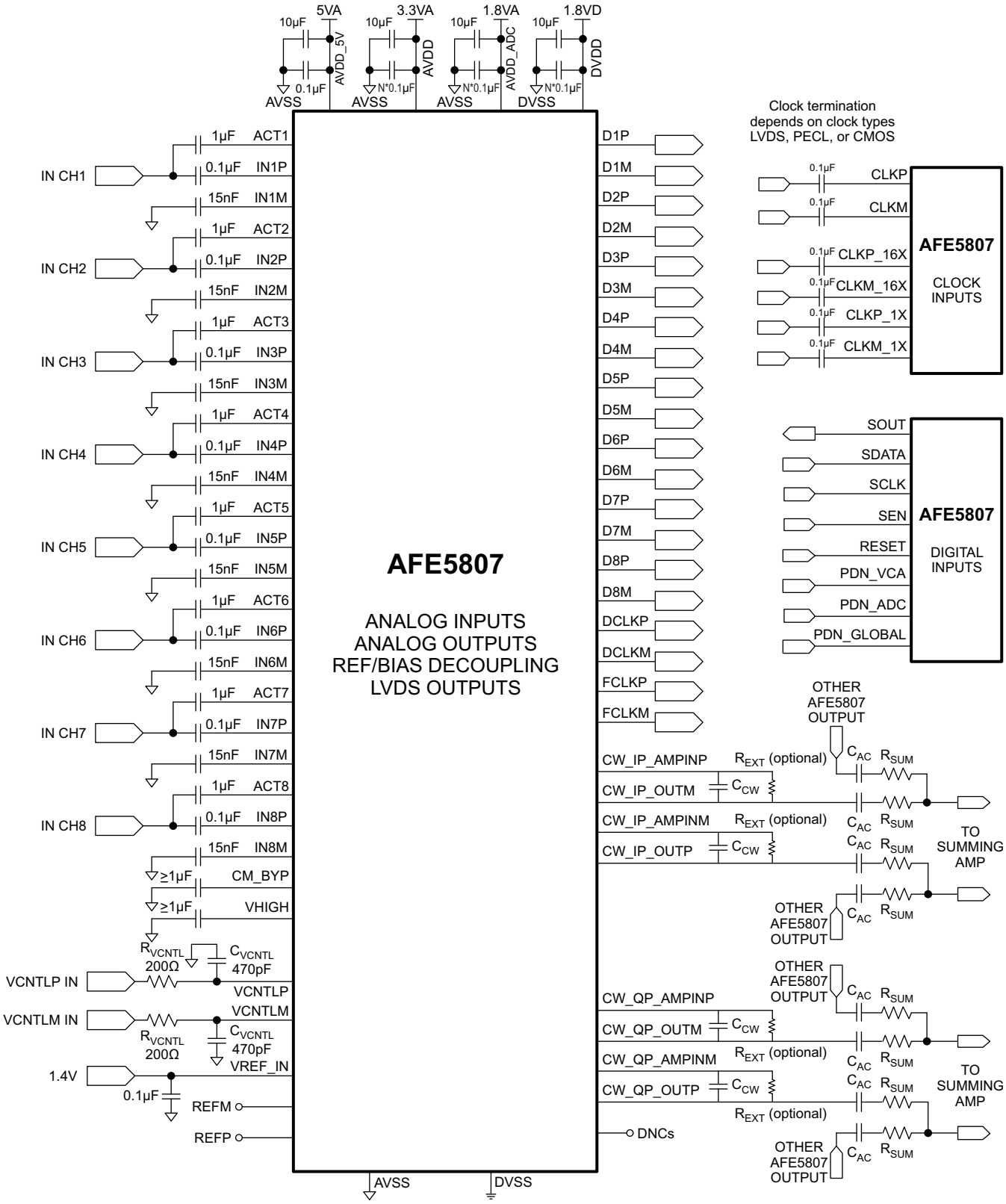


Figure 82. Application Circuit

A typical application circuit diagram is listed above. The configuration for each block is discussed below.

LNA CONFIGURATION

LNA Input Coupling and Decoupling

The LNA closed-loop architecture is internally compensated for maximum stability without the need of external compensation components. The LNA inputs are biased at 2.4V and AC coupling is required. A typical input configuration is shown in Figure 83. C_{IN} is the input AC coupling capacitor. C_{ACT} is a part of the active termination feedback path. Even if the active termination is not used, the C_{ACT} is required for the clamp functionality. Recommended values for C_{ACT} is 1 µF and C_{IN} is ≥ 0.1µF. A pair of clamping diodes is commonly placed between the T/R switch and the LNA input. Schottky diodes with suitable forward drop voltage (e.g. the BAT754/54 series, the BAS40 series, the MMBD7000 series, or similar) can be considered depending on the transducer echo amplitude.

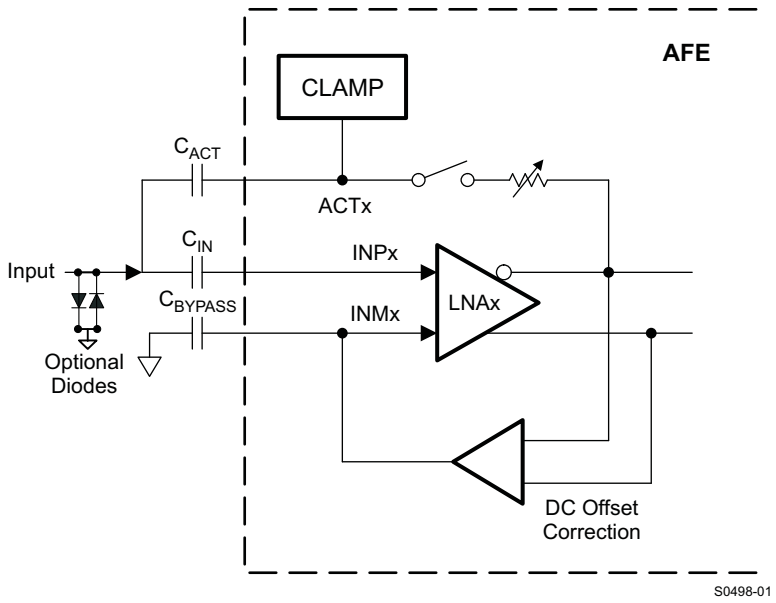


Figure 83. LNA Input Configurations

This architecture minimizes any loading of the signal source that may otherwise lead to a frequency-dependent voltage divider. The closed-loop design yields very low offsets and offset drift. C_{BYPASS} (≥0.015µF) is used to set the high-pass filter cut-off frequency and decouple the complimentary input. Its cut-off frequency is inversely proportional to the C_{BYPASS} value, The HPF cut-off frequency can be adjusted through the register 59[3:2] a Table 11 lists. Low frequency signals at T/R switch output, such as signals with slow ringing, can be filtered out. In addition, the HPF can minimize system noise from DC-DC converters, pulse repetition frequency (PRF) trigger, and frame clock. Most ultrasound systems' signal processing unit includes digital high-pass filters or band-pass filters (BPFs) in FPGAs or ASICs. Further noise suppression can be achieved in these blocks. In addition, a digital HPF is available in the AFE5807 ADC. If low frequency signal detection is desired in some applications, the LNA HPF can be disabled.

Table 11. LNA HPF Settings (C_{BYPASS} = 15 nF)

Reg59[3:2] (0x3B[3:2])	Frequency
00	100 KHz
01	50 KHz
10	200 KHz
11	150 KHz

CM_BYP and VHIGH pins, which generate internal reference voltages, need to be decoupled with ≥1uF capacitors. Bigger bypassing capacitors (>2.2uF) may be beneficial if low frequency noise exists in system.

LNA Noise Contribution

The noise spec is critical for LNA and it determines the dynamic range of entire system. The LNA of the AFE5807 achieves low power and an exceptionally low-noise voltage of 0.63nV/√Hz, and a low current noise of 2.7pA/√Hz.

Typical ultrasonic transducer's impedance Rs varies from tens of ohms to several hundreds of ohms. Voltage noise is the dominant noise in most cases; however, the LNA current noise flowing through the source impedance (Rs) generates additional voltage noise.

$$LNA\_Noise_{total} = \sqrt{V^2_{LNAnoise} + R^2_s \times I^2_{LNAnoise}} \quad (5)$$

The AFE5807 achieves low noise figure (NF) over a wide range of source resistances as shown in Figure 32, Figure 33, andFigure 34.

Active Termination

In ultrasound applications, signal reflection exists due to long cables between transducer and system. The reflection results in extra ringing added to echo signals in PW mode. Since the axial resolution depends on echo signal length, such ringing effect can degrade the axial resolution. Hence, either passive termination or active termination, is preferred if good axial resolution is desired. Figure 84 shows three termination configurations:

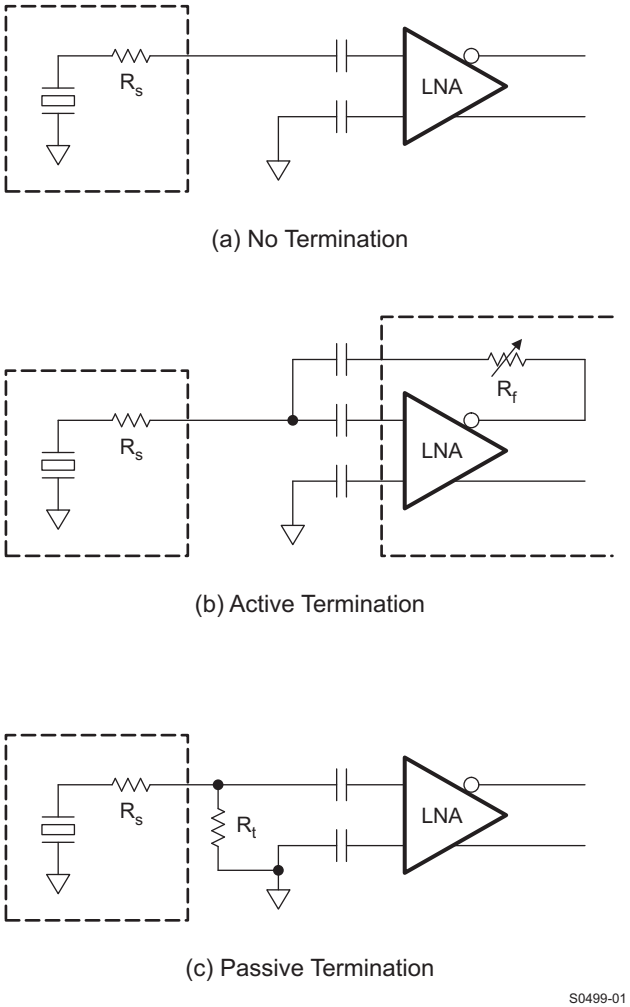


Figure 84. Termination Configurations

Under the no termination configuration, the input impedance of the AFE5807 is about 6KΩ (8K//20pF) at 1 MHz. Passive termination requires external termination resistor Rt, which contributes to additional thermal noise.

The LNA supports active termination with programmable values, as shown in Figure 85 .

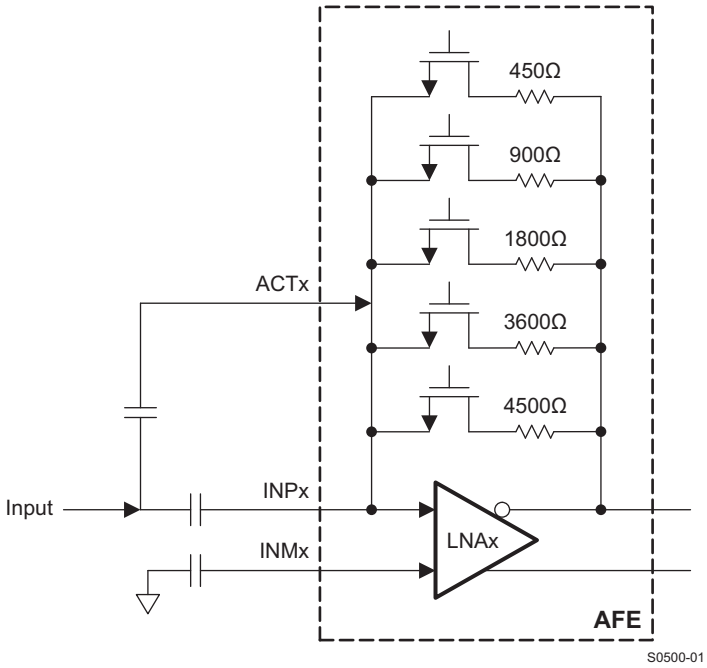


Figure 85. Active Termination Implementation

The AFE5807 has four pre-settings 50,100, 200 and 400 Ω which are configurable through the registers. Other termination values can be realized by setting the termination switches shown in the above figure. Register [52] is used to enable these switches. The input impedance of the LNA under the active termination configuration approximately follows:

$$Z_{IN} = \frac{R_f}{1 + \frac{A\nu_{LNA}}{2}} \quad (6)$$

Table 5 lists the LNA R_{IN}s under different LNA gains. System designers can achieve fine tuning for different probes.

The equivalent input impedance is given by Equation 7 where R_{IN} (8K) and C_{IN} (20pF) are the input resistance and capacitance of the LNA.

$$Z_{IN} = \frac{R_f}{1 + \frac{A\nu_{LNA}}{2}} / /C_{IN} / /R_{IN} \quad (7)$$

Therefore, the Z_{IN} is frequency dependent and it decreases as frequency increases shown in Figure 10. Since 2 MHz~10 MHz is the most commonly used frequency range in medical ultrasound, this rolling-off effect doesn't impact system performance greatly. Active termination can be applied to both CW and TGC modes. Since each ultrasound system includes multiple transducers with different impedances, the flexibility of impedance configuration is a great plus.

Figure 32, Figure 33, andFigure 34 shows the NF under different termination configurations. It indicates that no termination achieves the best noise figure; active termination adds less noise than passive termination. Thus termination topology should be carefully selected based on each use scenario in ultrasound.

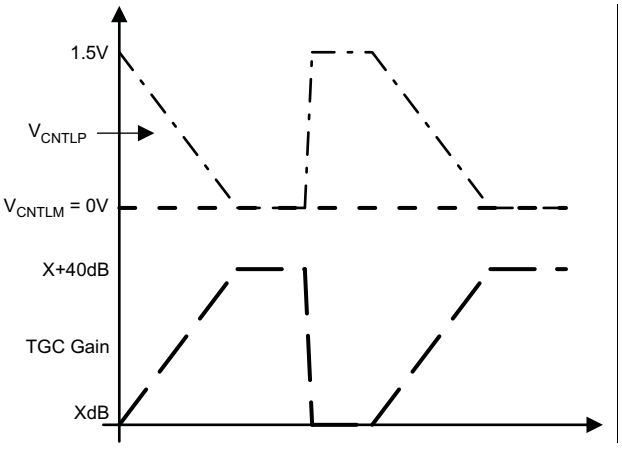
LNA Gain Switch Response

The LNA gain is programmable through SPI. The gain switching time depends on the SPI speed as well as the LNA gain response time. During the switching, glitches might occur and they can appear as artifacts in images. LNA gain switching in a single imaging line may not be preferred, although digital signal processing might be used here for glitch suppression.

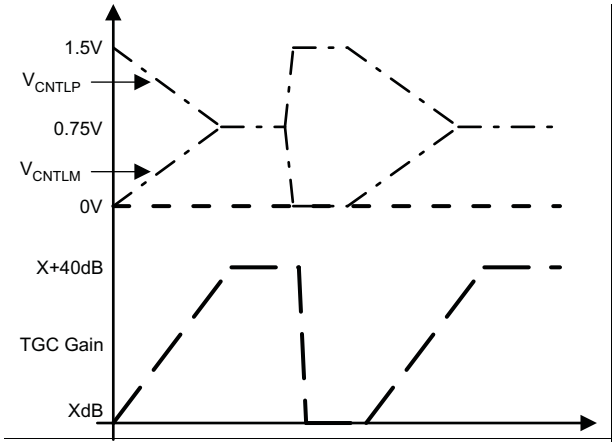
VOLTAGE-CONTROLLED-ATTENUATOR

The attenuator in the AFE5807 is controlled by a pair of differential control inputs, the $V_{CNTLM/P}$ pins. The differential control voltage spans from 0V to 1.5V. This control voltage varies the attenuation of the attenuator based on its linear-in-dB characteristic. Its maximum attenuation (minimum channel gain) appears at V_{CNTLP} - V_{CNTLM}= 1.5V, and minimum attenuation (maximum channel gain) occurs at V_{CNTLP} - V_{CNTLM} = 0. The typical gain range is 40dB and remains constant, independent of the PGA setting.

When only single-ended V_{CNTL} signal is available, this 1.5Vpp signal can be applied on the V_{CNTLP} pin with the V_{CNTLM} pin connected to ground. As the below figures show, TGC gain curve is inversely proportional to the V_{CNTLP} - V_{CNTLM}.



(a) Single-Ended Input at V_{CNTLP}



(b) Differential Inputs at V_{CNTLP} and V_{CNTLM}

W0004-01

Figure 86. V_{CNTLP} and V_{CNTLM} Configurations

As discussed in the theory of operation, the attenuator architecture uses seven attenuator segments that are equally spaced in order to approximate the linear-in-dB gain-control slope. This approximation results in a monotonic slope; the gain ripple is typically less than ±0.5dB.

The control voltage input ($V_{CNTLM/P}$ pins) represents a high-impedance input. The $V_{CNTLM/P}$ pins of multiple AFE5807 devices can be connected in parallel with no significant loading effects. When the voltage level (V_{CNTLP} - V_{CNTLM}) is above 1.5V or below 0V, the attenuator continues to operate at its maximum attenuation level or minimum attenuation level respectively. It is recommended to limit the voltage from -0.3V to 2V.

When the AFE5807 operates in CW mode, the attenuator stage remains connected to the LNA outputs. Therefore, it is recommended to power down the VCA using the PDN_VCA register bit. In this case, V_{CNTLP}-V_{CNTLM} voltage does not matter.

The AFE5807 gain-control input has a –3dB bandwidth of approximately 800KHz. This wide bandwidth, although useful in many applications (e.g. fast V_{CNTL} response), can also allow high-frequency noise to modulate the gain control input and finally affect the Doppler performance. In practice, this modulation can easily be avoided by additional external filtering (RV_{CNTL} and CV_{CNTL}) at $V_{CNTLM/P}$ pins as Figure 81 shows. However, the external filter's cutoff frequency cannot be kept too low as this results in low gain response time. Without external filtering, the gain control response time is typically less than 1 µs to settle within 10% of the final signal level of 1VPP (–6dBFS) output as indicated in Figure 51 and Figure 52.

Typical $V_{CNTLM/P}$ signals are generated by an 8bit to 12bit 10MSPS digital to analog converter (DAC) and a differential operation amplifier. TI's DACs, such as TLV5626 and DAC7821/11 (10MSPS/12bit), could be used to generate TGC control waveforms. Differential amplifiers with output common mode voltage control (e.g. THS4130 and OPA1632) can connect the DAC to the $V_{CNTLM/P}$ pins. The buffer amplifier can also be configured as an active filter to suppress low frequency noise. The $V_{CNTLM/P}$ circuit shall achieve low noise in order to prevent the $V_{CNTLM/P}$ noise being modulated to RF signals. It is recommended that $V_{CNTLM/P}$ noise is below 25 nV/rtHz at 1KHz and 5 nV/rtHz at 50 KHz. More information can be found in the literatures SLOS318F and SBAA150. The V_{CNTL} vs Gain curves can be found in Figure 2. The below table also shows the absolute gain vs. V_{CNTL}, which may help program DAC correspondingly.

In PW Doppler and color Doppler modes, V_{CNTL} noise should be minimized to achieve the best close-in phase noise and SNR. Digital V_{CNTL} feature is implemented to address this need in the AFE5807. In the digital V_{CNTL} mode, no external V_{CNTL} is needed.

Table 12. V_{CNTLP}–V_{CNTLM} vs Gain Under Different LNA and PGA Gain Settings (Low Noise Mode)

V_{CNTLP}–V_{CNTLM} (V)	Gain (dB) LNA = 12 dB PGA = 24 dB	Gain (dB) LNA = 18 dB PGA = 24 dB	Gain (dB) LNA = 24 dB PGA = 24 dB	Gain (dB) LNA = 12 dB PGA = 30 dB	Gain (dB) LNA = 18 dB PGA = 30 dB	Gain (dB) LNA = 24 dB PGA = 30 dB
0	36.45	42.45	48.45	42.25	48.25	54.25
0.1	33.91	39.91	45.91	39.71	45.71	51.71
0.2	30.78	36.78	42.78	36.58	42.58	48.58
0.3	27.39	33.39	39.39	33.19	39.19	45.19
0.4	23.74	29.74	35.74	29.54	35.54	41.54
0.5	20.69	26.69	32.69	26.49	32.49	38.49
0.6	17.11	23.11	29.11	22.91	28.91	34.91
0.7	13.54	19.54	25.54	19.34	25.34	31.34
0.8	10.27	16.27	22.27	16.07	22.07	28.07
0.9	6.48	12.48	18.48	12.28	18.28	24.28
1.0	3.16	9.16	15.16	8.96	14.96	20.96
1.1	–0.35	5.65	11.65	5.45	11.45	17.45
1.2	–2.48	3.52	9.52	3.32	9.32	15.32
1.3	–3.58	2.42	8.42	2.22	8.22	14.22
1.4	–4.01	1.99	7.99	1.79	7.79	13.79
1.5	–4	2	8	1.8	7.8	13.8

CW OPERATION

CW Summing Amplifier

In order to simplify CW system design, a summing amplifier is implemented in the AFE5807 to sum and convert 8-channel mixer current outputs to a differential voltage output. Low noise and low power are achieved in the summing amplifier while maintaining the full dynamic range required in CW operation.

This summing amplifier has 5 internal gain adjustment resistors which can provide 32 different gain settings (register 54[4:0], Figure 85 and Table 7). System designers can easily adjust the CW path gain depending on signal strength and transducer sensitivity. For any other gain values, an external resistor option is supported. The gain of the summation amplifier is determined by the ratio between the 500Ω resistors after LNA and the internal or external resistor network $R_{EXT/INT}$. Thus the matching between these resistors plays a more important role than absolute resistor values. Better than 1% matching is achieved on chip. Due to process variation, the absolute resistor tolerance could be higher. If external resistors are used, the gain error between I/Q channels or among multiple AFEs may increase. It is recommended to use internal resistors to set the gain in order to achieve better gain matching (across channels and multiple AFEs). With the external capacitor C_{EXT} , this summing amplifier has 1st order LPF response to remove high frequency components from the mixers, such as 2f0±fd. Its cut-off frequency is determined by:

$$f_{HP} = \frac{1}{2\pi R_{INT/EXT} C_{EXT}} \quad (8)$$

Note that when different gain is configured through register 54[4:0], the LPF response varies as well.

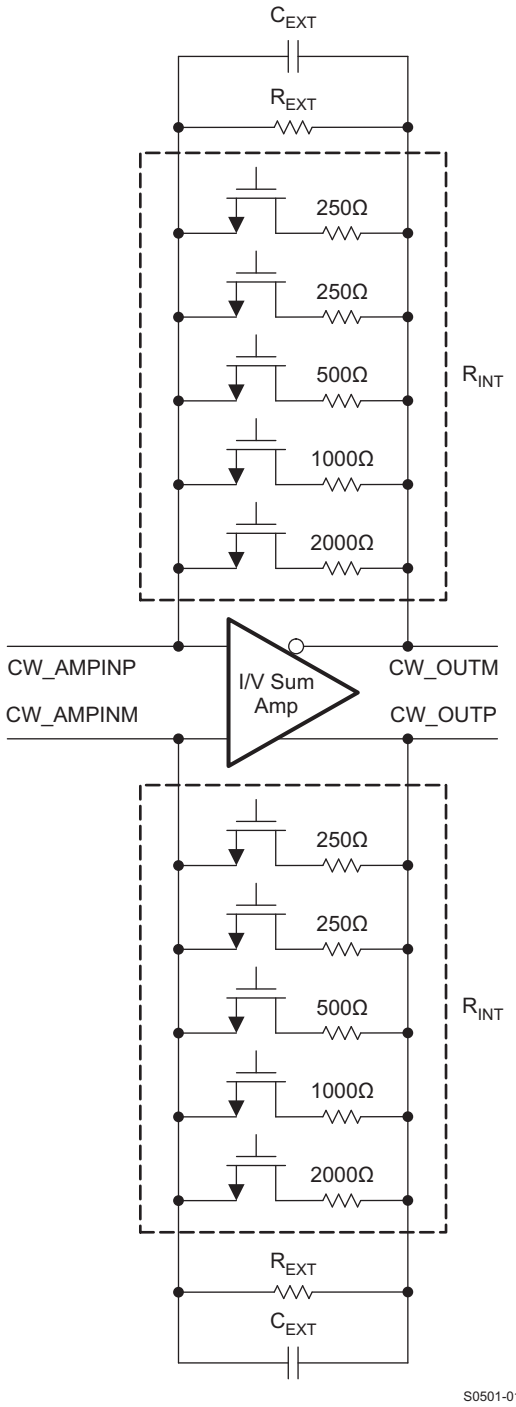


Figure 87. CW Summing Amplifier Block Diagram

Multiple AFE5807s are usually utilized in parallel to expand CW beamformer channel count. These AFE5807s' CW outputs can be summed and filtered externally further to achieve desired gain and filter response. AC coupling capacitors CAC are required to block DC component of the CW carrier signal. CAC can vary from 1uF to 10s µF depending on the desired low frequency Doppler signal from slow blood flow. Multiple AFE5807s' I/Q outputs can be summed together with a low noise external differential amplifiers before 16/18-bit differential audio ADCs. TI's ultralow noise differential precision amplifier OPA1632 and THS4130 are suitable devices.

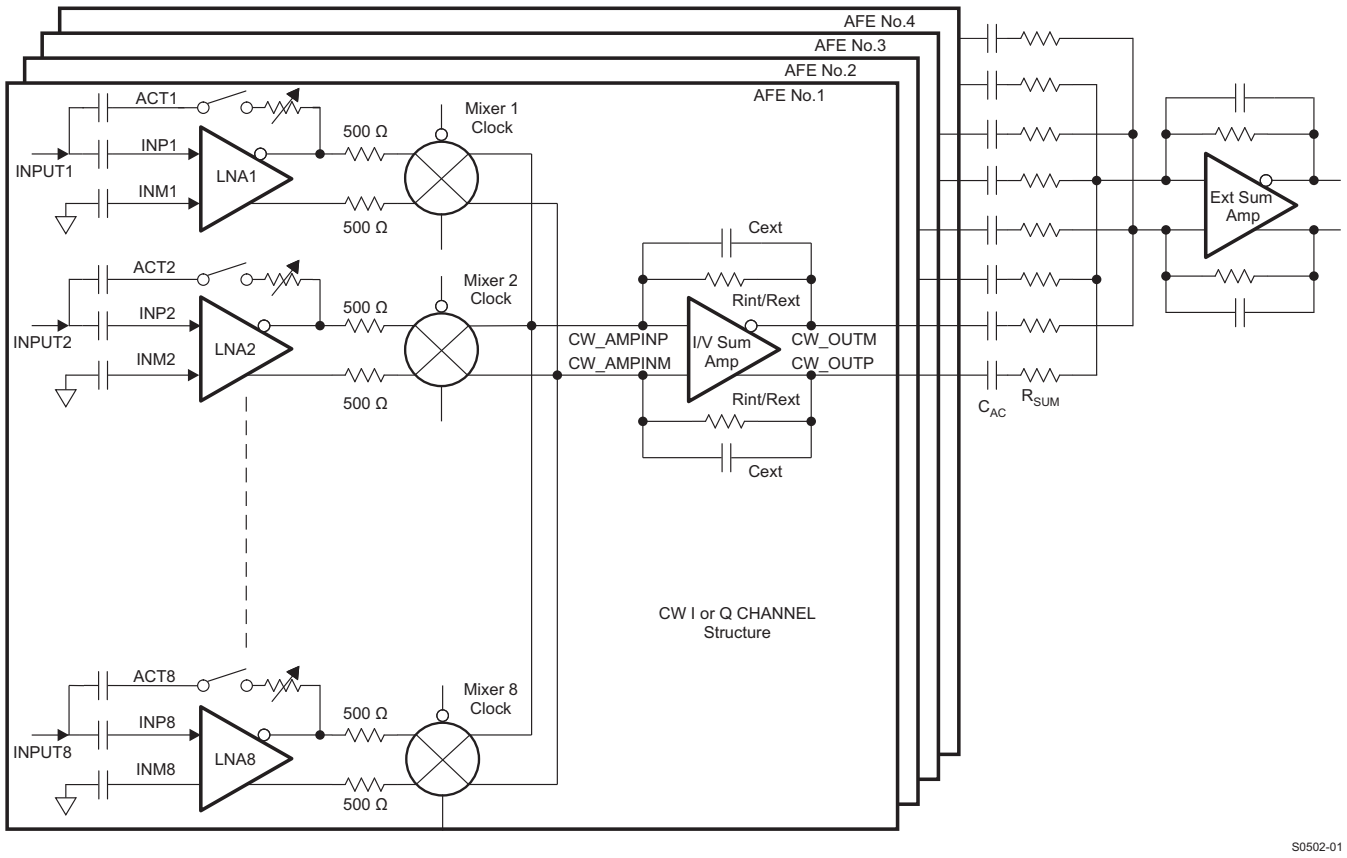


Figure 88. CW circuit with Multiple AFE5807s

The CW I/Q channels are well matched internally to suppress image frequency components in Doppler spectrum. Low tolerance components and precise operational amplifiers should be used for achieving good matching in the external circuits as well.

NOTE

The local oscillator inputs of the passive mixer are cos(ωt) for I-CH and sin(ωt) for Q-CH respectively. Depending on users' CW Doppler complex FFT processing, swapping I/Q channels in FPGA or DSP may be needed in order to get correct blood flow directions.

CW Clock Selection

The AFE5807 can accept differential LVDS, LVPECL, and other differential clock inputs as well as single-ended CMOS clock. An internally generated VCM of 2.5V is applied to CW clock inputs, i.e. CLKP_16X/ CLKM_16X and CLKP_1X/ CLKM_1X. Since this 2.5V VCM is different from the one used in standard LVDS or LVPECL clocks, AC coupling is required between clock drivers and the AFE5807 CW clock inputs. When CMOS clock is used, CLKM_1X and CLKM_16X should be tied to ground. Common clock configurations are illustrated in Figure 89. Appropriate termination is recommended to achieve good signal integrity.

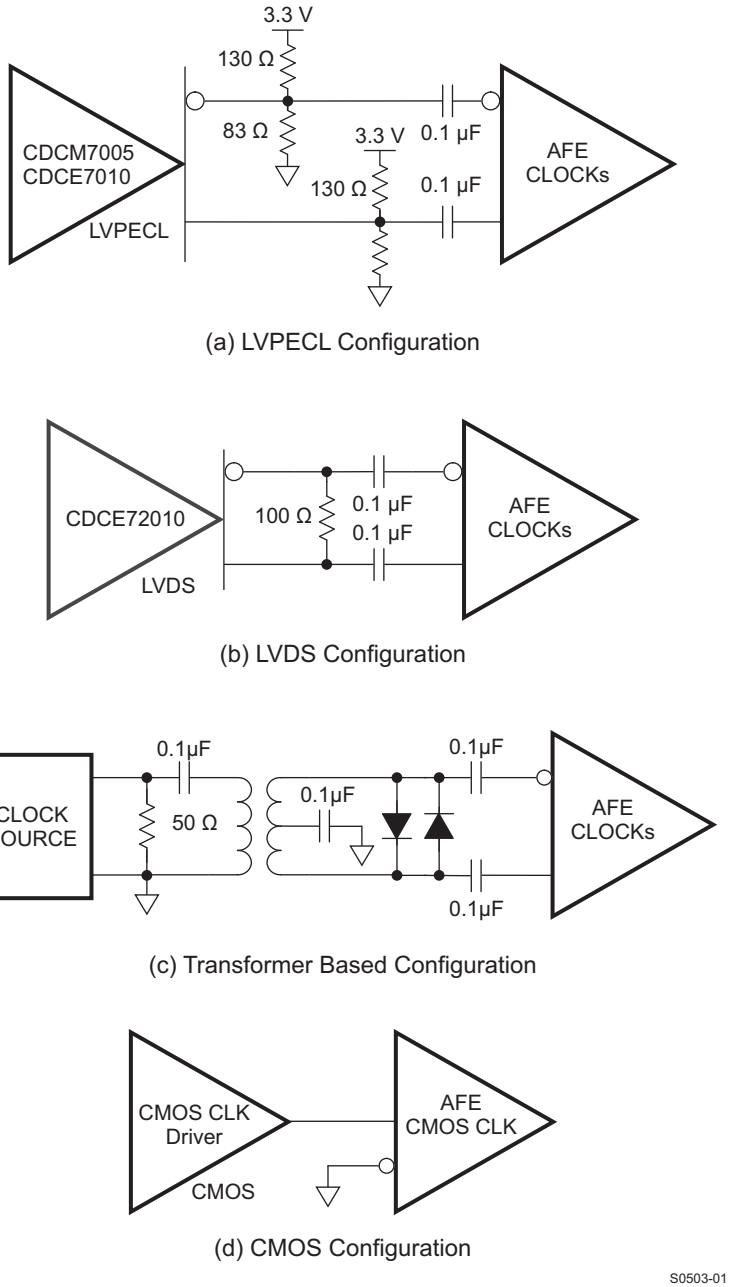


Figure 89. Clock Configurations

The combination of the clock noise and the CW path noise can degrade the CW performance. The internal clocking circuit is designed for achieving excellent phase noise required by CW operation. The phase noise of the AFE5807 CW path is better than 155dBc/Hz at 1KHz offset. Consequently the phase noise of the mixer clock inputs needs to be better than 155dBc/Hz.

In the 16/8/4×fcw operations modes, low phase noise clock is required for 16/8/4×f_{cw} clocks (i.e. CLKP_16X/ CLKM_16X pins) in order to maintain good CW phase noise performance. The 1×f_{cw} clock (i.e. CLKP_1X/ CLKM_1X pins) is only used to synchronize the multiple AFE5807 chips and is not used for demodulation. Thus 1×fcw clock's phase noise is not a concern. However, in the 1×fcw operation mode, low phase noise clocks are required for both CLKP_16X/ CLKM_16X and CLKP_1X/ CLKM_1X pins since both of them are used for mixer demodulation. In general, higher slew rate clock has lower phase noise; thus clocks with high amplitude and fast slew rate are preferred in CW operation. In the CMOS clock mode, 5V CMOS clock can achieve the highest slew rate.

Clock phase noise can be improved by a divider as long as the divider's phase noise is lower than the target phase noise. The phase noise of a divided clock can be improved approximately by a factor of 20logN dB where N is the dividing factor of 16, 8, or 4. If the target phase noise of mixer LO clock 1×fcw is 160dBc/Hz at 1KHz off carrier, the 16×fcw clock phase noise should be better than 160-20log16=136dBc/Hz. TI's jitter cleaners LMK048X/CDCM7005/CDCE72010 exceed this requirement and can be selected for the AFE5807. In the 4X/1X modes, higher quality input clocks are expected to achieve the same performance since N is smaller. Thus the 16X mode is a preferred mode since it reduces the phase noise requirement for system clock design. In addition, the phase delay accuracy is specified by the internal clock divider and distribution circuit.

NOTE

In the 16X operation mode, the CW operation range is limited to 8 MHz due to the 16X CLK. The maximum clock frequency for the 16X CLK is 128 MHz. In the 8X, 4X, and 1X modes, higher CW signal frequencies up to 15 MHz can be supported with small degradation in performance., e.g. the phase noise is degraded by 9 dB at 15MHz, compared to 2MHz.

As the channel number in a system increases, clock distribution becomes more complex. It is not preferred to use one clock driver output to drive multiple AFEs since the clock buffer's load capacitance increases by a factor of N. As a result, the falling and rising time of a clock signal is degraded. A typical clock arrangement for multiple AFE5807s is illustrated in Figure 90. Each clock buffer output drives one AFE5807 in order to achieve the best signal integrity and fastest slew rate, i.e. better phase noise performance. When clock phase noise is not a concern, e.g. the 1×fcw clock in the 16/8/4×fcw operation modes, one clock driver output may excite more than one AFE5807s. Nevertheless, special considerations should be applied in such a clock distribution network design. In typical ultrasound systems, it is preferred that all clocks are generated from a same clock source, such as 16×fcw , 1×fcw clocks, audio ADC clocks, RF ADC clock, pulse repetition frequency signal, frame clock and etc. By doing this, interference due to clock asynchronization can be minimized

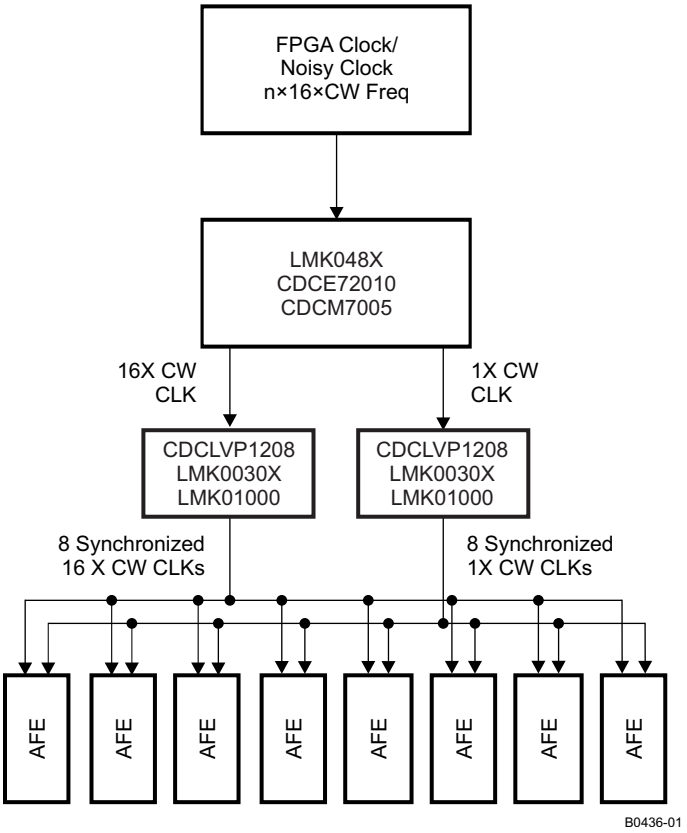


Figure 90. CW Clock Distribution

CW Supporting Circuits

As a general practice in CW circuit design, in-phase and quadrature channels should be strictly symmetrical by using well matched layout and high accuracy components.

In systems, additional high-pass wall filters (20Hz to 500Hz) and low-pass audio filters (10KHz to 100KHz) with multiple poles are usually needed. Since CW Doppler signal ranges from 20Hz to 20KHz, noise under this range is critical. Consequently low noise audio operational amplifiers are suitable to build these active filters for CW post-processing, e.g. OPA1632 or OPA2211. More filter design techniques can be found from www.ti.com, e.g. TI's active filter design tool http://focus.ti.com/docs/toolsw/folders/print/filter-designer.html

The filtered audio CW I/Q signals are sampled by audio ADCs and processed by DSP or PC. Although CW signal frequency is from 20 Hz to 20 KHz, higher sampling rate ADCs are still preferred for further decimation and SNR enhancement. Due to the large dynamic range of CW signals, high resolution ADCs (>=16bit) are required, such as ADS8413 (2MSPS/16it/92dBFS SNR) and ADS8472 (1MSPS/16bit/95dBFS SNR). ADCs for in-phase and quadature-phase channels must be strictly matched, not only amplitude matching but also phase matching, in order to achieve the best I/Q matching,. In addition, the in-phase and quadrature ADC channels must be sampled simultaneously.

ADC OPERATION

ADC Clock Configurations

To ensure that the aperture delay and jitter are the same for all channels, the AFE5807 uses a clock tree network to generate individual sampling clocks for each channel. The clock, for all the channels, are matched from the source point to the sampling circuit of each of the eight internal ADCs. The variation on this delay is described in the aperture delay parameter of the output interface timing. Its variation is given by the aperture jitter number of the same table.

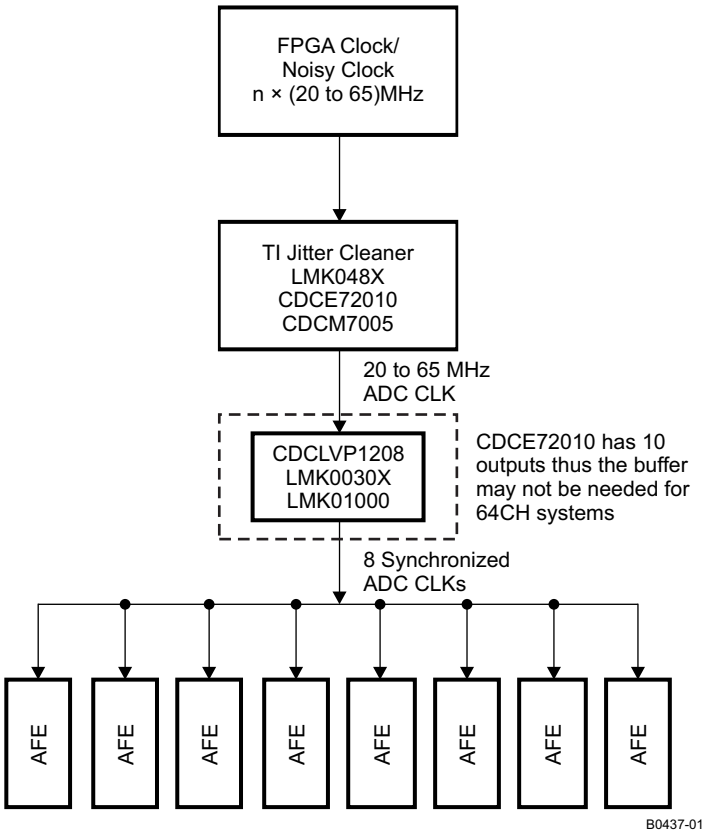


Figure 91. ADC Clock Distribution Network

The AFE5807 ADC clock input can be driven by differential clocks (sine wave, LVPECL or LVDS) or singled clocks (LVCMOS) similar to CW clocks as shown in Figure 89. In the single-end case, it is recommended that the use of low jitter square signals (LVCMOS levels, 1.8V amplitude). See TI document SLYT075 for further details on the theory.

The jitter cleaner LMK048X, CDCM7005 or CDCE72010 is suitable to generate the AFE5807's ADC clock and ensure the performance for the 12bit ADC with 70dBFS SNR. A clock distribution network is shown in Figure 91.

ADC Reference Circuit

The ADC's voltage reference can be generated internally or provided externally. When the internal reference mode is selected, the REFP/M becomes output pins and should be floated. When 3[15] =1 and 1[13]=1, the device is configured to operate in the external reference mode in which the VREF_IN pin should be driven with a 1.4V reference voltage and REFP/M must be left open. Since the input impedance of the VREF_IN is high, no special drive capability is required for the 1.4V voltage reference

The digital beam-forming algorithm in an ultrasound system relies on gain matching across all receiver channels. A typical system would have about 12 octal AFEs on the board. In such a case, it is critical to ensure that the gain is matched, essentially requiring the reference voltages seen by all the AFEs to be the same. Matching references within the eight channels of a chip is done by using a single internal reference voltage buffer. Trimming the reference voltages on each chip during production ensures that the reference voltages are well-matched across different chips. When the external reference mode is used, a solid reference plane on a printed circuit board can ensure minimal voltage variation across devices. More information on voltage reference design can be found in the document SLYT339. The dominant gain variation in the AFE5807 comes from the VCA gain variation. The gain variation contributed by the ADC reference circuit is much smaller than the VCA gain variation. Hence, in most systems, using the ADC internal reference mode is sufficient to maintain good gain matching among multiple AFE5807s. In addition, the internal reference circuit without any external components achieves satisfactory thermal noise and phase noise performance.

POWER MANAGEMENT

Power/Performance Optimization

The AFE5807 has options to adjust power consumption and meet different noise performances. This feature would be useful for portable systems operated by batteries when low power is more desired. Please refer to characteristics information listed in the table of electrical characteristics as well as the typical characteristic plots.Under the default register setting, the AFE5807 is configured as low power operation for both TGC and CW modes.

Power Management Priority

Power management plays a critical role to extend battery life and ensure long operation time. The AFE5807 has fast and flexible power down/up control which can maximize battery life. The AFE5807 can be powered down/up through external pins or internal registers. The following table indicates the affected circuit blocks and priorities when the power management is invoked. In the device, all the power down controls are logically ORed to generate final power down for different blocks. Thus, the higher priority controls can cover the lower priority ones

Table 13. Power Management Priority

	Name	Blocks	Priority
Pin	PDN_GLOBAL	All	High
Pin	PDN_VCA	LNA + VCAT+ PGA	Medium
Register	VCA_PARTIAL_PDN	LNA + VCAT+ PGA	Low
Register	VCA_COMPLETE_PDN	LNA + VCAT+ PGA	Medium
Pin	PDN_ADC	ADC	Medium
Register	ADC_PARTIAL_PDN	ADC	Low
Register	ADC_COMPLETE_PDN	ADC	Medium
Register	PDN_VCAT_PGA	VCAT + PGA	Lowest
Register	PDN_LNA	LNA	Lowest

Partial Power-Up/Down Mode

The partial power up/down mode is also called as fast power up/down mode. In this mode, most amplifiers in the signal path are powered down, while the internal reference circuits remain active as well as the LVDS clock circuit, i.e. the LVDS circuit still generates its frame and bit clocks.

The partial power down function allows the AFE5807 to be wake up from a low-power state quickly. This configuration ensures that the external capacitors are discharged slowly; thus a minimum wake-up time is needed as long as the charges on those capacitors are restored. The VCA wake-up response is typically about 2 µs or 1% of the power down duration whichever is larger. The longest wake-up time depends on the capacitors connected at INP and INM, as the wake-up time is the time required to recharge the caps to the desired operating voltages. For 0.1µF at INP and 15nF at INM can give a wake-up time of 2.5ms. For larger capacitors this time will be longer. The ADC wake-up time is about 1 µs. Thus, the AFE5807 wake-up time is more dependent on the VCA wake-up time. This also assumes that the ADC clock has been running for at least 50 µs before normal operating mode resumes. The power-down time is instantaneous, less than 1µs.

This fast wake-up response is desired for portable ultrasound applications in which the power saving is critical. The pulse repetition frequency of a ultrasound system could vary from 50KHz to 500Hz, while the imaging depth (i.e. the active period for a receive path) varies from 10 µs to hundreds of us. The power saving can be significant when a system's PRF is low. In some cases, only the VCA would be powered down while the ADC keeps running normally to ensure minimal impact to FPGAs.

In the partial power-down mode, the AFE5807 typically dissipates only 26mW/ch, representing an 80% power reduction compared to the normal operating mode. This mode can be set using either pins (PDN_VCA and PDN_ADC) or register bits (VCA_PARTIAL_PDN and ADC_PARTIAL_PDN). The AFE5807 register settings are maintained when the AFE5807 is in either partial power down mode or complete power down mode.

Complete Power-Down Mode

To achieve the lowest power dissipation of 0.7 mW/CH, the AFE5807 can be placed into a complete power-down mode. This mode is controlled through the registers ADC_COMPLETE_PDN, VCA_COMPLETE_PDN or PDN_GLOBAL pin. In the complete power-down mode, all circuits including reference circuits within the AFE5807 are powered down; and the capacitors connected to the AFE5807 are discharged. The wake-up time depends on the time needed to recharge these capacitors. The wake-up time depends on the time that the AFE5807 spends in shutdown mode. 0.1µF at INP and 15nF at INM can give a wake-up time close to 2.5ms

Power Saving in CW Mode

Usually only half the number of channels in a system are active in the CW mode. Thus the individual channel control through ADC_PDN_CH <7:0> and VCA_PDN_CH <7:0> can power down unused channels and save power consumption greatly. Under the default register setting in the CW mode, the voltage controlled attenuator, PGA, and ADC are still active. During the debug phase, both the PW and CW paths can be running simultaneously. In real operation, these blocks need to be powered down manually.

TEST MODES

The AFE5807 includes multiple test modes to accelerate system development. The ADC test modes have been discussed in the register description section.

The VCA has a test mode in which the CH7 and CH8 PGA outputs can be brought to the CW pins. By monitoring these PGA outputs, the functionality of VCA operation can be verified. The PGA outputs are connected to the virtual ground pins of the summing amplifier (CW_IP_AMPINM/P, CW_QP_AMPINM/P) through 5KΩ resistors. The PGA outputs can be monitored at the summing amplifier outputs when the LPF capacitors C_{EXT} are removed. Note that the signals at the summing amplifier outputs are attenuated due to the 5KΩ resistors. The attenuation coefficient is $R_{INT/EXT}$/5KΩ

If users would like to check the PGA outputs without removing CEXT, an alternative way is to measure the PGA outputs directly at the CW_IP_AMPINM/P and CW_QP_AMPINM/P when the CW summing amplifier is powered down

Some registers are related to this test mode. PGA Test Mode Enable: Reg59[9]; Buffer Amplifier Power Down Reg59[8]; and Buffer Amplifier Gain Control Reg54[4:0]. Based on the buffer amplifier configuration, the registers can be set in different ways:

Configuration 1:

In this configuration, the test outputs can be monitored at CW_AMPINP/M

- Reg59[9]=1 ;Test mode enabled
- Reg59[8]=0 ;Buffer amplifier powered down

Configuration 2:

In this configuration, the test outputs can be monitored at CW_OUTP/M

- Reg59[9]=1 ;Test mode enabled
- Reg59[8]=1 ;Buffer amplifier powered on
- Reg54[4:0]=10H; Internal feedback 2K resistor enabled. Different values can be used as well

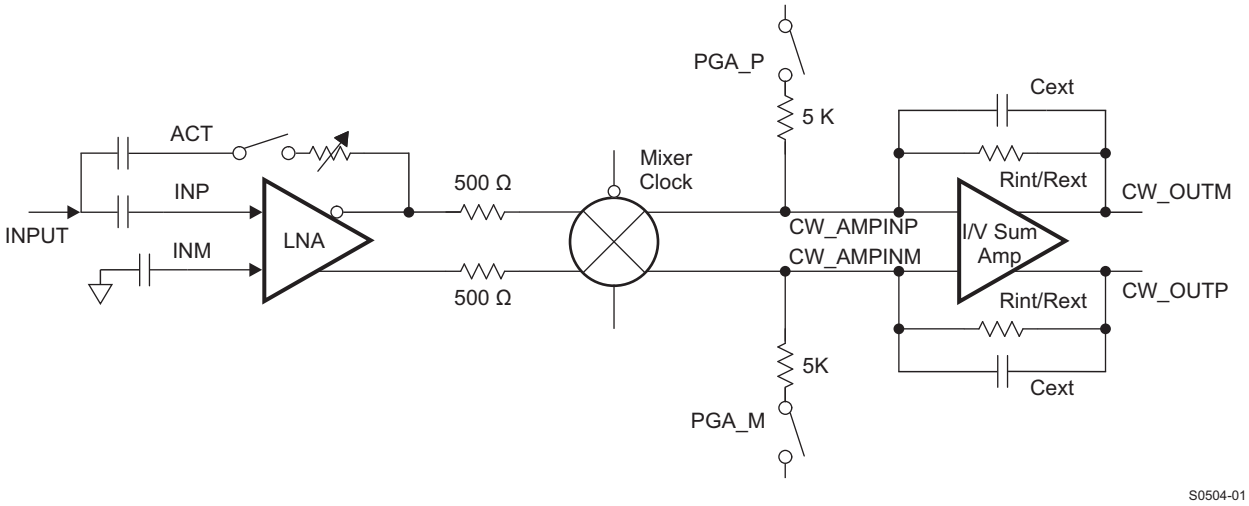


Figure 92. AFE5807 PGA Test Mode

POWER SUPPLY, GROUNDING AND BYPASSING

In a mixed-signal system design, power supply and grounding design plays a significant role. The AFE5807 distinguishes between two different grounds: AVSS(Analog Ground) and DVSS(digital ground). In most cases, it should be adequate to lay out the printed circuit board (PCB) to use a single ground plane for the AFE5807. Care should be taken that this ground plane is properly partitioned between various sections within the system to minimize interactions between analog and digital circuitry. Alternatively, the digital (DVDD) supply set consisting of the DVDD and DVSS pins can be placed on separate power and ground planes. For this configuration, the AVSS and DVSS grounds should be tied together at the power connector in a star layout. In addition, optical isolator or digital isolators, such as ISO7240, can separate the analog portion from the digital portion completely. Consequently they prevent digital noise to contaminate the analog portion. Table 13 lists the related circuit blocks for each power supply. The AFE5807 register settings are maintained when the AFE5807 is in either partial power down mode or complete power down mode.

Table 14. Supply vs Circuit Blocks

Power Supply	Ground	Circuit Blocks
AVDD (3.3VA)	AVSS	LNA, attenuator, PGA with current clamp circuit and BPF, reference circuits, CW summing amplifier, CW mixer, VCA SPI
AVDD_5V (5VA)	AVSS	LNA, CW clock circuits, reference circuits
AVDD_ADC (1.8VA)	AVSS	ADC analog and reference circuits
DVDD (1.8VD)	DVSS	LVDS and ADC SPI

All bypassing and power supplies for the AFE5807 should be referenced to their corresponding ground planes. All supply pins should be bypassed with 0.1µF ceramic chip capacitors (size 0603 or smaller). In order to minimize the lead and trace inductance, the capacitors should be located as close to the supply pins as possible. Where double-sided component mounting is allowed, these capacitors are best placed directly under the package. In addition, larger bipolar decoupling capacitors 2.2µF to 10µF, effective at lower frequencies) may also be used on the main supply pins. These components can be placed on the PCB in proximity (< 0.5 in or 12.7 mm) to the AFE5807 itself.

The AFE5807 has a number of reference supplies needed to be bypassed, such CM_BYP, VHIGH, and VREF_IN. These pins should be bypassed with at least 1µF; higher value capacitors can be used for better low-frequency noise suppression. For best results, choose low-inductance ceramic chip capacitors (size 0402, > 1µF) and place them as close as possible to the device pins.

High-speed mixed signal devices are sensitive to various types of noise coupling. One primary source of noise is the switching noise from the serializer and the output buffer/drivers. For the AFE5807, care has been taken to ensure that the interaction between the analog and digital supplies within the device is kept to a minimal amount. The extent of noise coupled and transmitted from the digital and analog sections depends on the effective inductances of each of the supply and ground connections. Smaller effective inductance of the supply and ground pins leads to improved noise suppression. For this reason, multiple pins are used to connect each supply and ground sets. It is important to maintain low inductance properties throughout the design of the PCB layout by use of proper planes and layer thickness.

BOARD LAYOUT

Proper grounding and bypassing, short lead length, and the use of ground and power-supply planes are particularly important for high-frequency designs. Achieving optimum performance with a high-performance device such as the AFE5807 requires careful attention to the PCB layout to minimize the effects of board parasitics and optimize component placement. A multilayer PCB usually ensures best results and allows convenient component placement. In order to maintain proper LVDS timing, all LVDS traces should follow a controlled impedance design. In addition, all LVDS trace lengths should be equal and symmetrical; it is recommended to keep trace length variations less than 150 mil (0.150 in or 3.81 mm).

To avoid noise coupling through supply pins, it is recommended to keep sensitive input pins, such as INM, INP, ACT pins away from the AVDD 3.3 V, AVDD_5V, AVDD_ADC, DVDD, DVDD_LDO1/2, and other noise supply planes. For example, either the traces or vias connected to these pins should not be routed across the these power supply planes. In addition, appropriate delay matching should be considered for the CW clock path, especially in systems with high channel count. For example, if clock delay is half of the 16x clock period, a phase error of 22.5°C could exist. Thus the timing delay difference among channels contributes to the beamformer accuracy.

Additional details on BGA PCB layout techniques can be found in the Texas Instruments Application Report MicroStar BGA Packaging Reference Guide (SSYZ015B), which can be downloaded from www.ti.com .

REVISION HISTORY

Changes from Original (SEPTEMBER 2010) to Revision A **Page**

- Revision A expanded the data sheet technical information 1
- Changed "10Ω resistors" to "10-15Ω parasitic resistors" in Figure 70 45
- Updated Figure 73that output clocks align at the rising edge of the 4X/8X CLK. 49

Changes from Revision A (December 2011) to Revision B **Page**

- Added pin compatible devices AFE5803 and AFE5808A to the Description text 1
- Changed the PIN FUNCTION table 4
- Changed the TYP value of en (RTO) - 8 channel mixer From: 0.4 nV/rtHz To 4.0 nV/rtHz 8
- Added Test Condition - TGC Default power mode (Low power), 40MSPS/12bit 9
- Added 40 MSPS Test Condition 10
- Changed the t_{delay} Test Condiitons From: Input clock rising edge (zero cross) to frame clock rising edge (zero cross) minus half the input clock period (T). To: Input clock rising edge (zero cross) to frame clock rising edge (zero cross) minus 3/7 of the input clock period (T). 25
- Changed Table 3 33
- Added Note: 54[9] is only effective in CW mode. 36
- Added Note: 59[8] is only effective in TGC test mode. 37
- Changed Figure 70 45
- Changed Figure 83 54

Changes from Revision B (April 2012) to Revision C **Page**

- Added " AFE5809 is another member with enhanced digital demodulation features in this family " to the Description text 1
- Added " In addtion, clock amplitude can influence phase noise as well and >0.7Vpp is recommended when differential clocks are used." 8
- Added Table Note "According to design and characterization, LVDS and LVPECL CLK input amplitude can be as low as 0.2Vpp". 11
- Changed from "Data Valid to Input Clock Zero-Crossing "... to DCLK Zero-crossing". 25
- Changed from "Input Clock Zero-Crossing to Data Invalid" to "DCLK Zero-crossing to Data Invalide". 25
- Added a note "The above timing data can be applied to 14-bit or 16-bit LVDS rates ..." 25
- Changed "SPI pull down resistors from 100kΩ to 20kΩ." 27
- Changed Address 3[4:1] to 33[4:1] in 32
- Combined Register 51[7:5], removed the -4dBFS clamping option, and added notes "The maximum PGA output level can exceed 2Vpp with the clamp circuit enabled. In the low power and medium power modes, PGA_CLAMP is disabled for saving power if 51[7]=0". 35
- Combined Register 53[11:10] to POWER_MODES. 36
- Added "The maximum PGA output level can be above 2Vpp even with the clamp circuit enabled..." in PROGRAMMABLE GAIN AMPLIFIER (PGA). 43
- Added Note: "In the low power and medium power modes, PGA_CLAMP is disabled for saving power if 51[7]=0" 43
- Changed "a programmable low-pass filter" to "a programmable butterworth low-pass filter" in PROGRAMMABLE GAIN AMPLIFIER (PGA). 43
- Added a note "The local oscillator inputs of the passive mixer are cos(ωt) for I-CH and sin(ωt) for Q-CH ...". 44
- Updated Figure 73that output clocks align at the rising edge of the 16X CLK. 47
- Added text "..It is recommended that $V_{CNTLM/P}$ noise is below 25 nV/rtHz at 1KHz and 5 nV/rtHz at 50 KHz. " 58
- Added a note "The local oscillator inputs of the passive mixer are cos(ωt) for I-CH and sin(ωt) for Q-CH ...". 61

- Added LMK048X as a jitter cleaner in CW Clock SelectionFigure 90. 63
- Added LMK devices in Figure 90. 64
- Added LMK devices in Figure 91. 65
- Added LMK048X as a jitter cleaner in CW Clock SelectionADC Clock Configurations. 65
- Added "it is recommended to keep sensitive input pins, such as INM, INP, ACT pins away from the AVDD 3.3 V, AVDD_5V, AVDD_ADC, DVDD, DVDD_LDO1/2, and other noise supply planes." 69

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
AFE5807ZCF	ACTIVE	NFBGA	ZCF	135	160	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 85	AFE5807	Samples

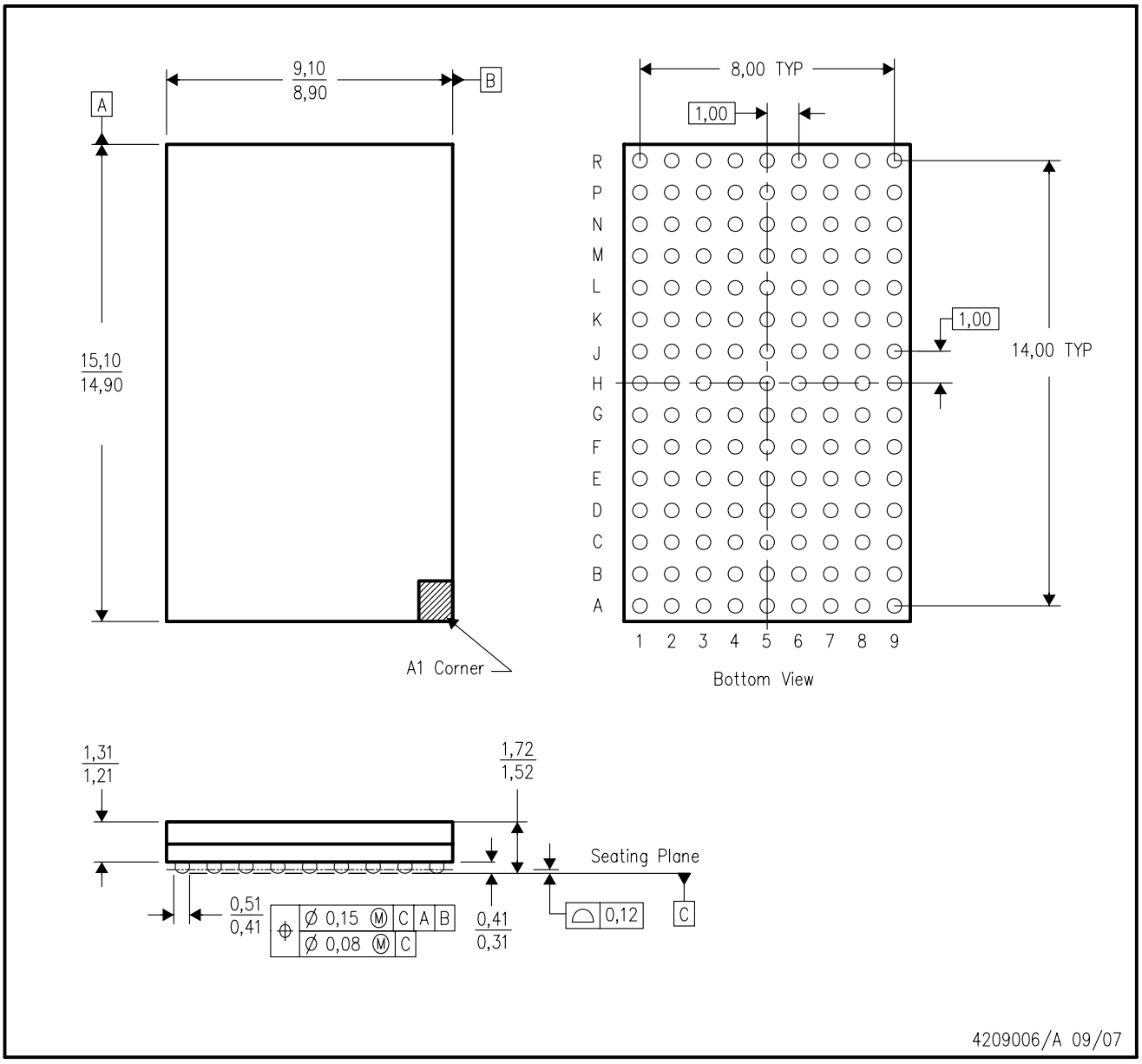
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

ZCF (R–PBGA–N135) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994 .
B. This drawing is subject to change without notice.
C. This is a lead–free solder ball design.

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