LMH6580/LMH6581 8x4 500 MHz Analog Crosspoint Switch, Gain of 1, Gain of 2

Check for Samples: LMH6580, LMH6581

FEATURES

- **8 Inputs and 4 Outputs**
- **48-pin TQFP Package**
- **−3 dB Bandwidth (V_{OUT} = 2 V_{PP}, R_L = 1 kΩ) 500 MHz**
- **−3 dB Bandwidth (V_{OUT} = 2 V_{PP}, R_L = 150Ω) 450 MHz**
- **Fast Slew Rate 2100 V/µs**
- **Channel to Channel Crosstalk (10/100 MHz) −70/ −52 dBc**
- **All Hostile Crosstalk (10/100 MHz) −55/−45 dBc**
- **Easy to Use Serial Programming 4 Wire Bus**
- **Two Programming Modes Serial & Addressed Modes**
- **Symmetrical Pinout Facilitates Expansion.**
- **Output Current ±70 mA**
- **Two Gain Options A_V = 1 or A_V = 2**

APPLICATIONS

- **Studio Monitoring/Production Video Systems**
- **Conference Room Multimedia Video Systems**
- **KVM (Keyboard Video Mouse) Systems**
- **Security/Surveillance Systems**
- **Multi-Antenna Diversity Radio**
- **Video Test Equipment**
- **Medical Imaging**
- **Wide-Band Routers & Switches**

DESCRIPTION

The LMH™ family of products is joined by the LMH6580 and the LMH6581, high speed, non-blocking, analog, crosspoint switches. The LMH6580/LMH6581 are designed for high speed, DC coupled, analog signals such as high resolution video (UXGA and higher). The LMH6580/LMH6581 each has eight inputs and four outputs. The non-blocking architecture allows any output to be connected to any input, including an input that is already selected. With fully buffered inputs the LMH6580/LMH6581 can be impedance matched to nearly any source impedance. The buffered outputs of the LMH6580/LMH6581 can drive up to two back terminated video loads (75Ω load). The outputs and inputs also feature high impedance inactive states allowing high performance input and output expansion for array sizes such as 8 x 8 or 16 x 4 by combining two devices. The LMH6580/LMH6581 are controlled with a 4 pin serial interface that can be configured as a 3 wire interface. Both serial mode and addressed modes are available.

The LMH6580/LMH6581 come in 48-pin TQFP packages. They also have diagonally symmetrical pin assignments to facilitate double sided board layouts and easy pin connections for expansion.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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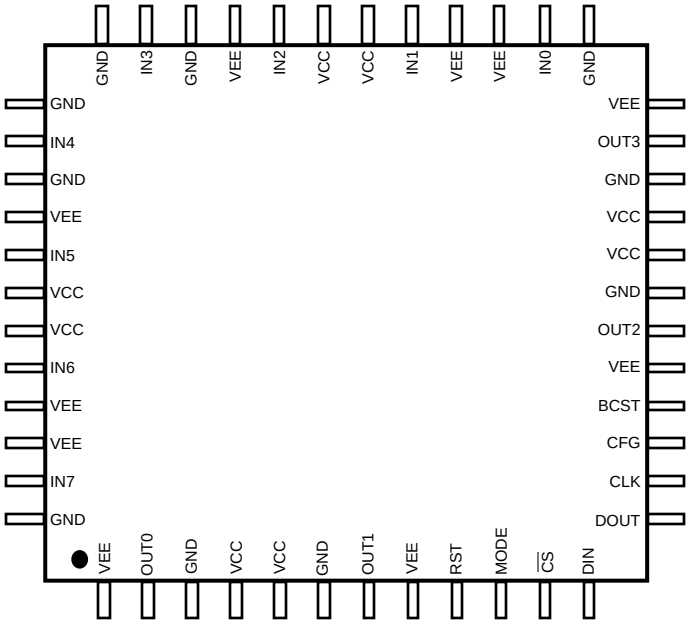
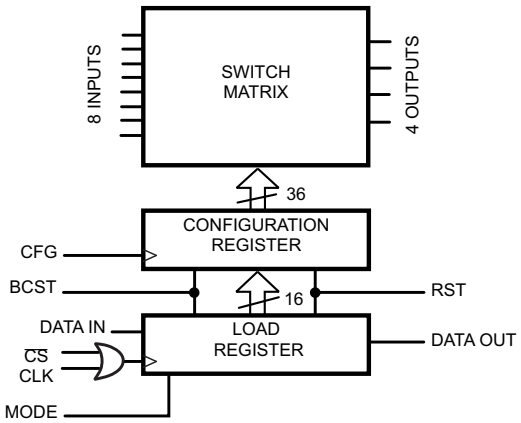
Connection Diagram



Block Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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ABSOLUTE MAXIMUM RATINGS(1)(2)

ESD Tolerance(3)	Human Body Model	2000V
	Machine Model	200V
V_S		±6V
I_{IN} (Input Pins)		±20 mA
I_{OUT}		See(4)
Input Voltage Range		V^- to V^+
Maximum Junction Temperature		+150°C
Storage Temperature Range		−65°C to +150°C
Soldering Information	Infrared or Convection (20 sec.)	235°C
	Wave Soldering (10 sec.)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see ±3.3V Electrical Characteristics and ±5V Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(4) The maximum output current (I_{OUT}) is determined by device power dissipation limitations. The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

OPERATING RATINGS(1)

Temperature Range(2)		−40°C to +85°C
Supply Voltage Range		±3V to ±5.5V
Thermal Resistance 48-Pin TQFP	θ_{JA}	44°C/W
	θ_{JC}	12°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see ±3.3V Electrical Characteristics and ±5V Electrical Characteristics.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

±3.3V ELECTRICAL CHARACTERISTICS(1)

Unless otherwise specified, typical conditions are: T_A = 25°C, A_V = +2, V_S = ±3.3V, R_L = 100Ω; **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min(2)	Typ(3)	Max(2)	Units
Frequency Domain Performance						
SSBW	−3 dB Bandwidth	V_{OUT} = 0.5 V_{PP}		425		MHz
LSBW		LMH6580 V_{OUT} = 1 V_{PP}, LMH6581 V_{OUT} = 2 V_{PP}, R_L = 1 kΩ		500		
		LMH6580 V_{OUT} = 1 V_{PP}, LMH6581 V_{OUT} = 2 V_{PP}, R_L = 150Ω		450		
GF	0.1 dB Gain Flatness	LMH6580 V_{OUT} = 1 V_{PP}, LMH6581 V_{OUT} = 2 V_{PP}, R_L = 150Ω		70		MHz
Time Domain Response						
t_r	Rise Time	LMH6580 1V Step, LMH6581 2V Step, 10% to 90%		3.1		ns
t_f	Fall Time	LMH6580 1V Step, LMH6581 2V Step, 10% to 90%		1.4		ns

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. No ensured parametric performance is indicated in the electrical tables under conditions different than those tested.
(2) Room Temperature limits are 100% production tested at 25°C. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.

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±3.3V ELECTRICAL CHARACTERISTICS[1] (continued)

Unless otherwise specified, typical conditions are: T_A = 25°C, A_V = +2, V_S = ±3.3V, R_L = 100Ω; **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min[2]	Typ[3]	Max[2]	Units
OS	Overshoot	2V Step		<1		%
SR	Slew Rate	LMH6580, 2 V_{PP}, 40% to 60%[4]		900		V/µs
	Slew Rate	LMH6581, 2 V_{PP}, 40% to 60%[4]		1700		V/µs
t_s	Settling Time	2V Step, V_{OUT} within 0.5%		7		ns
Distortion And Noise Response						
HD2	2nd Harmonic Distortion	2 V_{PP}, 10 MHz		−76		dBc
HD3	3rd Harmonic Distortion	2 V_{PP}, 10 MHz		−76		dBc
e_n	Input Referred Voltage Noise	>1 MHz		12		nV/ $\sqrt{Hz}$
i_n	Input Referred Noise Current	>1 MHz		2		pA/ $\sqrt{Hz}$
XTLK	Crosstalk	All Hostile, f = 100 MHz		−45		dBc
ISOL	Off Isolation	f = 100 MHz		−60		dBc
Static, DC Performance						
A_V	Gain	LMH6581	1.986	2.00	2.014	
		LMH6580	0.994	1.00	1.005	
V_{OS}	Input Offset Voltage			±3	±17	mV
TCV_{OS}	Input Offset Voltage Average Drift	See[5]		38		µV/°C
I_B	Input Bias Current	Non-Inverting[6]		−5		µA
TCI_B	Input Bias Current Average Drift	Non-Inverting[5]		−12		nA/°C
V_O	Output Voltage Range	LMH6581, R_L = 100Ω	±1.8	±2.1		V
		LMH6580, R_L = 100Ω	±1.24	±1.3		
V_O	Output Voltage Range	LMH6581, R_L = ∞Ω,[7]	±2.08	±2.2		V
		LMH6580 R_L = ∞Ω,	±1.25	±1.3		
PSRR	Power Supply Rejection Ratio			−45		dBc
I_{CC}	Positive Supply Current	R_L = ∞		50	60	mA
I_{EE}	Negative Supply Current	R_L = ∞		50	56	mA
	Tri State Supply Current	RST Pin > 2.0V		10	13	mA
Miscellaneous Performance						
R_{IN}	Input Resistance	Non-Inverting		100		kΩ
C_{IN}	Input Capacitance	Non-Inverting		1		pF
R_O	Output Resistance Enabled	Closed Loop, Enabled		300		mΩ
R_O	Output Resistance Disabled	LMH6580		50		kΩ
		LMH6581	1100	1350	1500	
CMVR	Input Common Mode Voltage Range			±1.3		V
I_O	Output Current	Sourcing, V_O = 0 V		±50		mA
Digital Control						
V_{IH}	Input Voltage High		2.0			V
V_{IL}	Input Voltage Low				0.8	V
V_{OH}	Output Voltage High			>2.0		V
V_{OL}	Output Voltage Low			<0.4		V
	Switching Time			15		ns
T_S	Setup Time			7		ns
T_H	Hold Time			7		ns

(4) Slew Rate is the average of the rising and falling edges.
(5) Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.
(6) Negative input current implies current flowing out of the device.
(7) This parameter is specified by design and/or characterization and is not tested in production.

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±5V ELECTRICAL CHARACTERISTICS(1)

Unless otherwise specified, typical conditions are: T_A = 25°C, A_V = +2, V_S = ±5V, R_L = 100Ω; **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min(2)	Typ(3)	Max(2)	Units
Frequency Domain Performance						
SSBW	−3 dB Bandwidth	V_{OUT} = 0.5 V_{PP}(4)		450		MHz
		LMH6580 V_{OUT} = 1 V_{PP}, LMH6581 V_{OUT} = 2 V_{PP}, R_L = 1 kΩ		500		
LSBW		LMH6580 V_{OUT} = 1 V_{PP}, LMH6581 V_{OUT} = 2 V_{PP}, R_L = 150Ω		450		
GF	0.1 dB Gain Flatness	LMH6580, V_{OUT} = 1 V_{PP}, LMH6581, V_{OUT} = 2 V_{PP}, R_L = 150Ω		100		MHz
DG	Differential Gain	R_L = 150Ω, 3.58 MHz/4.43 MHz		.05		%
DP	Differential Phase	R_L = 150Ω, 3.58 MHz/4.43 MHz		.05		deg
Time Domain Response						
t_r	Rise Time	LMH6580 2V, Step, 10% to 90%		2.8		ns
		LMH6581 2V, Step, 10% to 90%		1.2		
t_f	Fall Time	2V Step, 10% to 90%		1.6		ns
OS	Overshoot	2V Step		<1		%
SR	Slew Rate	LMH6580, 2 V_{PP}, 40% to 60%(5)		1200		V/µs
SR	Slew Rate	LMH6581, 6 V_{PP}, 40% to 60%(5)		2100		V/µs
t_s	Settling Time	2V Step, V_{OUT} Within 0.5%		6		ns
Distortion And Noise Response						
HD2	2nd Harmonic Distortion	2 V_{PP}, 5 MHz		−80		dBc
HD3	3rd Harmonic Distortion	2 V_{PP}, 5 MHz		−70		dBc
e_n	Input Referred Voltage Noise	>1 MHz		12		nV/ √Hz
i_n	Input Referred Noise Current	>1 MHz		2		pA/ √Hz
XTLK	Cross Talk	All Hostile, f = 100 MHz		−45		dBc
		Channel to Channel, f = 100 MHz		−52		dBc
ISOL	Off Isolation	f = 100 MHz		−65		dBc
Static, DC Performance						
A_V	Gain	LMH6581	1.986	2.00	2.014	
		LMH6580	0.995	1.00	1.005	
V_{os}	Input Offset Voltage			±2	±17	mV
TCV_{os}	Input Offset Voltage Average Drift	See(6)		38		µV/°C
I_B	Input Bias Current	Non-Inverting(7)		−5	±12	µA
TCI_B	Input Bias Current Average Drift	Non-Inverting(6)		−12		nA/°C
V_O	Output Voltage Range	LMH681, R_L = 100Ω	±3.4	±3.6		V
		LMH6580, R_L = 100Ω	±2.9	±3.0		
V_O	Output Voltage Range	LMH6581, R_L = ∞Ω	±3.7	±3.9		V
		LMH6580, R_L = ∞Ω	±2.9	±3.0		
PSRR	Power Supply Rejection Ratio	DC	−42	−45		dBc

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. No ensured parametric performance is indicated in the electrical tables under conditions different than those tested.
(2) Room Temperature limits are 100% production tested at 25°C. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(4) This parameter is specified by design and/or characterization and is not tested in production.
(5) Slew Rate is the average of the rising and falling edges.
(6) Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.
(7) Negative input current implies current flowing out of the device.

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±5V ELECTRICAL CHARACTERISTICS[1] (continued)

Unless otherwise specified, typical conditions are: T_A = 25°C, A_V = +2, V_S = ±5V, R_L = 100Ω; **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min[2]	Typ[3]	Max[2]	Units
XTLK	DC Crosstalk Rejection	DC, Channel to Channel	−62	−90		dBc
OISO	DC Off Isloation	DC	−60	−90		dBc
I_{CC}	Positive Supply Current	R_L = ∞		54	66	mA
I_{EE}	Negative Supply Current	R_L = ∞		50	62	mA
	Tri State Supply Current	RST Pin > 2.0V		14	17	mA
Miscellaneous Performance						
R_{IN}	Input Resistance	Non-Inverting		100		kΩ
C_{IN}	Input Capacitance	Non-Inverting		1		pF
R_O	Output Resistance Enabled	Closed Loop, Enabled		300		mΩ
R_O	Output Resistance Disabled	LMH6580, Resistance to Ground		50		kΩ
		LMH6581, Resistance to Ground	1100	1300	1500	
CMVR	Input Common Mode Voltage Range			±3.0		V
I_O	Output Current	Sourcing, V_O = 0 V	±60	±70		mA
Digital Control						
V_{IH}	Input Voltage High		2.0			V
V_{IL}	Input Voltage Low				0.8	V
V_{OH}	Output Voltage High			>2.4		V
V_{OL}	Output Voltage Low			<0.4		V
	Switching Time			15		ns
T_S	Setup Time			5		ns
T_H	Hold Time			5		ns

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TYPICAL PERFORMANCE CHARACTERISTICS LMH6580

1 V_{PP} Frequency Response

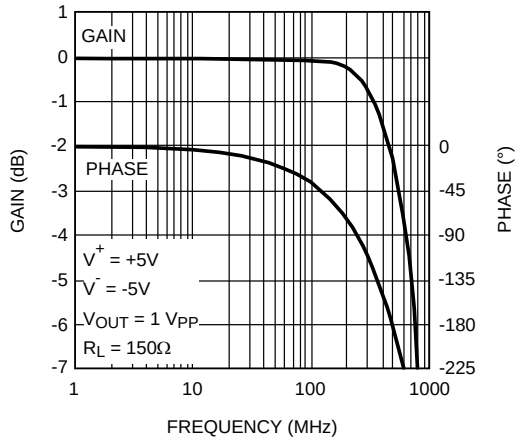

Figure 1.

1 V_{PP} Frequency Response

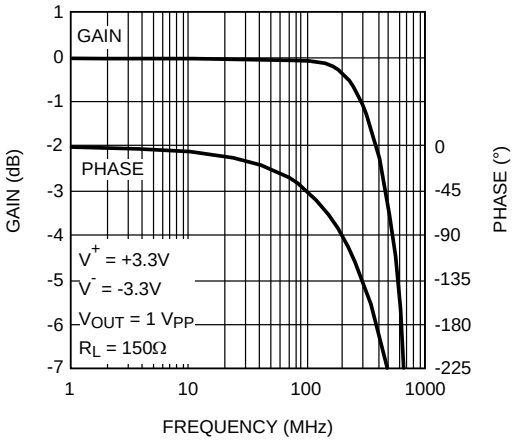

Figure 2.

1 V_{PP} Frequency Response Broadcast

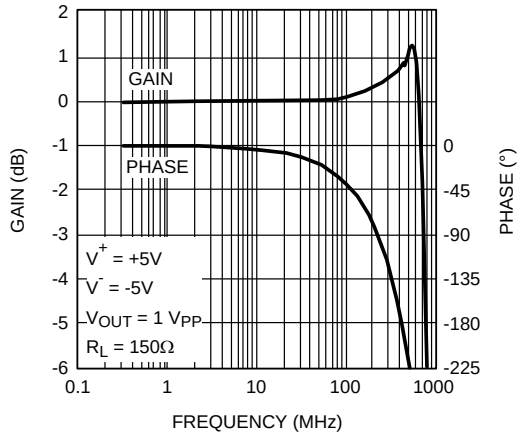

Figure 3.

1 V_{PP} Frequency Response Broadcast

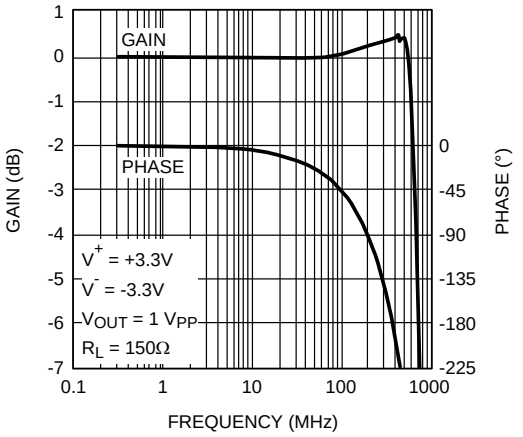

Figure 4.

Frequency Response 1 kΩ Load

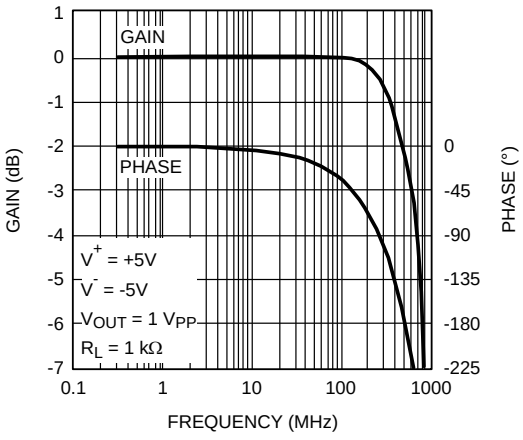

Figure 5.

Frequency Response 1kΩ Load

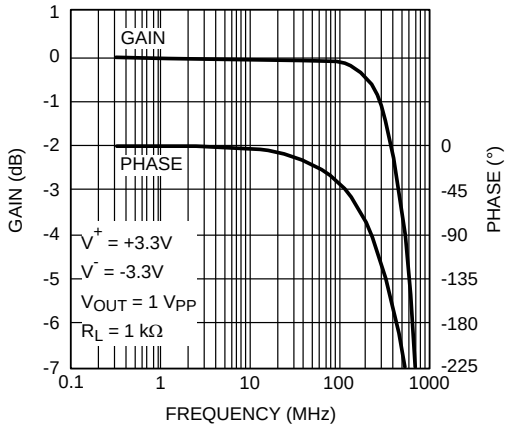

Figure 6.

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TYPICAL PERFORMANCE CHARACTERISTICS LMH6580 (continued)

Frequency Response with Input Expansion

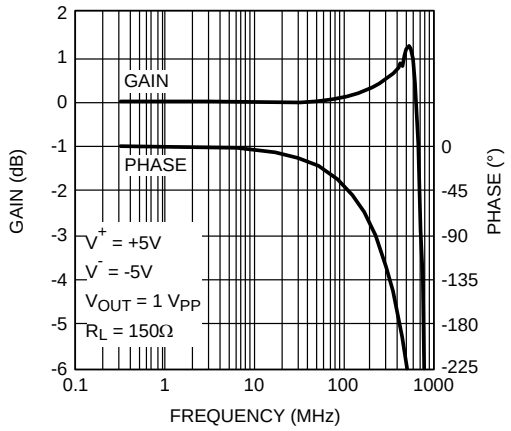

Figure 7.

Frequency Response with Input Expansion

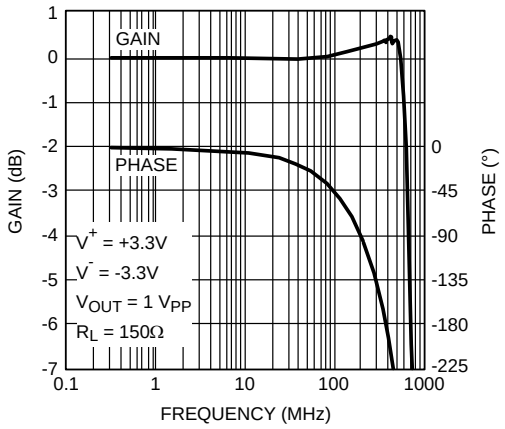

Figure 8.

2 V_{PP} Pulse Response

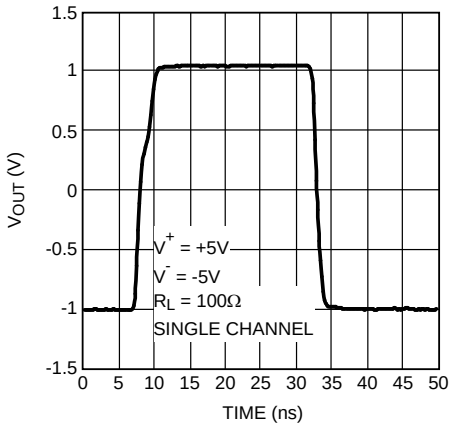

Figure 9.

2 V_{PP} Pulse Response

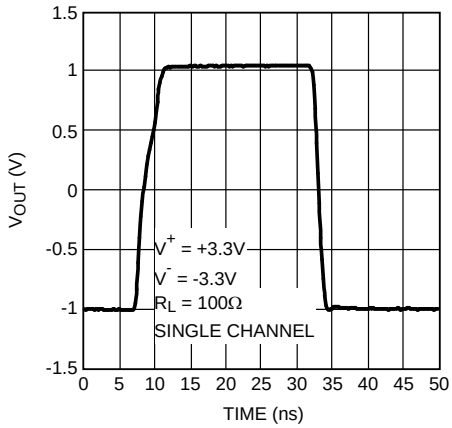

Figure 10.

2 V_{PP} Pulse Response, Broadcast Mode

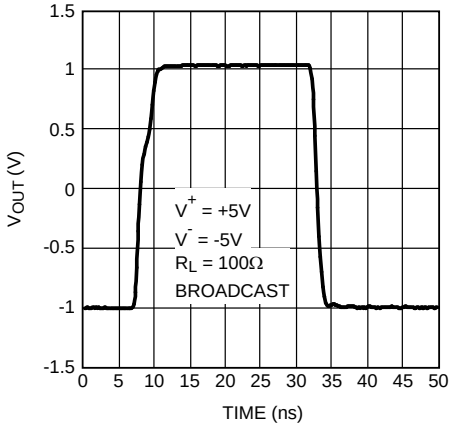

Figure 11.

2 V_{PP} Pulse Response, Broadcast Mode

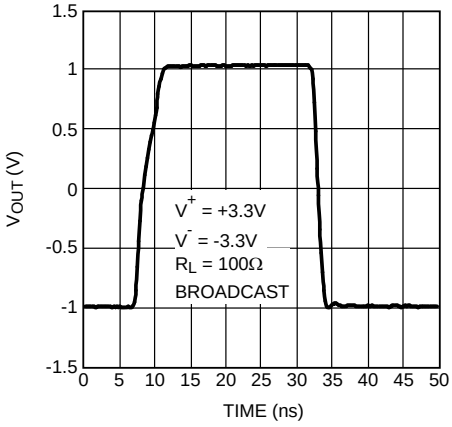

Figure 12.

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TYPICAL PERFORMANCE CHARACTERISTICS LMH6580 (continued)

1 V_{PP} Pulse Response

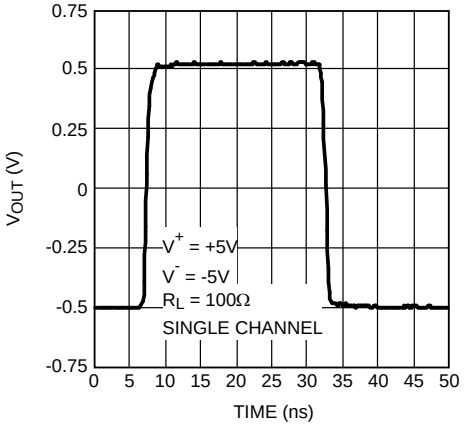

Figure 13.

1 V_{PP} Pulse Response

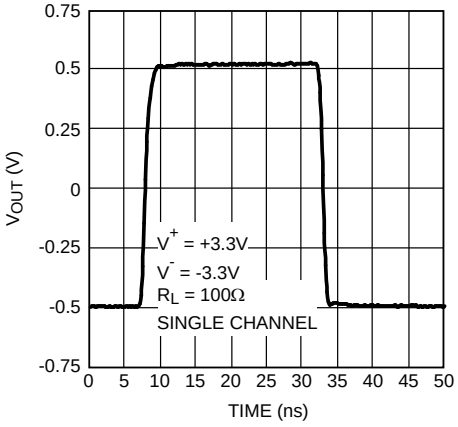

Figure 14.

Channel to Channel Crosstalk

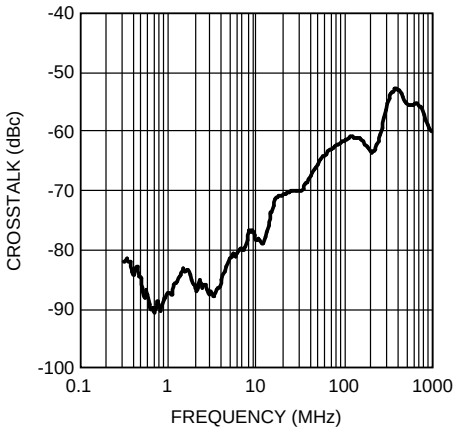

Figure 15.

All Hostile Crosstalk

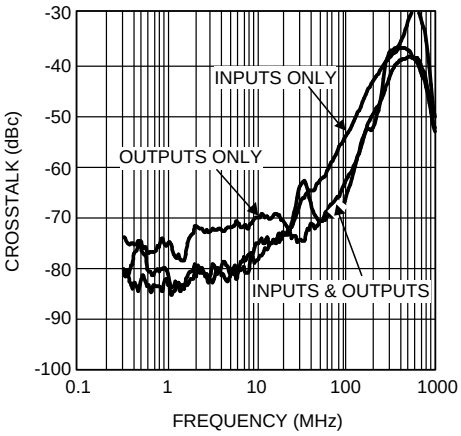

Figure 16.

Second Order Distortion (HD2) vs. Frequency

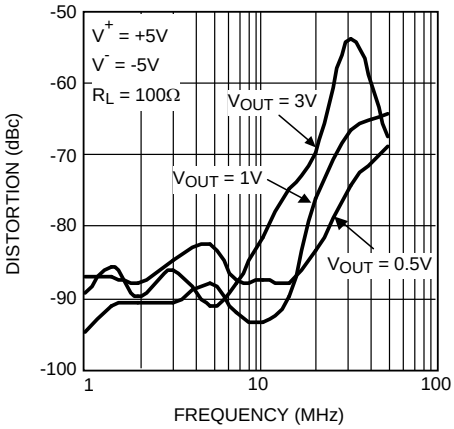

Figure 17.

Third Order Distortion (HD3) vs. Frequency

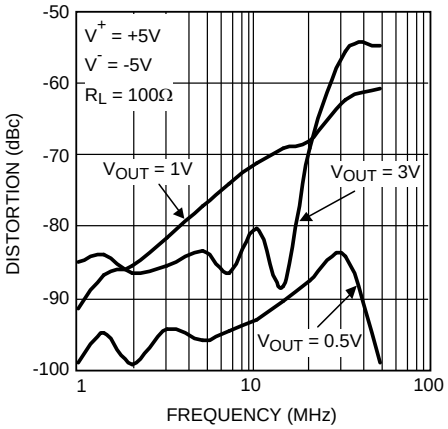

Figure 18.

TYPICAL PERFORMANCE CHARACTERISTICS LMH6580 (continued)

Second Order Distortion (HD2) vs. Frequency

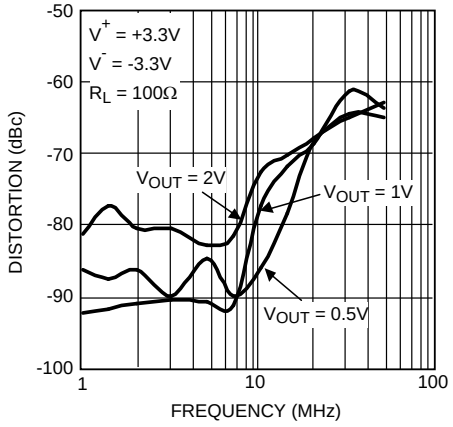

Figure 19.

Third Order Distortion (HD3) vs. Frequency

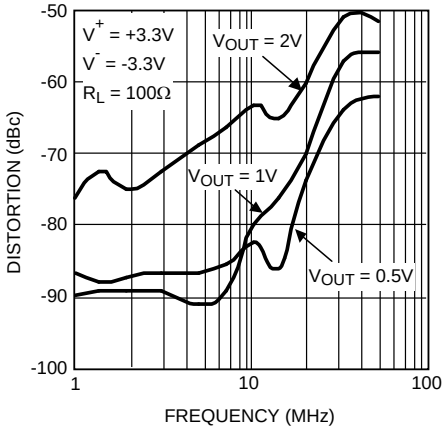

Figure 20.

Positive Voltage Swing over Temperature

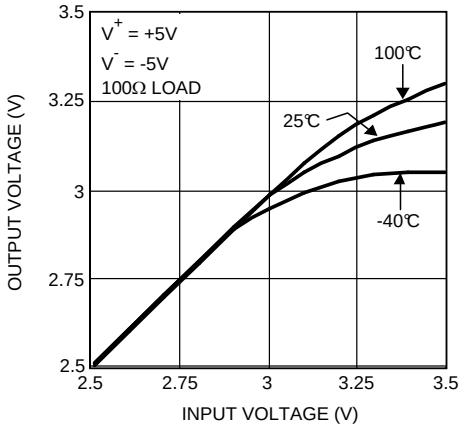

Figure 21.

Negative Voltage Swing over Temperature

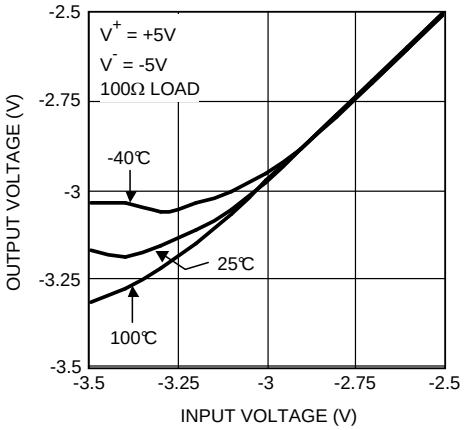

Figure 22.

Positive Voltage Swing over Temperature

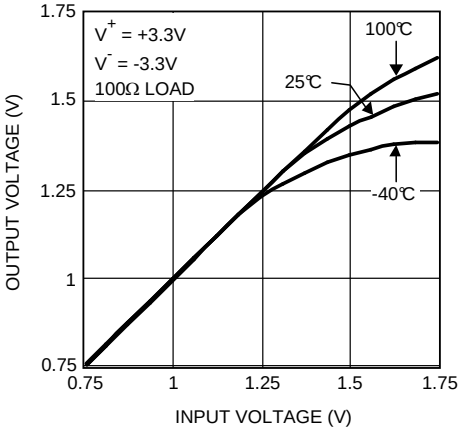

Figure 23.

Negative Voltage Swing over Temperature

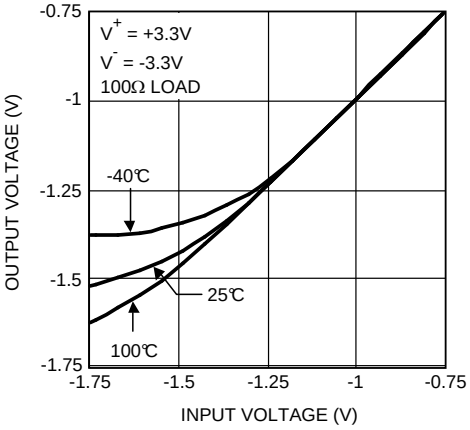

Figure 24.

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TYPICAL PERFORMANCE CHARACTERISTICS LMH6580 (continued)

Enabled Output Impedance

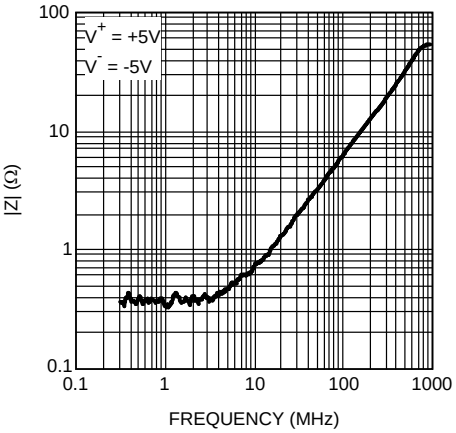

Figure 25.

Enabled Output Impedance

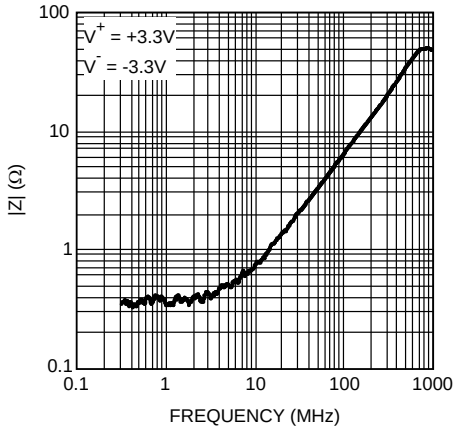

Figure 26.

Disabled Output Impedance

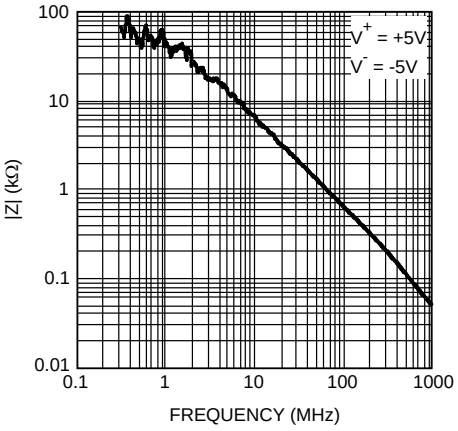

Figure 27.

Disabled Output Impedance

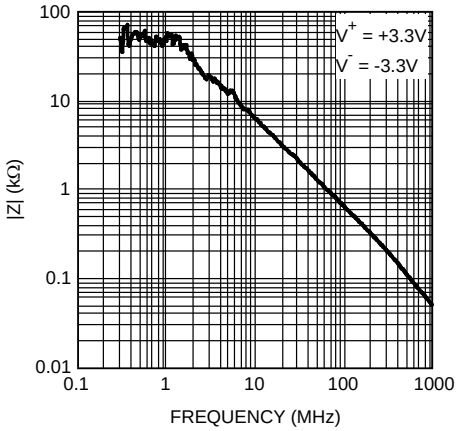

Figure 28.

Switching Time

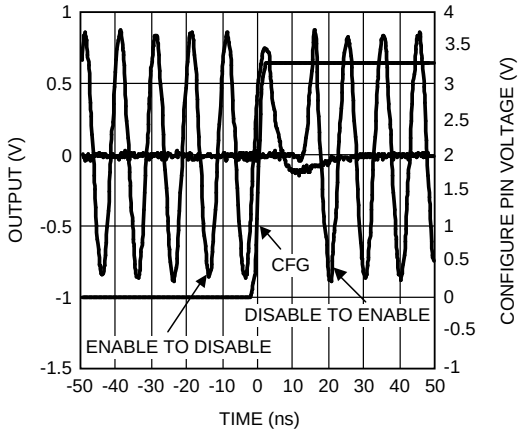

Figure 29.

TYPICAL PERFORMANCE CHARACTERISTICS LMH6581

2 V_{PP} Frequency Response

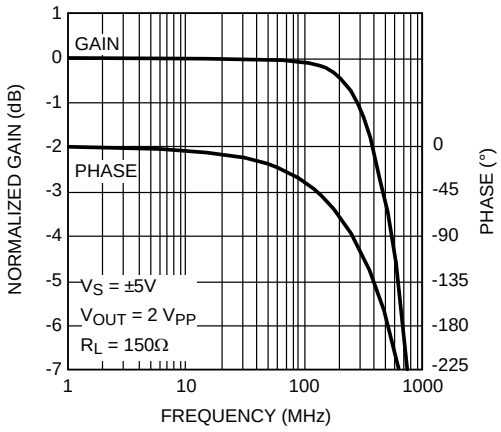

Figure 30.

2 V_{PP} Frequency Response

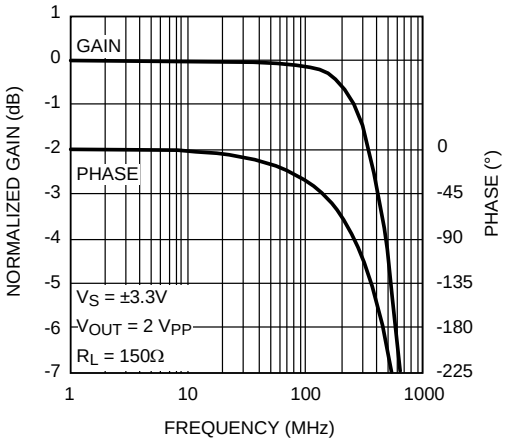

Figure 31.

Large Signal Bandwidth

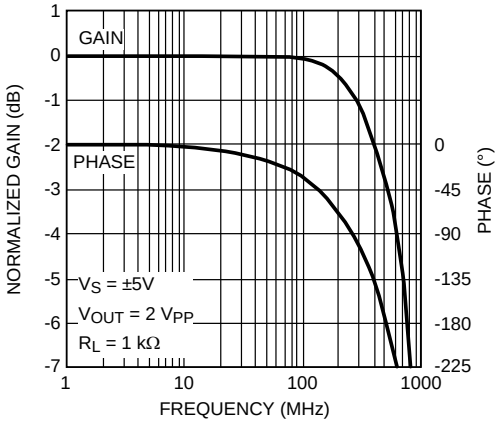

Figure 32.

Large Signal Bandwidth

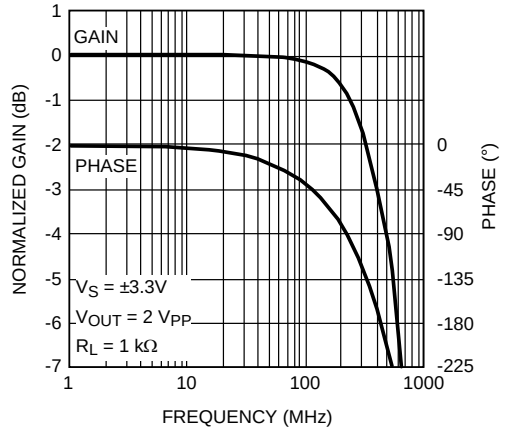

Figure 33.

Small Signal Bandwidth

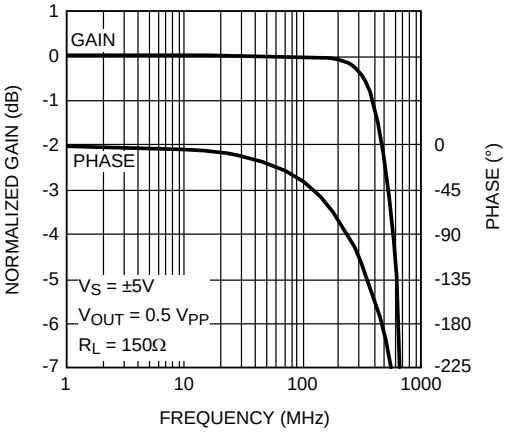

Figure 34.

Small Signal Bandwidth

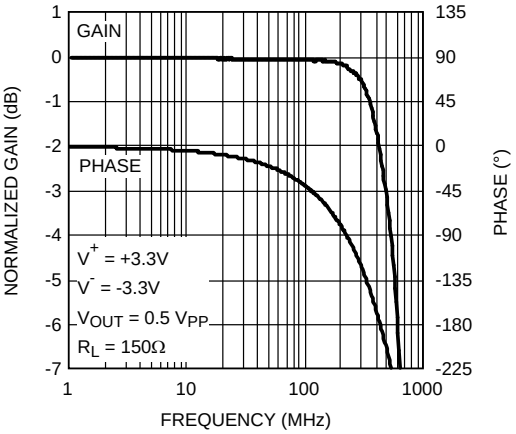

Figure 35.

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TYPICAL PERFORMANCE CHARACTERISTICS LMH6581 (continued)

Frequency Response 1 kΩ Load

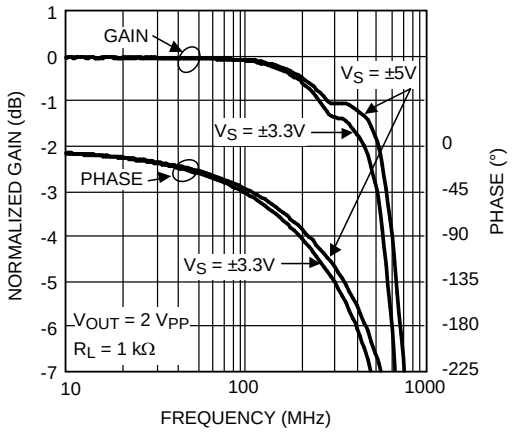

Figure 36.

Group Delay

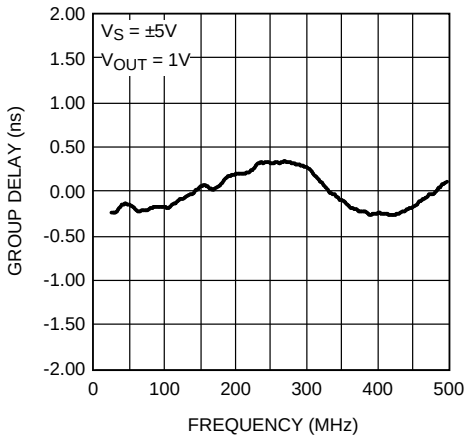

Figure 37.

2 V_{PP} Pulse Response

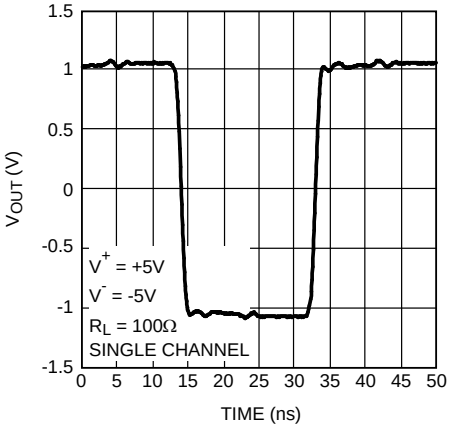

Figure 38.

2 V_{PP} Pulse Response

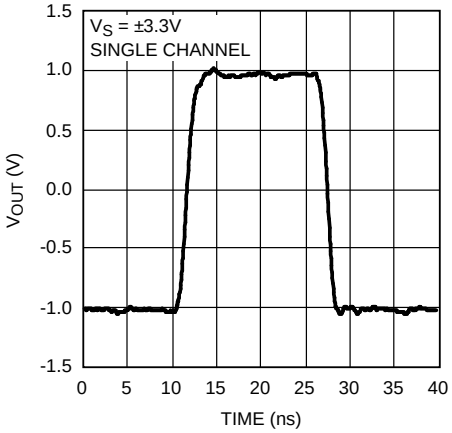

Figure 39.

4 V_{PP} Pulse Response

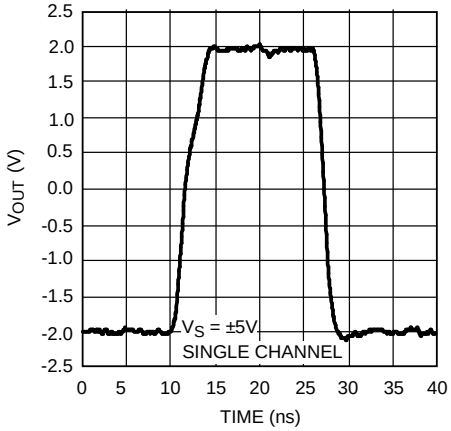

Figure 40.

4 V_{PP} Pulse Response Broadcast

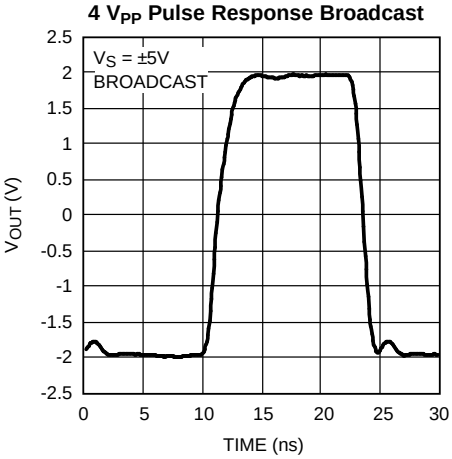

Figure 41.

TYPICAL PERFORMANCE CHARACTERISTICS LMH6581 (continued)

4 V_{PP} Pulse Response

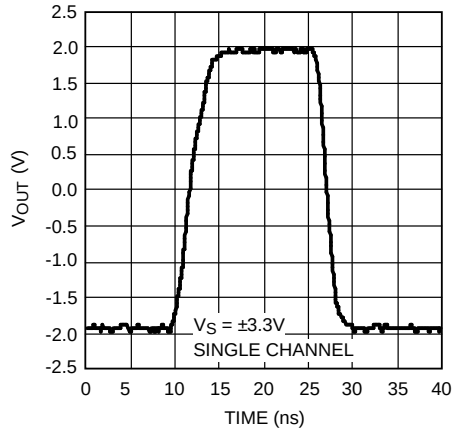

Figure 42.

6 V_{PP} Pulse Response

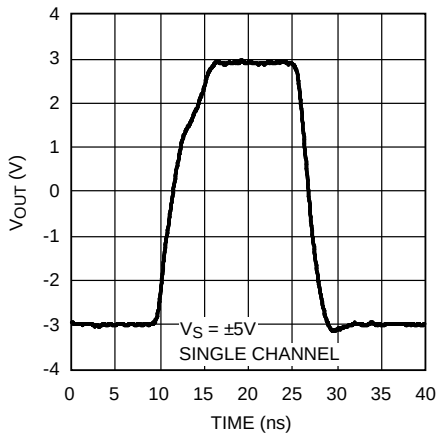

Figure 43.

Off Isolation

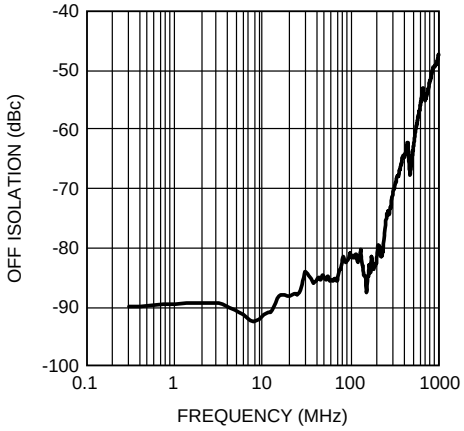

Figure 44.

All Hostile Crosstalk

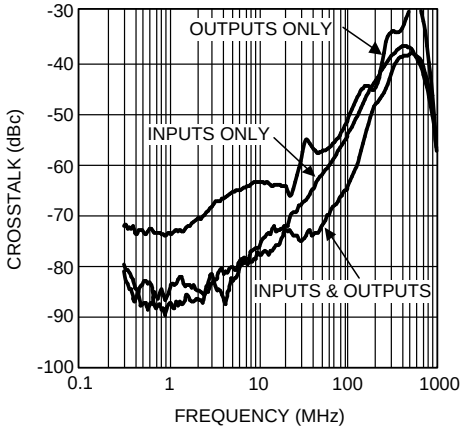

Figure 45.

Second Order Distortion (HD2) vs. Frequency

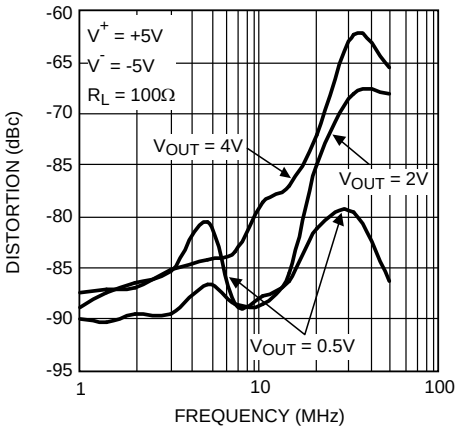

Figure 46.

Third Order Distortion (HD3) vs. Frequency

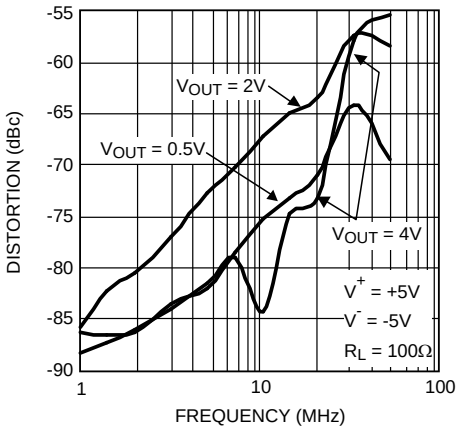

Figure 47.

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TYPICAL PERFORMANCE CHARACTERISTICS LMH6581 (continued)

Second Order Distortion vs. Frequency

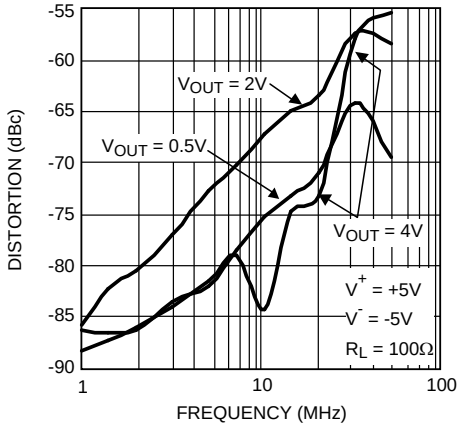

Figure 48.

Third Order Distortion vs. Frequency

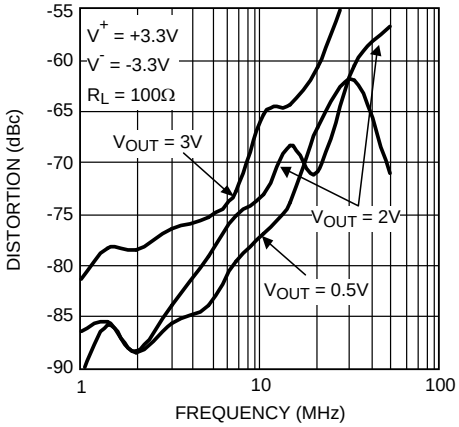

Figure 49.

No Load Output Swing

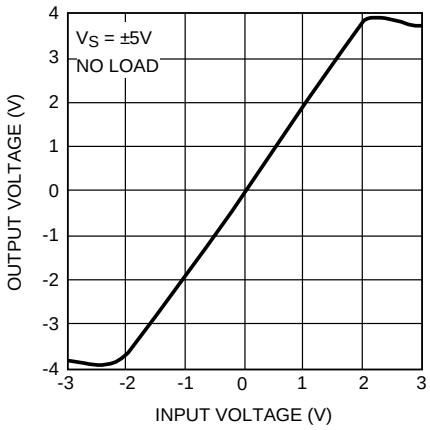

Figure 50.

Positive Swing over Temperature

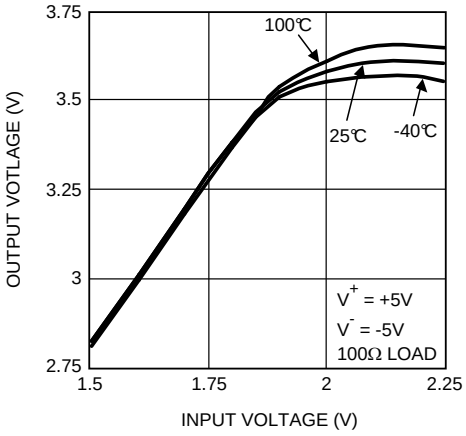

Figure 51.

Negative Swing Over Temperature

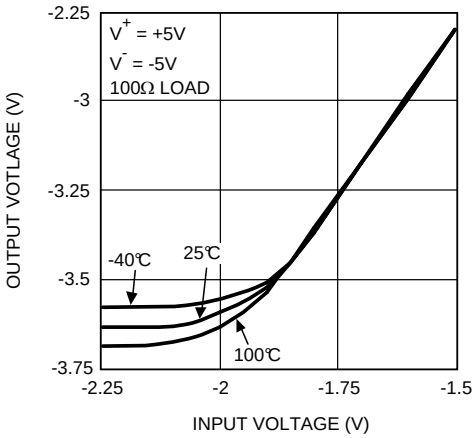

Figure 52.

No Load Output Swing

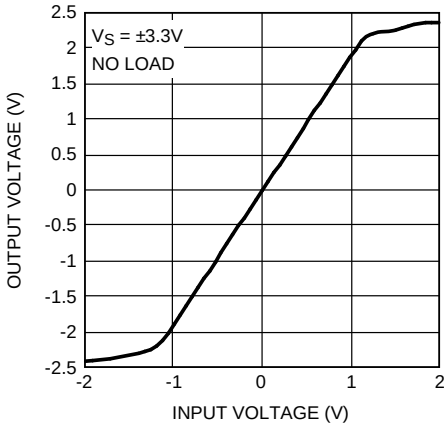

Figure 53.

TYPICAL PERFORMANCE CHARACTERISTICS LMH6581 (continued)

Positive Swing over Temperature

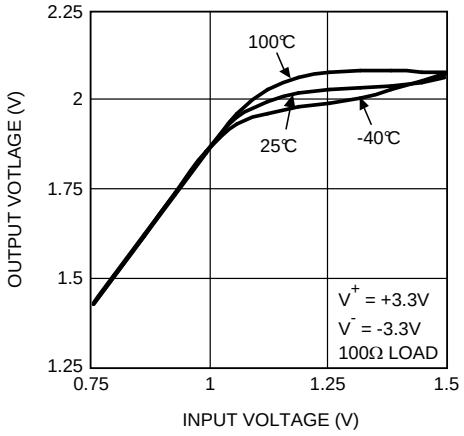

Figure 54.

Negative Swing over Temperature

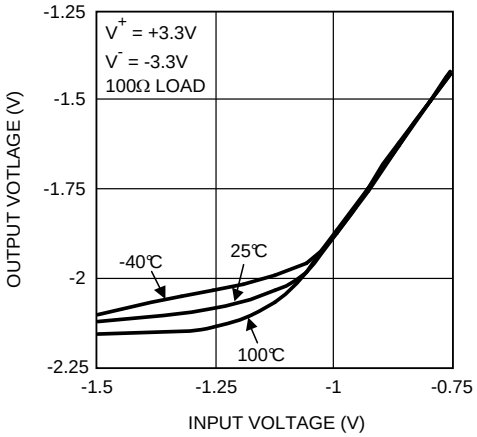

Figure 55.

Enabled Output Impedance

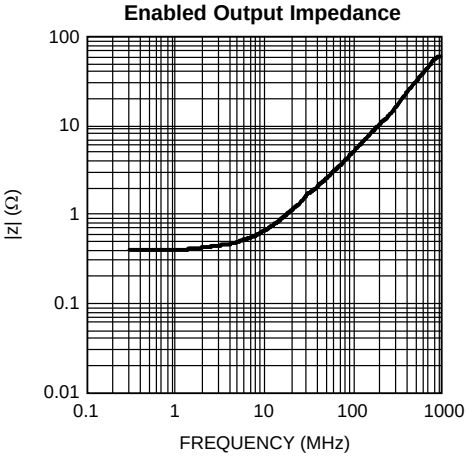

Figure 56.

Disabled Output Impedance

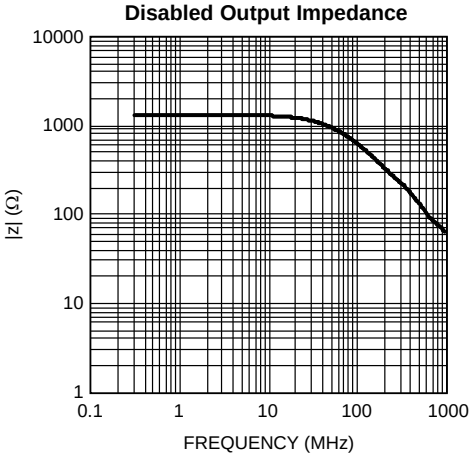

Figure 57.

Switching Time

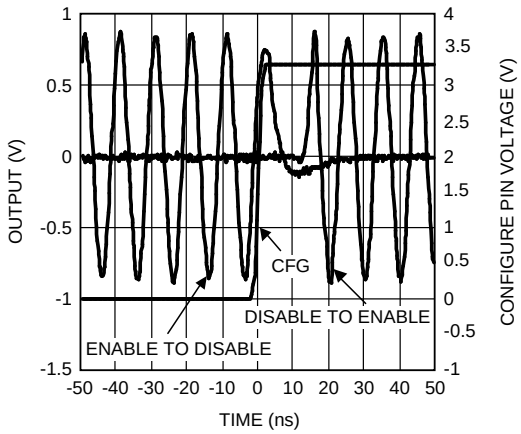

Figure 58.

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APPLICATION INFORMATION

INTRODUCTION

The LMH6580/LMH6581 are high speed, fully buffered, non- blocking, analog crosspoint switches. Having fully buffered inputs allows the LMH6580/LMH6581 to accept signals from low or high impedance sources without the worry of loading the signal source. The fully buffered outputs will drive 75Ω or 50Ω back terminated transmission lines with no external components other than the termination resistor. When disabled, the outputs are in a high impedance state. The LMH6580/LMH6581 can have any input connected to any (or all) output(s). Conversely, a given output can have only one associated input.

INPUT AND OUTPUT EXPANSION

The LMH6580/LMH6581 have high impedance inactive states for both inputs and outputs allowing maximum flexibility for crosspoint expansion. In addition the LMH6580/LMH6581 employ diagonal symmetry in pin assignments. The diagonal symmetry makes it easy to use direct pin to pin vias when the parts are mounted on opposite sides of a board. As an example two LMH6580/LMH6581 chips can be combined on one board to form either an 8 x 8 crosspoint or a 16 x 4 crosspoint. To make an 8 x 8 crosspoint all 8 input pins would be tied together (Input 0 on side 1 to input 7 on side 2 and so on) while the 4 output pins on each chip would be left separate. To make the 16 x 4 crosspoint, the 4 outputs would be tied together while all 16 inputs would remain independent. In the 16 x 4 configuration it is important not to have 2 connected outputs active at the same time. With the 8 x 8 configuration, on the other hand, having two connected inputs active is a valid state. Crosspoint expansion as detailed above has the advantage that the signal will go through only one crosspoint. Expansion methods that have cascaded stages will suffer bandwidth loss far greater than the small loading effect of parallel expansion.

Output expansion as shown in Figure 59 is very straight forward. Connecting the inputs of two crosspoint switches has a very minor impact on performance. Input expansion requires more planning. Input expansion, as show in Figure 60 and Figure 61 gives the option of two ways to connect the outputs of the crosspoint switches. In Figure 60 the crosspoint switch outputs are connected directly together and share one termination resistor. This is the easiest configurarion to implement and has only one drawback. Because the disabled output of the unused crosspoint (only one output can be active at a time) has a small amount of capacitance, the frequency response of the active crosspoint will show peaking. This is illustrated in Figure 62 and Figure 63. In most cases this small amount of peaking is not a problem.

As illustrated in Figure 61 each crosspoint output can be given its own termination resistor. This results in a frequency response nearly identical to the non expansion case. There is one drawback for the gain of 2 crosspoint, and that is gain error. With a 75Ω termination resistor the 1250Ω resistance of the disabled crosspoint output will cause a gain error. In order to counter act this the termination resistors of both crosspoints should be adjusted to approximately 80Ω. This will provide very good matching, but the gain accuracy of the system will now be dependent on the process variations of the crosspoint resistors which have a variability of approximately ±20%.

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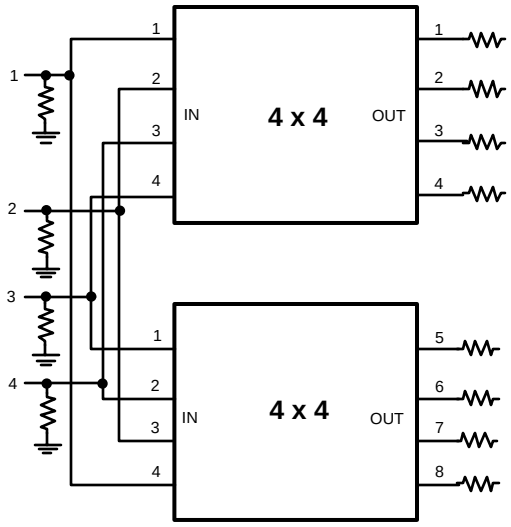

Figure 59. Output Expansion

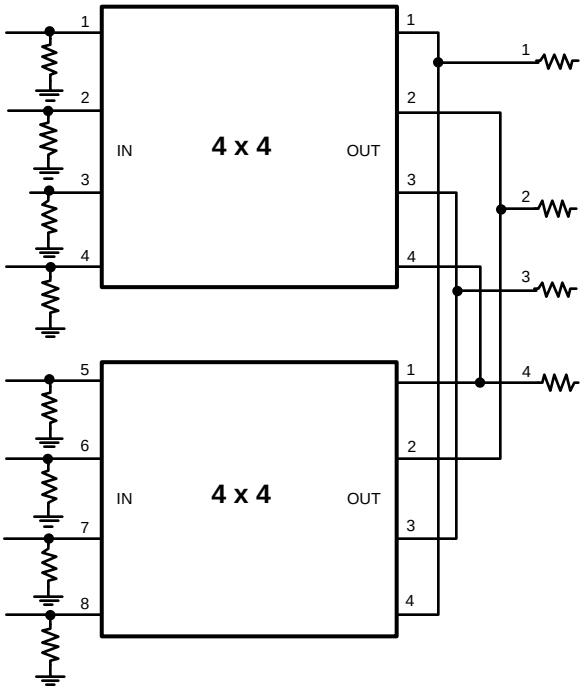

Figure 60. Input Expansion with Shared Termination Resistors

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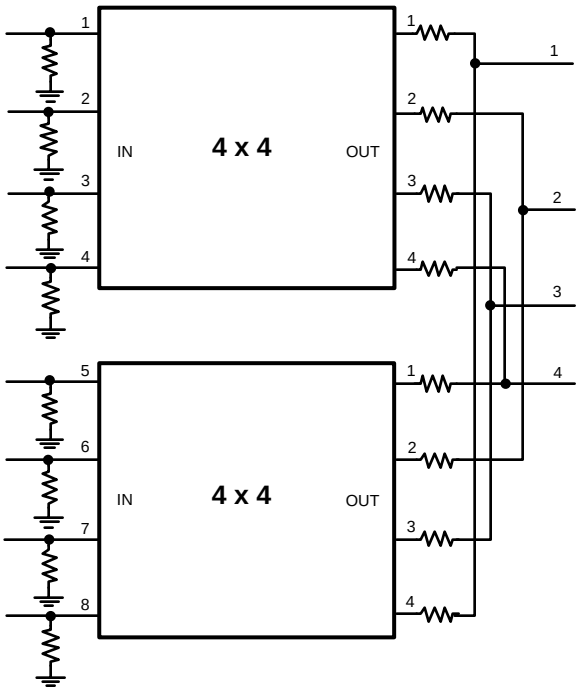

Figure 61. Input Expansion with Separate Termination Resistors

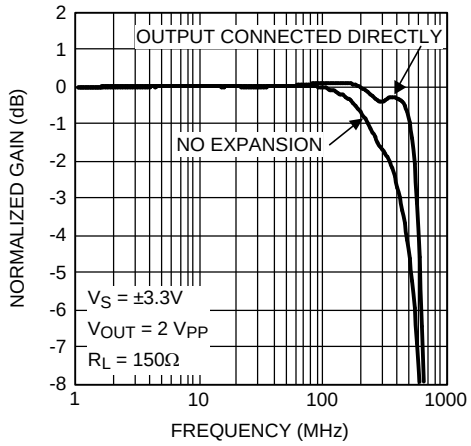

Figure 62. Input Expansion Frequency Response

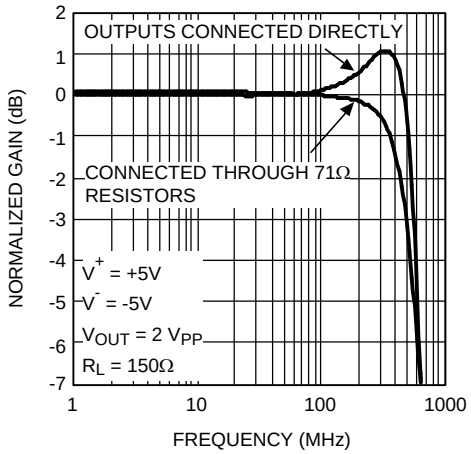

Figure 63. Input Expansion Frequency Response

DRIVING CAPACITIVE LOADS

Capacitive output loading applications will benefit from the use of a series output resistor R_{OUT}. Capacitive loads of 5 pF to 120 pF are the most critical, causing ringing, frequency response peaking and possible oscillation. Since most capacitive loading is due to undesired parasitic capacitances the values of the capacitive loading will not usually be known exactly. It is best to start with a conservative value of R_{OUT} and decrease the value until the bandwidth shows slight peaking. At this point the value of the isloation resistor will be determined by whether flat frequency response or maximum bandwidth is the desired goal. Smaller values of R_{OUT} will produce some peaking, but maximum bandwidth. Larger resistor values will decrease bandwidth and suppress peaking.

As starting values, a capacitive load of 5 pF should have around 75 Ω of isolation resistance. A value of 120 pF would require around 12Ω. When driving transmission lines, the output termination resistor is normally sufficient.

USING OUTPUT BUFFERING TO ENHANCE BANDWIDTH AND INCREASE REBIABILITY

The LMH6580/LMH6581 crosspoint switch can offer enhanced bandwidth and reliability with the use of external buffers on the outputs. The bandwidth is increased by unloading the outputs and driving the high impedance of an external buffer. See the Frequency Response 1 kΩ Load curve in Typical Performance section for an example of bandwidth achieved with less loading on the outputs. For this technique to provide maximum benefit a very high speed amplifier such as the LMH6703 should be used. As shown in Figure 64 the resistor R_L is placed between the crosspoint output and the buffer amplifier. This resistor will provide a load for the crosspoint output buffer and reduce peaking caused by the buffer input capacitance. A recommended value for R_L is 500Ω to 1000Ω. Higher values of R_L will give higher bandwidth, but also higher peaking. The optimum value of R_L will depend greatly on board layout and the input capacitance of the buffer amplifier.

Besides offering enhanced bandwidth performance using an external buffer provides greater system reliability. The first advantage is to reduce thermal loading on the crosspoint switch. This reduced die temperature will increase the life of the crosspoint. The second advantage is enhanced ESD reliability. It is very difficult to build high speed devices that can withstand all possible ESD events. With external buffers the crosspoint switch is isolated from ESD events on the external system connectors.

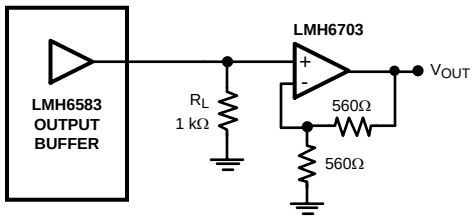

Figure 64. Buffered Output

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CROSSTALK

When designing a large system such as a video router crosstalk can be a very serious problem. Extensive testing in our lab has shown that most crosstalk is related to board layout rather than occurring in the crosspoint switch. There are many ways to reduce board related crosstalk. Using controlled impedance lines is an important step. Using well decoupled power and ground planes will help as well. When crosstalk does occur within the crosspoint switch itself it is often due to signals coupling into the power supply pins. Using appropriate supply bypassing will help to reduce this mode of coupling. Another suggestion is to place as much grounded copper as possible between input and output signal traces. Care must be taken, though, not to influence the signal trace impedances by placing shielding copper too closely. One other caveat to consider is that as shielding materials come closer to the signal trace the trace needs to be smaller to keep the impedance from falling too low. Using thin signal traces will result in unacceptable losses due to trace resistance. This effect becomes even more pronounced at higher frequencies due to the skin effect. The skin effect reduces the effective thickness of the trace as frequency increases. Resistive losses make crosstalk worse because as the desired signal is attenuated with higher frequencies crosstalk increases at higher frequencies.

DIGITAL CONTROL

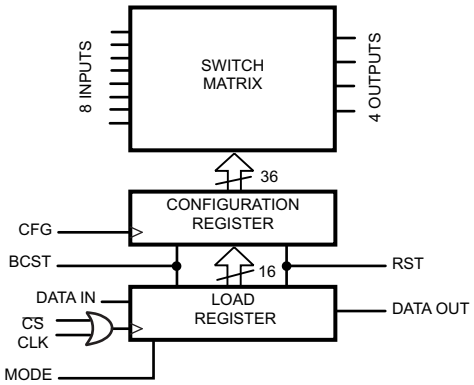

Figure 65. Block Diagram

Table 1. Logic Pins

Pin Name	Level Sensitive	Edge Triggered	Triggered by
CLK	Yes		
$\overline{CS}$		Yes	CLK rising edge
DATA IN		Yes	CLK falling edge
DATA OUT		Yes	CLK rising edge
CFG	Yes		
MODE	Yes		
RST	Yes		
BCST	Yes		

There are two modes for programing the LMH6580/LMH6581, Serial Mode and Addressed Mode. The LMH6580/LMH6581 have internal control registers that store the programming states of the crosspoint switch. The logic is two staged to allow for maximum programming flexibility. The first stage of the control logic is tied directly to the crosspoint switching matrix. This logic consists of one register for each output that stores the on/off state and the address of which input to connect to. These registers are not directly accessible to the user. The second level of logic is another bank of registers identical to the first, but set up as shift registers. These registers are accessed by the user via the serial input bus.

The LMH6580/LMH6581 is programmed via a serial input bus with the support of four other digital control pins. The Serial bus consists of a clock pin (CLK), a serial data in pin (DIN), and a serial data out pin (D_{OUT}). The serial bus is gated by a chip select pin (CS). The chip select pin is active low. While the chip select pin is high all data on the serial input pin and clock pins is ignored. When the chip select pin is brought low the internal logic is set to begin receiving data by the first positive transition (0 to 1) of the clock signal. The chip select pin must be

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brought low at least 5 ns before the first rising edge of the clock signal. The first data bit is clocked in on the next negative transition (1 to 0) of the clock signal. All input data is read from the bus on the negative edge of the clock signal. Once the last valid data has been clocked in, either the chip select pin must go high or, the clock signal must stop. Otherwise invalid data will be clocked into the chip. The data clocked into the chip is not transferred to the crosspoint matrix until the CFG pin is pulsed high. This is the case regardless of the state of the MODE pin. The CFG pin is not dependent on the state of the Chip select pin. If no new data is clocked into the chip subsequent pulses on the CFG pin will have no effect on device operation.

The programming format of the incoming serial data is selected by the MODE pin. When the MODE pin is HIGH the crosspoint can be programmed one output at a time by entering a string of data that contains the address of the output that is going to be changed (Addressed Mode). When the mode pin is LOW the crosspoint is in Serial Mode. In this mode the crosspoint accepts a 16 bit array of data that programs all of the outputs. In both modes the data fed into the chip does not change the chip operation until the Configure pin is pulsed high. The configure and mode pins are independent of the chip select pin.

THREE WIRE VS. FOUR WIRE CONTROL

There are two ways to connect the serial data pins. The first way is to control all four pins separately, and the second option is to connect the CFG and the CS pins together for a 3 wire interface. The benefit of the 4-wire interface is that the chip can be configured independently using the CS pin. This would be an advantage in a system with multiple crosspoint chips where all of them could be programmed ahead of time and then configured simultaneously. The 4-wire solution is also helpful in a system that has a free running clock on the CLK pin. In this case, the CS pin needs to be brought high after the last valid data bit to prevent invalid data from being clocked into the chip.

The 3-wire option provides the advantage of one less pin to control at the expense of having less flexibility with the configure pin. One way around this loss of flexibility would be if the clock signal is generated by an FPGA or microcontroller where the clock signal can be stopped after the data is clocked in. In this case the Chip select function is provided by the presence or absence of the clock signal.

SERIAL PROGRAMMING MODE

Serial programming mode is the mode selected by bringing the MODE pin low. In this mode a stream of 16-bits programs all four outputs of the crosspoint. The data is fed to the chip as shown in Table 2 and Table 3 (two tables are required to show the entire data frame). The table is arranged such that the first bit clocked into the crosspoint register is labeled bit number 0. The register labeled Load Register in Figure 65 is a shift register. If the chip select pin is left low after the valid data is shifted into the chip and if the clock signal keeps running then additional data will be shifted into the register, and the desired data will be shifted out.

Also illustrated is the timing relationships for the digital pins in Figure 66. It is important to note that all the pin timing relationships are important, not just the data and clock pins. One example is that the Chip Select pin (CS) must transition low before the first rising edge of the clock signal. This allows the internal timing circuits to synchronize to allow data to be accepted on the next falling edge. The chip select pin must then transition high after the final data bit has been clocked in and before another clock signal positive edge occurs to prevent invalid data from being clocked into the chip. Another way to accomplish the same thing is to strobe the clock pin with only the desired number of pulses starting and ending with clock in the low condition. The configure (CFG) pin timing is not so critical, but it does need to be kept low until all data has been shifted into the crosspoint registers.

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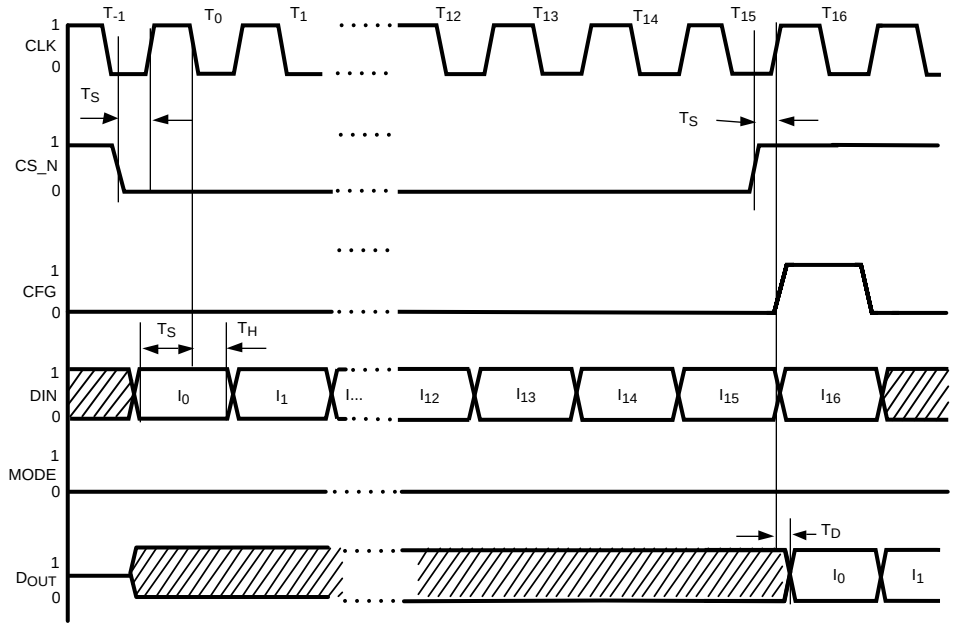

Figure 66. Timing Diagram for Serial Mode

Table 2. Serial Mode Data Frame (First Two Words)(1)

Output 0				Output 1			
Input Address			On = 0	Input Address			On = 0
LSB		MSB	Off = 1	LSB	LSB		Off = 1
0	1	2	3	4	5	6	7

(1) Off = TRI-STATE, Bit 0 is first bit clocked into device.

Table 3. Serial Mode Data Frame (Continued)

Output 2				Output 3			
Input Address			On = 0	Input Address			On = 0
LSB		MSB	Off = 1	LSB		MSB	Off = 1
8	9	10	11	12	13	14	15

ADDRESSED PROGRAMMING MODE

Addressed programming mode makes it possible to change only one output register at a time. To utilize this mode the mode pin must be High. All other pins function the same as in serial programming mode except that the word clocked in is 5 bits and is directed only at the output specified. In addressed mode the data format is shown below in Table 4.

Also illustrated is the timing relationships for the digital pins in Figure 67. It is important to note that all the pin timing relationships are important, not just the data and clock pins. One example is that the Chip Select pin (CS) must transition low before the first rising edge of the clock signal. This allows the internal timing circuits to synchronize to allow data to be accepted on the next falling edge. The chip select pin must then transition high after the final data bit has been clocked in and before another clock signal positive edge occurs to prevent invalid data from being clocked into the chip. Also, in addressed mode is it necessary for the clock signal to make a low to high transition after the chip select pin has been brought high. If there is not a low to high transition of the clock after the chip select pin goes high subsequent data wil not be loaded into the chip properly. The configure (CFG) pin timing is not critical, but it does need to be kept low until all data has been shifted into the crosspoint registers.

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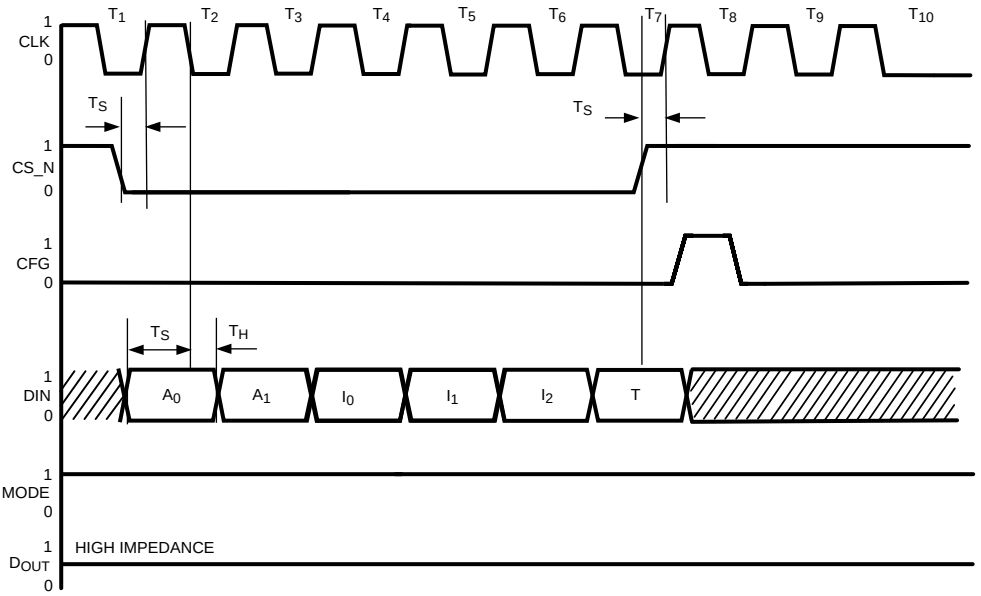

Figure 67. Timing Diagram for Addressed Mode

Table 4. Addressed Mode Word Format(1)

Output Address		Input Address			TRI-STATE
LSB	MSB	LSB		MSB	1 = TRI-STATE 0 = On
0	1	2	3	4	5

(1) Bit 0 is first bit clocked into device.

DAISY CHAIN OPTION IN SERIAL MODE

The LMH6580/LMH6581 supports daisy chaining of the serial data stream between multiple chips. This feature is available only in the Serial Programming Mode. To use this feature serial data is clocked into the first chip D_{IN} pin, and the next chip D_{IN} pin is connected to the D_{OUT} pin of the first chip. Both chips may share a chip select signal, or the second chip can be enabled separately. When the chip select pin goes low on both chips a double length word is clocked into the first chip. As the first word is clocking into the first chip the second chip is receiving the data that was originally in the shift register of the first chip (invalid data). When a full 16 bits have been clocked into the first chip the next clock cycle begins moving the first frame of the new configuration data into the second chip. With a full 32 clock cycles both chips have valid data and the chip select pin of both chips should be brought high to prevent the data from overshooting. A configure pulse will activate the new configuration on both chips simultaneously, or each chip can be configured separately. The mode, chip select, configure and clock pins of both chips can be tied together and driven from the same sources.

SPECIAL CONTROL PINS

The LMH6580/LMH6581 have two special control pins that function independent of the serial control bus. One of these pins is the reset (RST) pin. The RST pin is active high meaning that at logic 1 level the chip is configured with all outputs disabled and in a high impedance state. The RST pin programs all the registers with input address 0 and all the outputs are turned off. In this configuration the device draws only 11mA. The RST pin can be used as a shutdown function to reduce power consumption. The other special control pin is the broadcast (BCST) pin. The BCST pin is also active high and sets all the outputs to the on state connected to input 0. This is sometimes referred to as broadcast mode, where input 0 is broadcast to all eight outputs.

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THERMAL MANAGEMENT

The LMH6580/LMH6581 are high performance devices that produce a significant amount of heat. With ±5V supplies, the LMH6580/LMH6581 will dissipate approximately 0.5 W of idling power with all outputs enabled. Idling power is calculated based on the typical supply current of 50 mA and a 10V supply voltage. This power dissipation will vary within the range of 0.4 W to 0.6 W due to process variations. In addition, each equivalent video load (150Ω) connected to the outputs should be budgeted 30 mW of power. For a typical application with one video load for each output this would be a total power of 0.62 W. With a θ_{JA} of 44 °C/W this will result in the silicon being 27°C over the ambient temperature. A more aggressive application would be two video loads per output which would result in 0.74 W of power dissipation. This would result in a 33°C temperature rise. For heavier loading, the TQFP package thermal performance can be significantly enhanced with an external heat sink and by providing for moving air ventilation. Also, be sure to calculate the increase in ambient temperature from all devices operating in the system case. Because of the high power output of this device, thermal management should be considered very early in the design process. Generous passive venting and vertical board orientation may avoid the need for fan cooling or heat sinks. Also, the LMH6580/LMH6581 can be operated with a ±3.3V power supply. This will cut power dissipation substantially while only reducing bandwidth by about 10% (2 V_{PP} output). The LMH6580/LMH6581 are fully characterized and factory tested at the ±3.3V power supply condition for applications where reduced power is desired.

PRINTED CIRCUIT LAYOUT

Generally, a good high frequency layout will keep power supply and ground traces away from the input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillations (see Application Note OA-15 for more information). If digital control lines must cross analog signal lines (particularly inputs) it is best if they cross perpendicularly. Texas Instruments suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization:

Device	Package	Evaluation Board Part Number
LMH6580	48–Pin	LMH730164EF

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REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	25

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6580VS/NOPB	ACTIVE	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 85	LMH6580 VS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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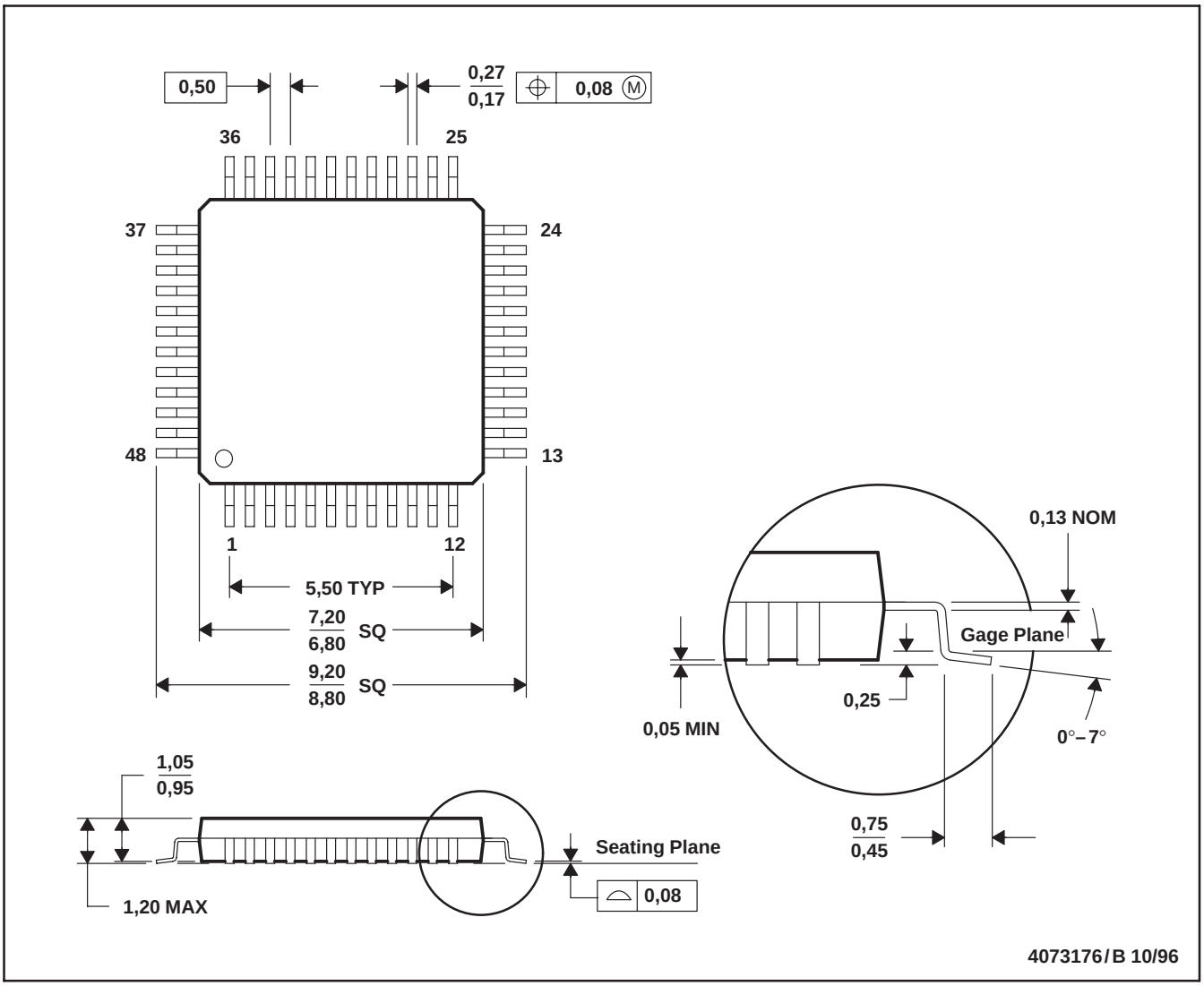
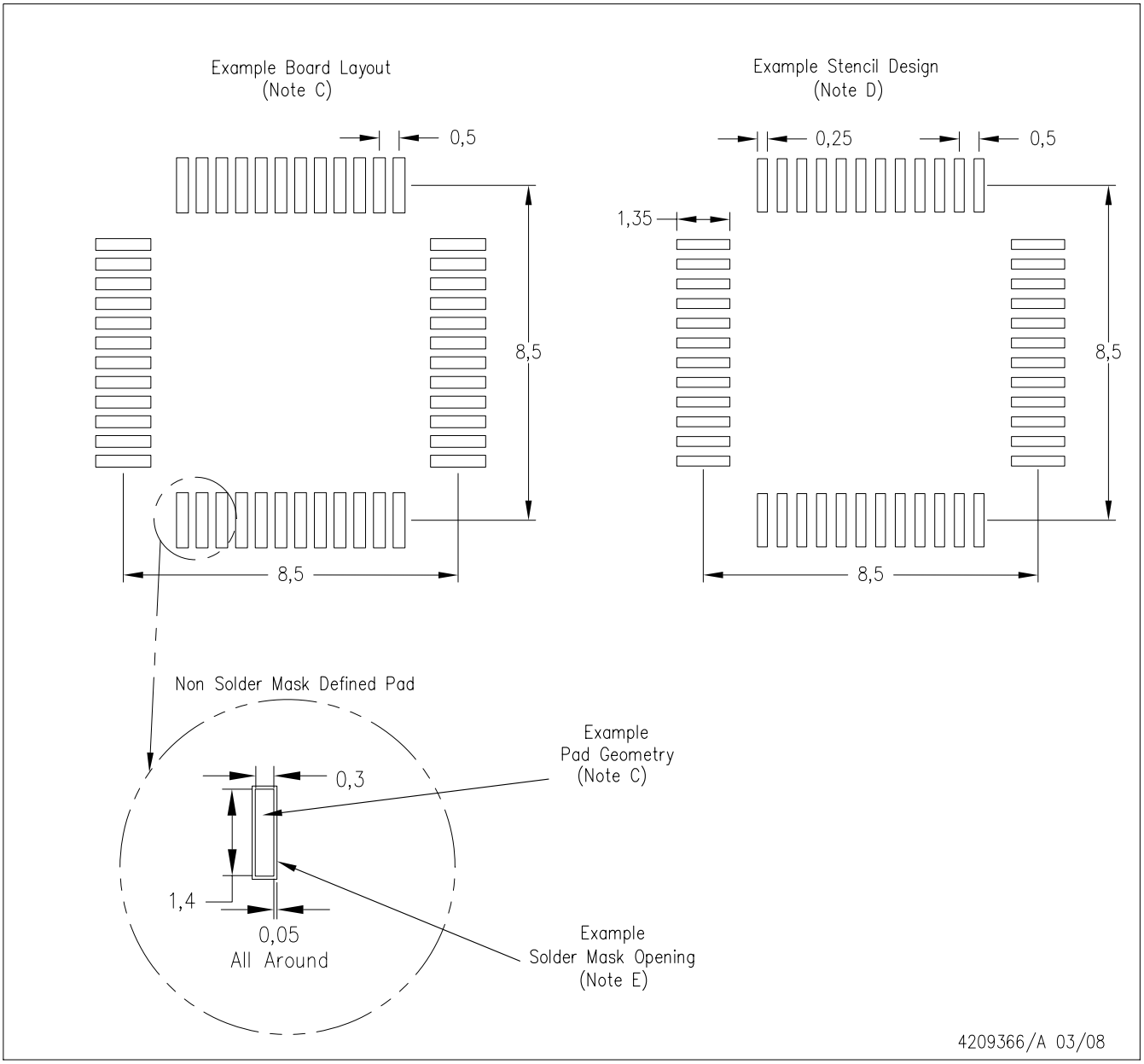
MTQF019A – JANUARY 1995 – REVISED JANUARY 1998

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PFB (S–PQFP–G48)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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