

# NL7SZ57

## Configurable Multifunction Gate

The NL7SZ57 is an advanced high-speed CMOS multifunction gate. The device allows the user to choose logic functions AND, OR, NAND, NOR, XNOR, INVERT and BUFFER. The device has Schmitt-trigger inputs, thereby enhancing noise immunity.

### Features

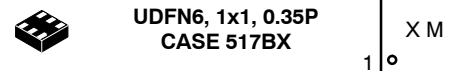
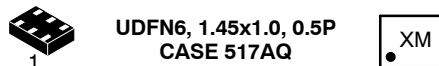
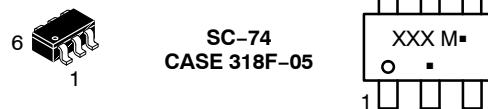
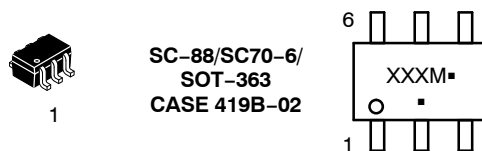
- Designed for 1.65 V to 5.5 V  $V_{CC}$  Operation
- 3.2 ns  $t_{PD}$  at  $V_{CC} = 5$  V (Typ)
- Inputs/Outputs Overvoltage Tolerant up to 5.5 V
- $I_{OFF}$  Supports Partial Power Down Protection
- Sink 24 mA at 3.0 V
- Chip Complexity < 100 FETs
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



ON Semiconductor®

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### MARKING DIAGRAMS



XXX = Specific Device Code

M = Date Code\*

▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation and/or position may vary depending upon manufacturing location.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

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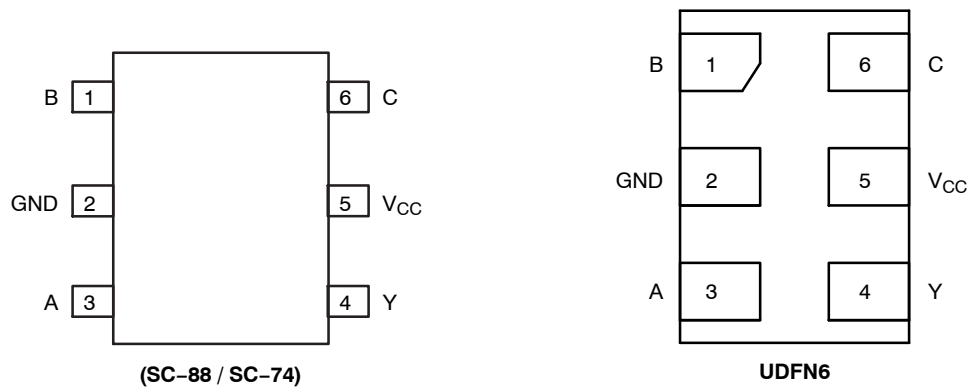


Figure 1. Pinout (Top View)

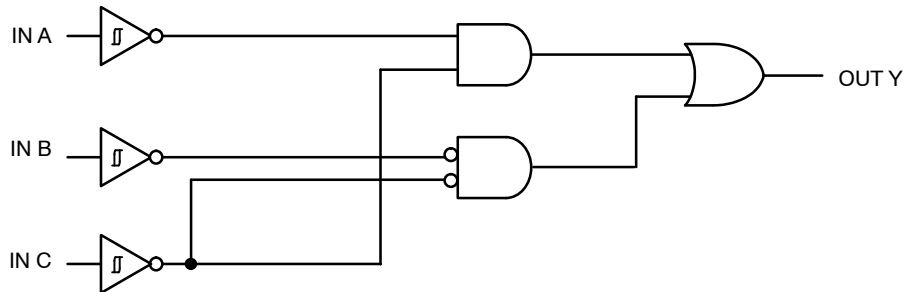


Figure 2. Function Diagram

## PIN ASSIGNMENT

Pin	Function
1	B
2	GND
3	A
4	Y
5	V <sub>CC</sub>
6	C

## FUNCTION TABLE\*

Input			Output
A	B	C	Y
L	L	L	H
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	H

\*To select a logic function, please refer to "Logic Configurations section".

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## LOGIC CONFIGURATIONS

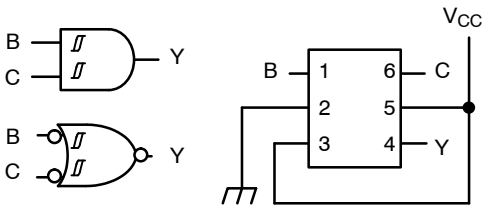


Figure 3. 2-Input AND (When A = "H")

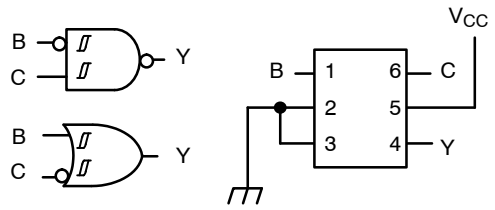


Figure 4. 2-Input NAND with input B inverted (When A = "L")

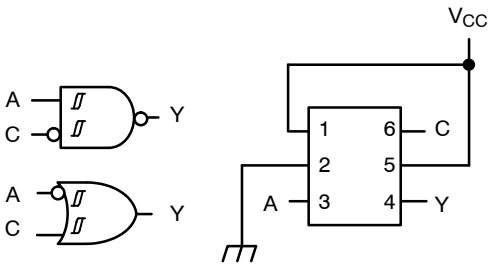


Figure 5. 2-Input NAND with Input C Inverted (When B = "H")

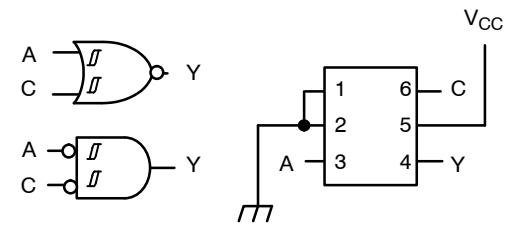


Figure 6. 2-Input NOR (When B = "L")

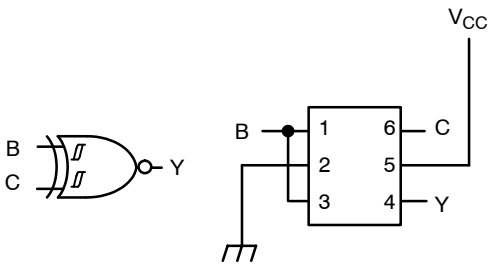


Figure 7. 2-Input XNOR (When A = B)

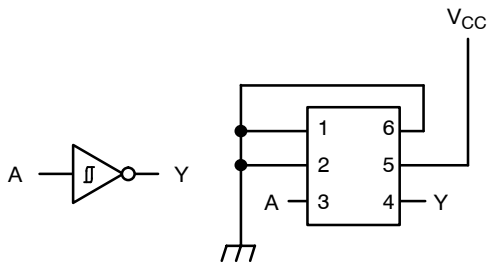


Figure 8. Inverter (When B = C = "L")

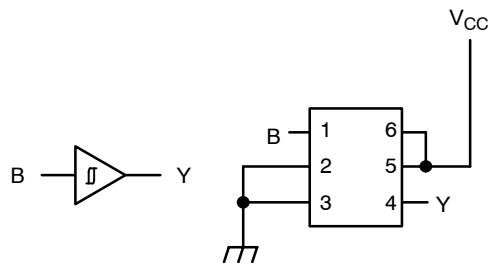


Figure 9. Buffer (When A = "L" and C = "H")

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## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit	
$V_{CC}$	DC Supply Voltage SC-88 (NLV) SC-88, SC-74, UDFN6	-0.5 to +7.0 -0.5 to +6.5	V	
$V_{IN}$	DC Input Voltage SC-88 (NLV) SC-88, SC-74, UDFN6	-0.5 to +7.0 -0.5 to +6.5	V	
$V_{OUT}$	DC Output Voltage SC-88 (NLV) Active-Mode (High or Low State) Tri-State Mode (Note 1) Power-Down Mode ( $V_{CC} = 0$ V)	-0.5 to $V_{CC} + 0.5$ -0.5 to +7.0 -0.5 to +7.0	V	
	DC Output Voltage SC-88, SC-74, UDFN6 Active-Mode (High or Low State) Tri-State Mode (Note 1) Power-Down Mode ( $V_{CC} = 0$ V)	-0.5 to $V_{CC} + 0.5$ -0.5 to +7.0 -0.5 to +7.0	V	
$I_{IK}$	DC Input Diode Current $V_{IN} < GND$	-50	mA	
$I_{OK}$	DC Output Diode Current $V_{OUT} < GND$	-50	mA	
$I_{OUT}$	DC Output Source/Sink Current	$\pm 50$	mA	
$I_{CC}$ or $I_{GND}$	DC Supply Current per Supply Pin or Ground Pin	$\pm 100$	mA	
$T_{STG}$	Storage Temperature Range	-65 to +150	$^{\circ}C$	
$T_L$	Lead Temperature, 1 mm from Case for 10 Secs	260	$^{\circ}C$	
$T_J$	Junction Temperature Under Bias	+150	$^{\circ}C$	
$\theta_{JA}$	Thermal Resistance (Note 2)	SC-88	659	$^{\circ}C/W$
		SC-74	555	
		UDFN6	382	
$P_D$	Power Dissipation in Still Air	SC-88	190	mW
		SC-74	225	
		UDFN6	327	
MSL	Moisture Sensitivity	Level 1		
$F_R$	Flammability Rating Oxygen Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in		
$V_{ESD}$	ESD Withstand Voltage (Note 3) Human Body Mode Charged Device Model (NLV) Charged Device Model	>2000	V	
		>200		
		N/A		
$I_{LATCHUP}$	Latchup Performance (Note 4) (NLV)	$\pm 500$ $\pm 100$	mA	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri-stated.
2. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace no air flow.
3. CDM tested to EIA/JESD22-C101-F. JEDEC recommends that ESD qualification to EIA/JESD22-A115-A (Machine Model) be discontinued per JEDEC/JEP172A.
4. Tested to EIA/JESD78 Class II.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	Positive DC Supply Voltage	1.65	5.5	V
$V_{IN}$	DC Input Voltage	0	5.5	V
$V_{OUT}$	DC Output Voltage Active-Mode (High or Low State) Tri-State Mode (Note 1) Power-Down Mode ( $V_{CC} = 0$ V)	0	5.5	V
$T_A$	Operating Free-Air Temperature	-55	+125	$^{\circ}C$
$t_r, t_f$	Input Rise or Fall Rate $V_{CC} = 1.65$ V to 1.95 V $V_{CC} = 2.3$ V to 2.7 V $V_{CC} = 3.0$ V to 3.6 V $V_{CC} = 4.5$ V to 5.5 V	0	No Limit	nS/V
		0	No Limit	
		0	No Limit	
		0	No Limit	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			-40°C ≤ T <sub>A</sub> ≤ 85°C		-55°C ≤ T <sub>A</sub> ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V <sub>T+</sub>	Positive Input Threshold Voltage		1.65	-	-	1.4	-	1.4	-	1.4	V
			2.3	-	-	1.8	-	1.8	-	1.8	
			3.0	-	-	2.2	-	2.2	-	2.2	
			4.5	-	-	3.1	-	3.1	-	3.1	
			5.5	-	-	3.6	-	3.6	-	3.6	
V <sub>T-</sub>	Negative Input Threshold Voltage		1.65	0.2	-	-	0.2	-	0.2	-	V
			2.3	0.4	-	-	0.4	-	0.4	-	
			3.0	0.6	-	-	0.6	-	0.6	-	
			4.5	1.0	-	-	1.0	-	1.0	-	
			5.5	1.2	-	-	1.2	-	1.2	-	
V <sub>H</sub>	Input Hysteresis Voltage		1.65	0.1	0.48	0.9	0.1	0.9	0.1	-	V
			2.3	0.25	0.75	1.1	0.25	1.1	0.25	-	
			3	0.4	0.93	1.2	0.4	1.2	0.4	-	
			4.5	0.6	1.2	1.5	0.6	1.5	0.6	-	
			5.5	0.7	1.4	1.7	0.7	1.7	0.7	-	
V <sub>OH</sub>	High-Level Output Voltage V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 μA	1.65 to 5.5	V <sub>CC</sub> - 0.1	V <sub>CC</sub>	-	V <sub>CC</sub> - 0.1	-	V <sub>CC</sub> - 0.1	-	V
		I <sub>OH</sub> = -4 mA	1.65	1.20	1.52	-	1.20	-	1.20	-	
		I <sub>OH</sub> = -8 mA	2.3	1.9	2.1	-	1.9	-	1.9	-	
		I <sub>OH</sub> = -16 mA	3	2.4	2.7	-	2.4	-	2.4	-	
		I <sub>OH</sub> = -24 mA	3	2.3	2.5	-	2.3	-	2.3	-	
		I <sub>OH</sub> = -32 mA	4.5	3.8	4	-	3.8	-	3.8	-	
V <sub>OL</sub>	Low-Level Output Voltage V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 100 μA	1.65 to 5.5	-	-	0.1	-	0.1	-	0.1	V
		I <sub>OL</sub> = 4 mA	1.65	-	0.08	0.45	-	0.45	-	0.45	
		I <sub>OL</sub> = 8 mA	2.3	-	0.2	0.3	-	0.3	-	0.4	
		I <sub>OL</sub> = 16 mA	3	-	0.28	0.4	-	0.4	-	0.5	
		I <sub>OL</sub> = 24 mA	3	-	0.38	0.55	-	0.55	-	0.55	
		I <sub>OL</sub> = 32 mA	4.5	-	0.42	0.55	-	0.55	-	0.65	
I <sub>IN</sub>	Input Leakage Current	V <sub>IN</sub> = 5.5 V or GND	1.65 to 5.5	-	-	+0.1	-	+1.0	-	+1.0	μA
I <sub>OFF</sub>	Power Off Leakage Current	V <sub>IN</sub> = 5.5 V or V <sub>OUT</sub> = 5.5 V	0	-	-	1.0	-	10	-	10	μA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>IN</sub> = 5.5 V or GND	5.5	-	-	1.0	-	10	-	10	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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## AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	Condition	$V_{CC}$ (V)	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$		$-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		Unit
				Min	Typ	Max	Min	Max	Min	Max	
$t_{PLH}$ , $t_{PHL}$	Propagation Delay (Figures 10 and 11)	$R_L = 1\text{ k}\Omega$ , $C_L = 30\text{ pF}$	1.65 to 1.95	-	8.6	14.4	-	14.4	-	14.4	ns
		$R_L = 500\ \Omega$ , $C_L = 30\text{ pF}$	2.3 to 2.7	-	5.1	8.3	-	8.3	-	8.3	
		$R_L = 500\ \Omega$ , $C_L = 50\text{ pF}$	3.0 to 3.6	-	3.9	6.3	-	6.3	-	6.3	
			4.5 to 5.5	-	3.3	5.1	-	5.1	-	5.1	

## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
$C_{IN}$	Input Capacitance	$V_{CC} = 5.5\text{ V}$ , $V_{IN} = 0\text{ V}$ or $V_{CC}$	2.5	pF
$C_{OUT}$	Output Capacitance	$V_{CC} = 5.5\text{ V}$ , $V_{IN} = 0\text{ V}$ or $V_{CC}$	4.0	pF
$C_{PD}$	Power Dissipation Capacitance (Note 5)	10 MHz, $V_{CC} = 3.3\text{ V}$ , $V_{IN} = 0\text{ V}$ or $V_{CC}$ 10 MHz, $V_{CC} = 5.0\text{ V}$ , $V_{IN} = 0\text{ V}$ or $V_{CC}$	16 19.5	pF

5.  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:  $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$ .  $C_{PD}$  is used to determine the no-load dynamic power consumption;  $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$ .

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$C_L$  includes probe and jig capacitance  
 $R_T$  is  $Z_{OUT}$  of pulse generator (typically 50  $\Omega$ )  
 $f = 1$  MHz

**Figure 10. Test Circuit**

Test	Switch Position	$C_L$ , pF	$R_L$ , $\Omega$	$R_1$ , $\Omega$
$t_{PLH} / t_{PHL}$	Open	See AC Characteristics Table		
$t_{PLZ} / t_{PZL}$	$2 \times V_{CC}$	50	500	500
$t_{PHZ} / t_{PZH}$	GND	50	500	500

X = Don't Care



**Figure 11. Switching Waveforms**

$V_{CC}$ , V	$V_{mi}$ , V	$V_{mo}$ , V		$V_Y$ , V
		$t_{PLH}, t_{PHL}$	$t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}$	
1.65 to 1.95	$V_{CC} / 2$	$(V_{OH} - V_{OL}) / 2$	$V_{CC} / 2$	0.15
2.3 to 2.7	$V_{CC} / 2$	$(V_{OH} - V_{OL}) / 2$	$V_{CC} / 2$	0.15
3.0 to 3.6	$V_{CC} / 2$	$(V_{OH} - V_{OL}) / 2$	$V_{CC} / 2$	0.3
4.5 to 5.5	$V_{CC} / 2$	$(V_{OH} - V_{OL}) / 2$	$V_{CC} / 2$	0.3

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## ORDERING INFORMATION

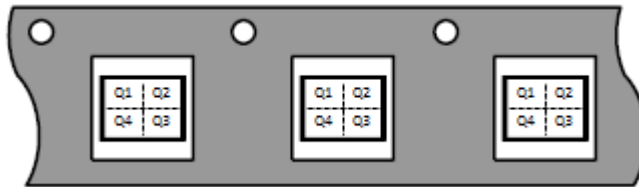
Device	Package			Shipping <sup>†</sup>
NL7SZ57DFT2G	SC-88 (Pb-Free)	MN	Q4	3000 / Tape & Reel
NLV7SZ57DFT2G*	SC-88 (Pb-Free)	MN	Q4	3000 / Tape & Reel
NL7SZ57DBVT1G	SC-74 (Pb-Free)	AL	Q4	3000 / Tape & Reel
NL7SZ57MU1TCG (In Development)	UDFN6, 1.45 x 1.0 x 0.35P (Pb-Free)	TBD	Q4	3000 / Tape & Reel
NL7SZ57MU3TCG (In Development)	UDFN6, 1.0 x 1.0 x 0.35P (Pb-Free)	TBD	Q4	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

### Pin 1 Orientation in Tape and Reel

Direction of Feed





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## PACKAGE DIMENSIONS

SC-88/SC70-6/SOT-363  
CASE 419B-02  
ISSUE Y

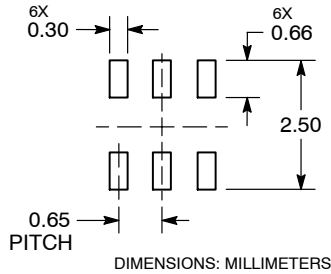


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.043
A1	0.00	---	0.10	0.000	---	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

**RECOMMENDED SOLDERING FOOTPRINT\***

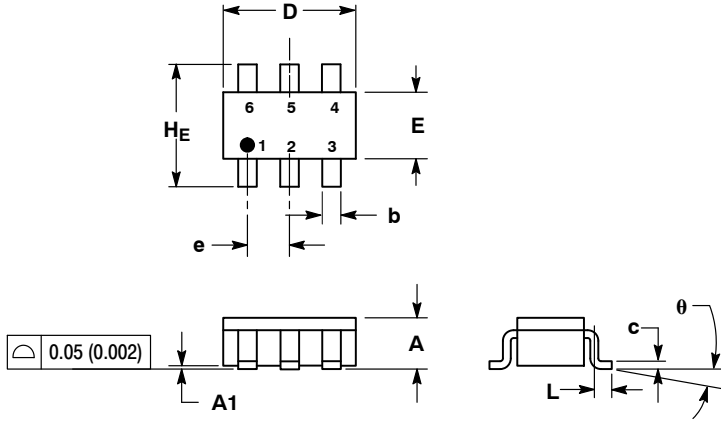


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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## PACKAGE DIMENSIONS

SC-74  
CASE 318F-05  
ISSUE N

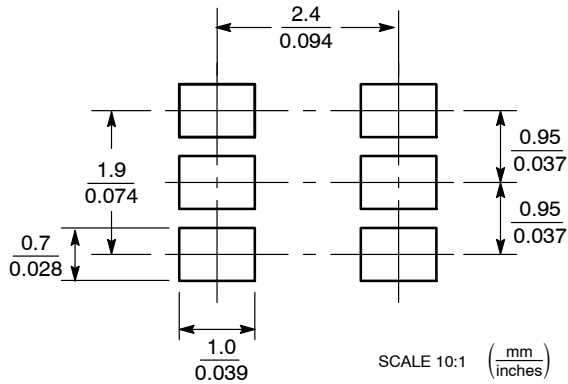


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318F-01, -02, -03, -04 OBSOLETE. NEW STANDARD 318F-05.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.37	0.50	0.010	0.015	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.95	0.95	1.05	0.037	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
HE	2.50	2.75	3.00	0.099	0.108	0.118
θ						

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLE 1:

- PIN 1. CATHODE
- 2. ANODE
- 3. CATHODE
- 4. CATHODE
- 5. ANODE
- 6. CATHODE

STYLE 2:

- PIN 1. NO CONNECTION
- 2. COLLECTOR
- 3. EMITTER
- 4. NO CONNECTION
- 5. COLLECTOR
- 6. BASE

STYLE 3:

- PIN 1. EMITTER 1
- 2. BASE 1
- 3. COLLECTOR 2
- 4. EMITTER 2
- 5. BASE 2
- 6. COLLECTOR 1

STYLE 4:

- PIN 1. COLLECTOR 2
- 2. EMITTER 1/EMITTER 2
- 3. COLLECTOR 1
- 4. EMITTER 3
- 5. BASE 1/BASE 2/COLLECTOR 3
- 6. BASE 3

STYLE 5:

- PIN 1. CHANNEL 1
- 2. ANODE
- 3. CHANNEL 2
- 4. CHANNEL 3
- 5. CATHODE
- 6. CHANNEL 4

STYLE 6:

- PIN 1. CATHODE
- 2. ANODE
- 3. CATHODE
- 4. CATHODE
- 5. CATHODE
- 6. CATHODE

STYLE 7:

- PIN 1. SOURCE 1
- 2. GATE 1
- 3. DRAIN 2
- 4. SOURCE 2
- 5. GATE 2
- 6. DRAIN 1

STYLE 8:

- PIN 1. EMITTER 1
- 2. BASE 2
- 3. COLLECTOR 2
- 4. EMITTER 2
- 5. BASE 1
- 6. COLLECTOR 1

STYLE 9:

- PIN 1. EMITTER 2
- 2. BASE 2
- 3. COLLECTOR 1
- 4. EMITTER 1
- 5. BASE 1
- 6. COLLECTOR 2

STYLE 10:

- PIN 1. ANODE/CATHODE
- 2. BASE
- 3. EMITTER
- 4. COLLECTOR
- 5. ANODE
- 6. CATHODE

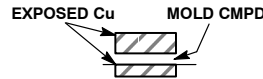
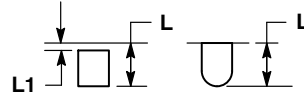
STYLE 11:

- PIN 1. EMITTER
- 2. BASE
- 3. ANODE/CATHODE
- 4. ANODE
- 5. CATHODE
- 6. COLLECTOR

# NL7SZ57

## PACKAGE DIMENSIONS

UDFN6, 1.45x1.0, 0.5P  
CASE 517AQ  
ISSUE O



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A2	0.07	REF
b	0.20	0.30
D	1.45	BSC
E	1.00	BSC
e	0.50	BSC
L	0.30	0.40
L1	---	0.15



### MOUNTING FOOTPRINT



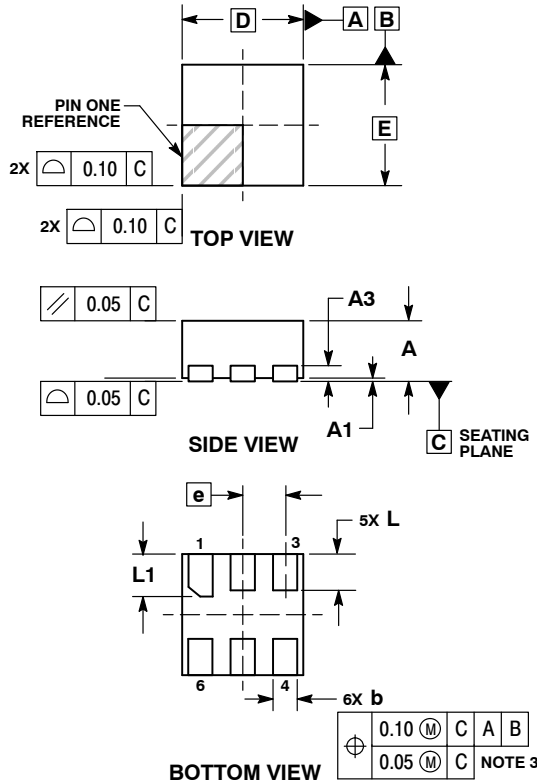
DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NL7SZ57

## PACKAGE DIMENSIONS

UDFN6, 1x1, 0.35P  
CASE 517BX  
ISSUE O

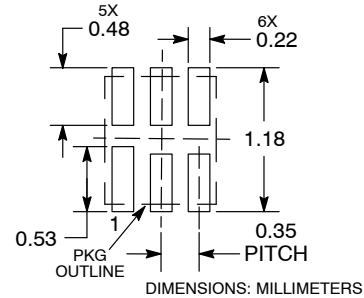


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13	REF
b	0.12	0.22
D	1.00	BSC
E	1.00	BSC
e	0.35	BSC
L	0.25	0.35
L1	0.30	0.40

**RECOMMENDED SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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