NCP5500, NCV5500, NCP5501, NCV5501

LDO Voltage Regulator

500 mA

These linear low drop voltage regulators provide up to 500 mA over a user−adjustable output range of 1.25 V to 5.0 V, or at a fixed output voltage of 1.5 V, 3.3 V or 5.0 V, with typical output voltage accuracy better than 3%. An internal PNP pass transistor permits low dropout voltage and operation at full load current at the minimum input voltage. NCV versions are qualified for demanding automotive applications that require extended temperature operation and site and change control. NCP5500 and NCV5500 versions include an Enable/Shutdown function and are available in a DPAK 5 and SOIC 8 packages. NCP5501 and NCV5501 versions are available in DPAK 3 for applications that do not require logical on/off control.

This regulator family is ideal for applications that require a broad input voltage range, and low dropout performance up to 500 mA load using low cost ceramic capacitors. Integral protection features include short circuit current and thermal shutdown.

Features

- Output Current up to 500 mA
- 2.9% Output Voltage Accuracy
- Low Dropout Voltage (230 mV at 500 mA)
- Enable Control Pin (NCP5500 / NCV5500)
- Reverse Bias Protection
- Short Circuit Protection
- Thermal Shutdown
- Wide Operating Temperature Range
  NCV5500 / NCV5501; −40°C to +125°C Ambient Temperature
  NCP5500 / NCP5501; −40°C to +85°C Ambient Temperature
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- Stable with Low Cost Ceramic Capacitors
- These are Pb−Free Devices

Typical Applications

- Automotive
- Industrial and Consumer
- Post SMPS Regulation
- Point of Use Regulation

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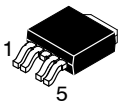
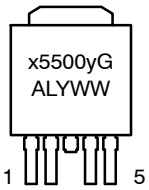
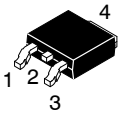
MARKING DIAGRAMS



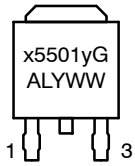
DPAK 5
CENTER LEAD CROP
CASE 175AA



Pin 1. EN
2. V_{in}
TAB, 3. GND
4. V_{out}
5. NC/ADJ



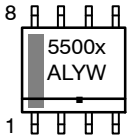
DPAK 3
SINGLE GAUGE
CASE 369C



Pin 1. V_{in}
TAB, 2. GND
3. V_{out}

x = P (NCP), V (NCV)
5500/1 = Device Code
y = Output Voltage
L = 1.5 V
T = 3.3 V
U = 5.0 V
W = Adjustable
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

SOIC−8
CASE 751

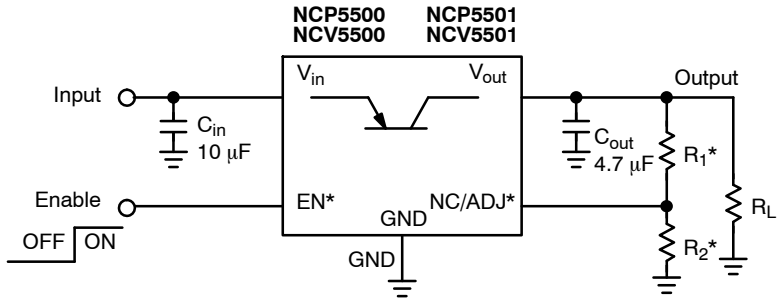


Pin 1. V_{in}
2. GND
3. GND
4. V_{out}
5. NC/ADJ
6. GND
7. GND
8. EN

x = Output Voltage, NCP/NCV
A = Adjustable, NCV
B = Adjustable, NCP
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

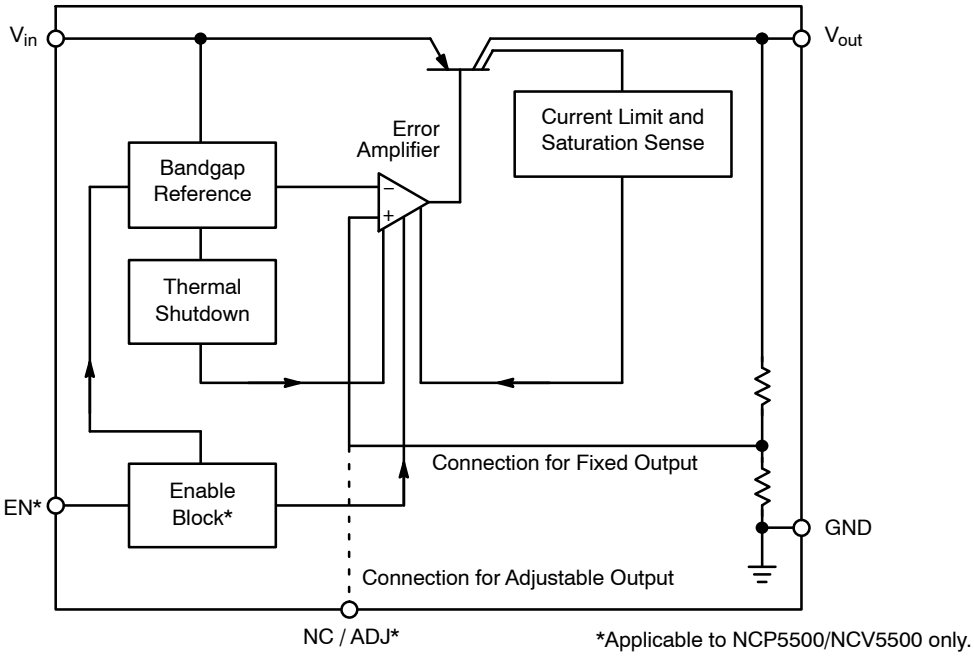


*Applicable to NCP5500/NCV5500 only.

Figure 1. Typical Application Circuit

PIN FUNCTION DESCRIPTIONS

DPAK 3	DPAK 5	SOIC−8	Pin Name	Description
Pin No.	Pin No.	Pin No.		
–	1	8	EN	Enable. This pin allows for on/off control of the regulator. High level turns on the output. To disable the device, connect to ground. If this function is not in use, connect to V_{in}.
1	2	1	V_{in}	Positive power supply input voltage.
2, Tab	3, Tab	2, 3, 6, 7	GND	Ground. This pin is internally connected to the Tab heat sink.
3	4	4	V_{out}	Regulated output voltage.
–	5	5	NC/ADJ	No connection (Fixed output versions). Voltage−adjust input (Adjustable output version). Use an external voltage divider to set the output voltage over a range of 1.25 V to 5.0 V.



*Applicable to NCP5500/NCV5500 only.

Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Input Voltage (Note 1)	V_{in}	−0.3 (Note 2)	+18	V
Output, Enable Voltage	V_{out}, EN	−0.3	+16 or V_{in} + 0.3 (Notes 2 and 5)	V
Maximum Junction Temperature	T_J	−	150	°C
Storage Temperature	T_{Stg}	−55	+150	°C
Moisture Sensitivity Level All Packages	MSL	1		−
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 3)	T_{sld}		265 Peak	°C
ESD Capability, Human Body Model (Note 4)	ESD_{HBM}	4000	−	V
ESD Capability, Machine Model (Note 4)	ESD_{MM}	200	−	V
ESD Capability, Charged Device Model (Note 4)	ESD_{CDM}	1000	−	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*Latchup Current Maximum Rating: ≤ 100 mA per JEDEC standard: JESD78.

1. Refer to Electrical Characteristics and Application Information for Safe Operating Area.
2. Reverse bias protection feature valid only if $V_{out} - V_{in} \leq 7$ V.
3. Pb−Free, 60 sec −150 sec above 217°C, 40 sec max at peak temperature
4. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   ESD Charged Device Model tested per EIA/JES D22/C101, Field Induced Charge Model
5. Maximum = +16 V or (V_{in} + 0.3 V), whichever is lower.

THERMAL CHARACTERISTICS

Rating	Symbol	Min	Max	Unit
Package Dissipation	P_D		Internally Limited	W
Thermal Characteristics, DPAK 3 and DPAK 5 (Note 1)				°C/W
Thermal Resistance, Junction−to−Air (Note 6)	$R_{\theta JA}$		60	
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$		5.2	
Thermal Characteristics, SOIC−8 (Note 1)				°C/W
Thermal Resistance, Junction−to−Air (Note 6)	$R_{\theta JA}$		80	
Thermal Reference, Junction−to−Lead	$R_{\Psi JL}$		22	

6. As measured using a copper heat spreading area of 650 mm^2, 1 oz copper thickness.

OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Operating Input Voltage (Note 1)	V_{in}	V_{out} + V_{DO}, 2.5 V (Note 7)	16	V
Adjustable Output Voltage Range (Adjustable Version Only)	V_{out}	1.25	5.0	V
Operating Ambient Temperature Range	T_A			°C
NCP5500, NCP5501		−40	85	
NCV5500, NCV5501		−40	125	

7. Minimum V_{in} = 2.5 V or (V_{out} + V_{DO}), whichever is higher.

ELECTRICAL CHARACTERISTICS V_{in} = 2.5 V or V_{out} + 1.0 V (whichever is higher), C_{in} = 10 μF, C_{out} = 4.7 μF, for typical values T_A = 25°C, for min/max values T_A = −40°C to 85°C (NCP Version), T_A = −40°C to 125°C (NCV Version) unless otherwise noted (Note 13).

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
OUTPUT						
Output Voltage (Note 14) 5 V Regulator 3.3 V Regulator 1.5 V Regulator ADJ Regulator	V_{out}	T_A = 25°C, I_{out} = 50 mA		V_{NOM}±2.9%		 V V V
Output Voltage (Note 8) 5 V Regulator 3.3 V Regulator 1.5 V Regulator ADJ Regulator	V_{out}	1.0 mA < I_{out} < 500 mA	(−4.9%) 4.755 3.138 1.427 1.189	V_{NOM} 5.0 3.3 1.5 1.25	(+4.9%) 5.245 3.462 1.574 1.311	 V V V
Line Regulation	REG_{LINE}	I_{out} = 50 mA 2.5 V or (V_{out} + 1.0 V) < V_{in} < 16 V	−1.0	0.1	1.0	%
Load Regulation	REG_{LOAD}	1.0 mA < I_{out} < 500 mA	−1.0	0.35	1.0	%
Dropout Voltage (Note 9) 5.0 V Version 3.3 V Version 1.5 V Version (Note 10) Adjustable Version (Note 11)	V_{DO}	 I_{out} = 1.0 mA, ΔV_{out} = −2% I_{out} = 500 mA, ΔV_{out} = −2% I_{out} = 1.0 mA, ΔV_{out} = −2% I_{out} = 500 mA, ΔV_{out} = −2% I_{out} = 1.0 mA, ΔV_{out} = −2% I_{out} = 500 mA, ΔV_{out} = −2% I_{out} = 1.0 mA, ΔV_{out} = −2% I_{out} = 500 mA, ΔV_{out} = −2%	 – – – – – – – –	 5 230 5 230 – – 5 230	 90 700 90 700 1073 1073 90 700	mV
Ground Current	I_{GND}	I_{out} = 100 μA I_{out} = 500 mA		300 10	500 20	μA mA
Disable Current in Shutdown (NCP5500, NCV5500)	I_{SD}	Adjustable and 1.5 V versions All other versions		30 40	50 50	μA
Current Limit	$I_{out(LIM)}$	V_{out} = 90% of $V_{out(nom)}$	500	700	900	mA
Ripple Rejection Ratio (Notes 9 & 14)	RR	120 Hz I_{out} = 100 mA, 1 kHz 10 kHz	– – –	75 75 70	– – –	dB
Output Noise Voltage (Notes 12 & 14)	V_n	f = 10 Hz to 100 kHz, V_{in} = 2.5 V V_{out} = 1.25 V, I_{out} = 1.0 mA f = 10 Hz to 100 kHz, V_{in} = 2.5 V V_{out} = 1.25 V, I_{out} = 100 mA		 18 35		μVrms
ENABLE (NCP5500, NCV5500 Only)						
Enable Voltage	V_{ENoff} V_{ENon}	OFF (shutdown) State ON (enabled) State	 2.0		0.4	V
Enable Pin Bias Current	I_{EN}	V_{EN} = V_{in}, I_{out} = 1.0 mA		–	1.0	μA
ADJUST						
Adjust Pin Current (Note 14)	I_{ADJ}	V_{EN} = V_{in}, V_{ADJ} = 1.25 V, V_{out} = 1.25 V		–	60	nA
THERMAL SHUTDOWN						
Thermal Shutdown Temperature (Note 14)	TSD	I_{out} = 100 μA	150	–	210	°C

8. Deviation from nominal. For adjustable versions, Pin ADJ connected to V_{out}.
9. See Typical Characteristics section for additional information.
10. V_{DO} is constrained by the minimum input voltage of 2.5 V.
11. V_{out} is set by external resistor divider to 5 V.
12. V_n for other fixed voltage versions, as well as adjustable versions set to other output voltages, can be calculated from the following formula: $V_n = V_{n(x)} * V_{out} / 1.25$, where $V_{n(x)}$ is the typical value from the table above.
13. Performance guaranteed over specified operating conditions by design, guard banded test limits, and/or characterization, production tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
14. Values are based on design and/or characterization.

TYPICAL CHARACTERISTICS

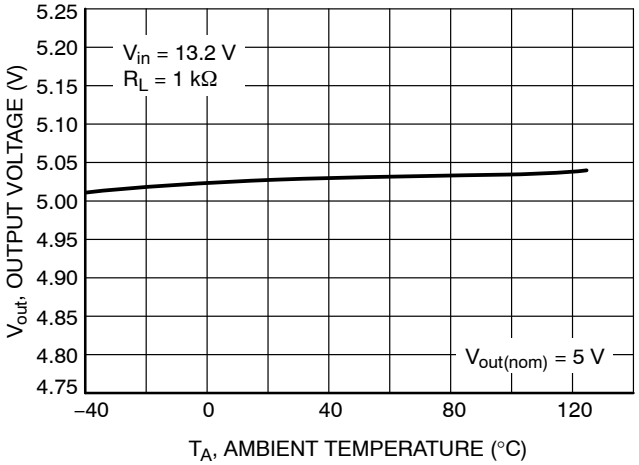


Figure 3. Output Voltage vs. Ambient Temperature

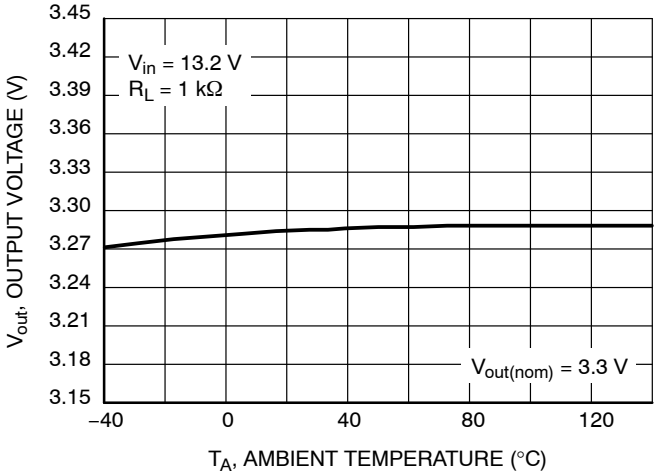


Figure 4. Output Voltage vs. Ambient Temperature

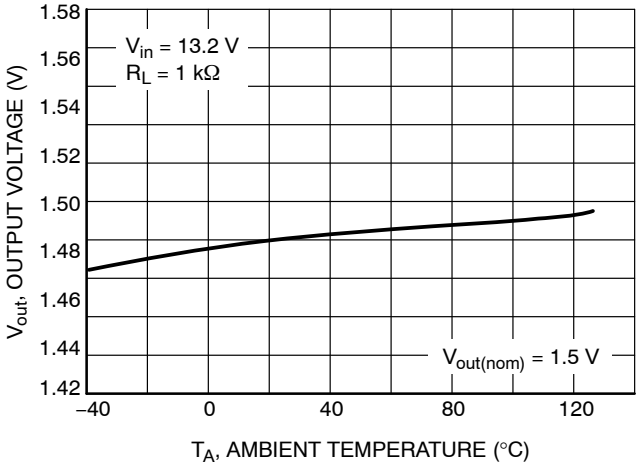


Figure 5. Output Voltage vs. Ambient Temperature

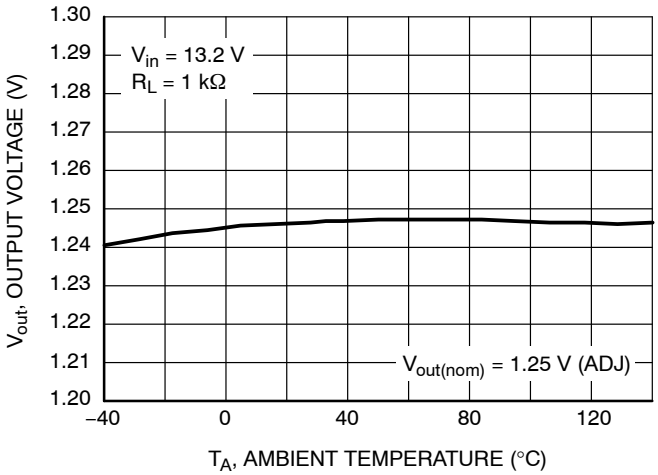


Figure 6. Output Voltage vs. Ambient Temperature

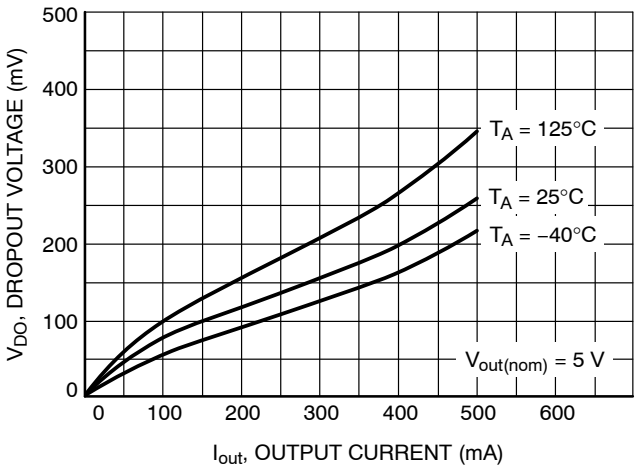


Figure 7. Dropout Voltage vs. Output Current

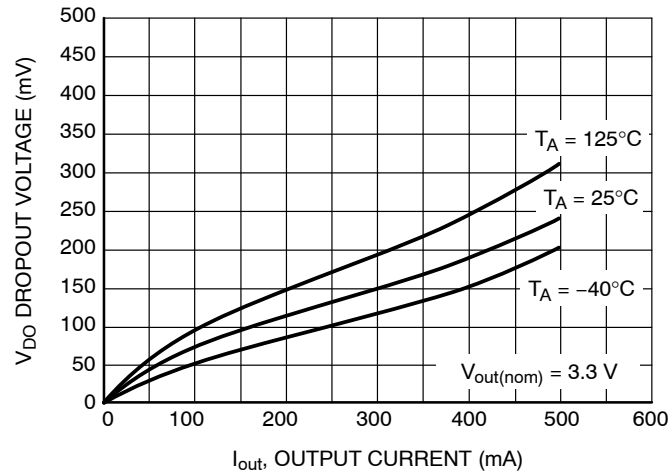


Figure 8. Dropout Voltage vs. Output Current

TYPICAL CHARACTERISTICS

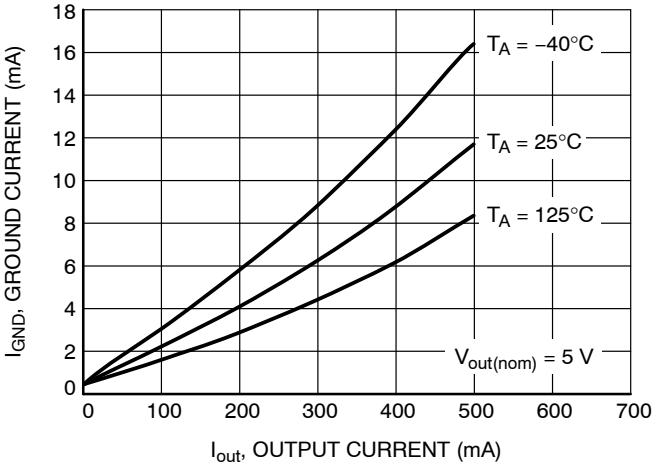


Figure 9. Ground Current vs. Output Current

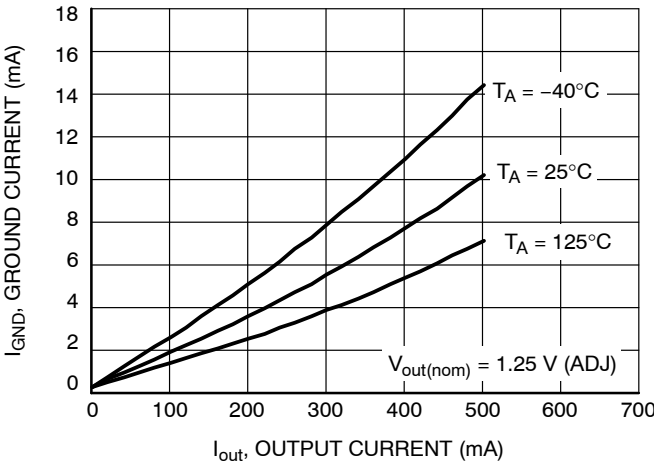


Figure 10. Ground Current vs. Output Current

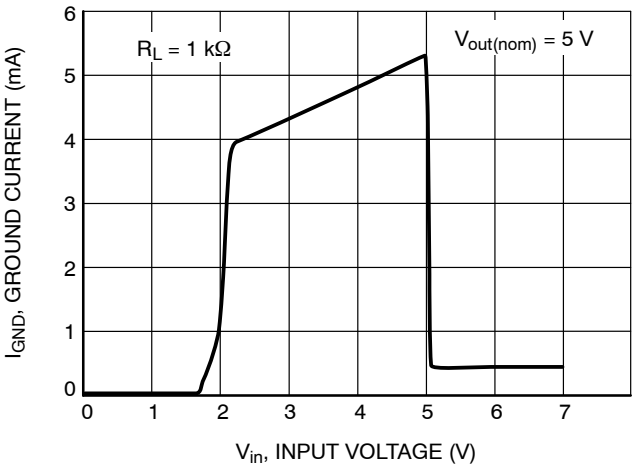


Figure 11. Ground Current vs. Input Voltage

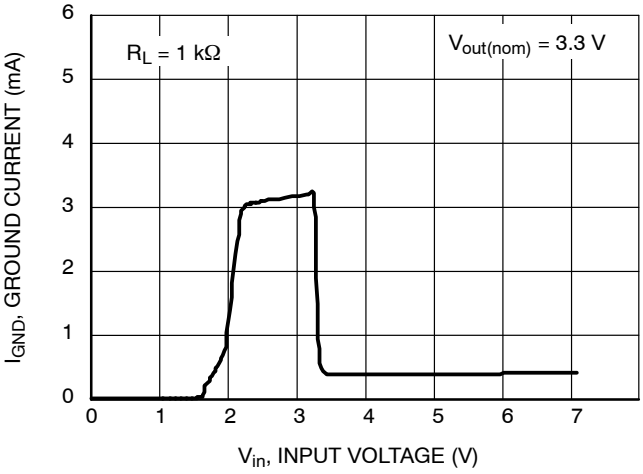


Figure 12. Ground Current vs. Input Voltage

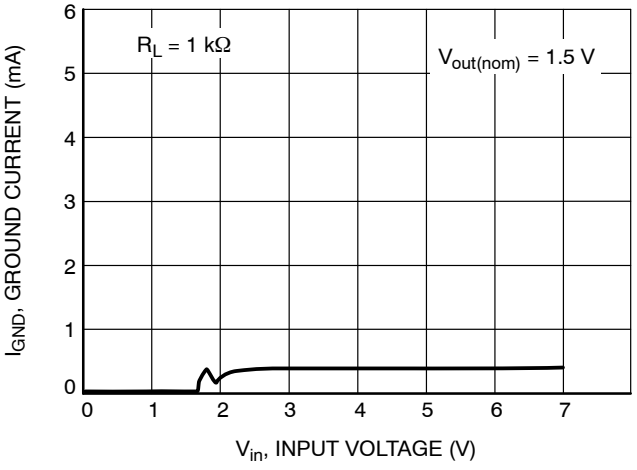


Figure 13. Ground Current vs. Input Voltage

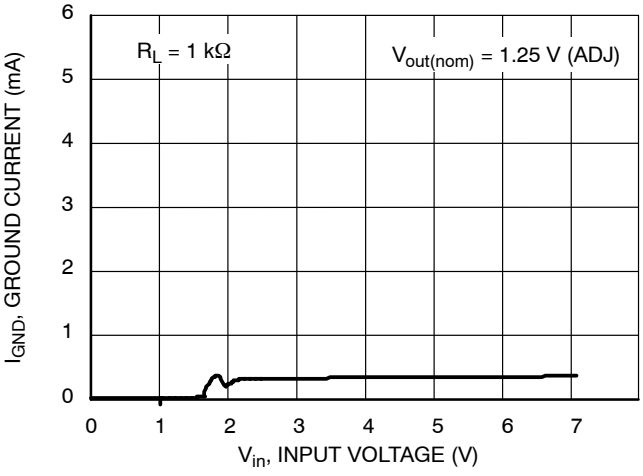


Figure 14. Ground Current vs. Input Voltage

TYPICAL CHARACTERISTICS

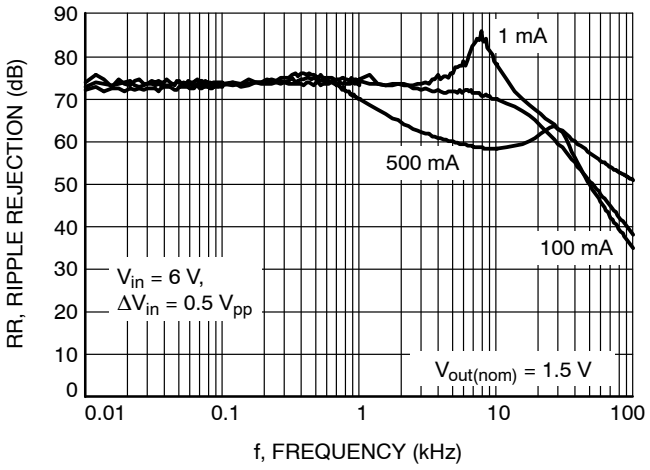


Figure 15. Ripple Rejection vs. Frequency

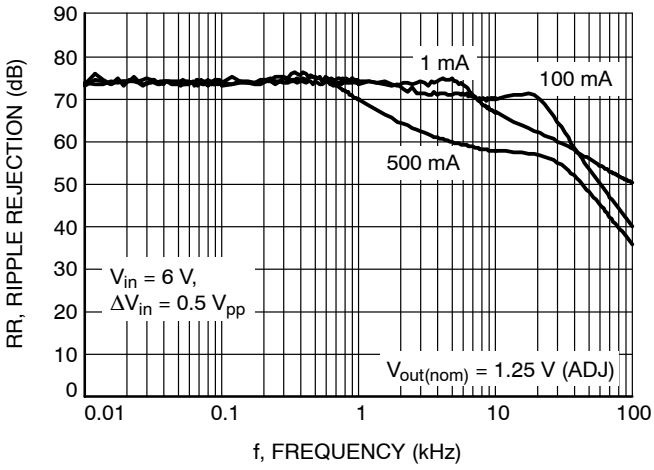


Figure 16. Ripple Rejection vs. Frequency

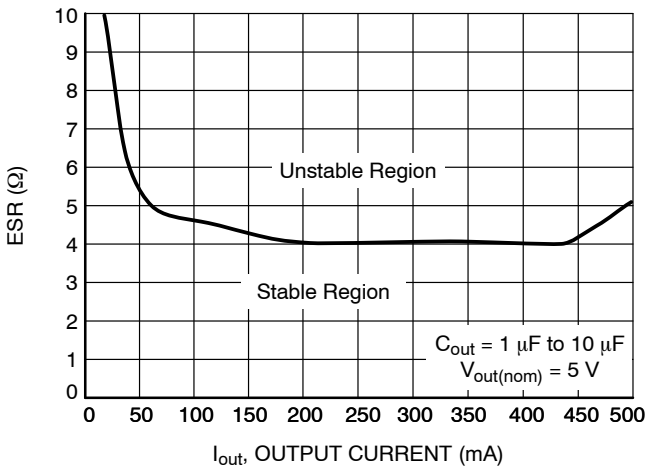


Figure 17. Output Capacitor ESR Stability vs. Output Current

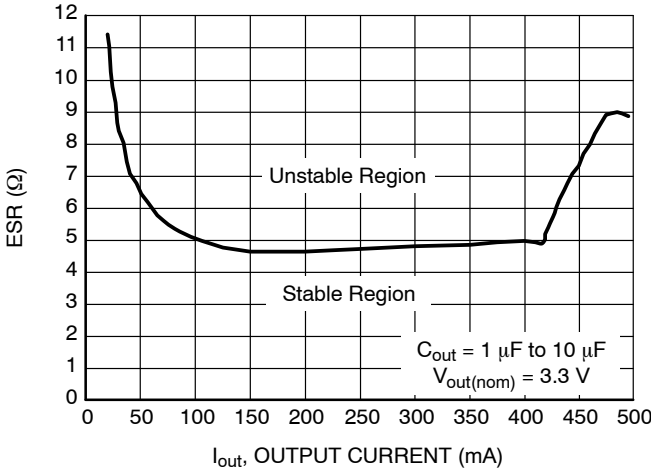


Figure 18. Output Capacitor ESR Stability vs. Output Current

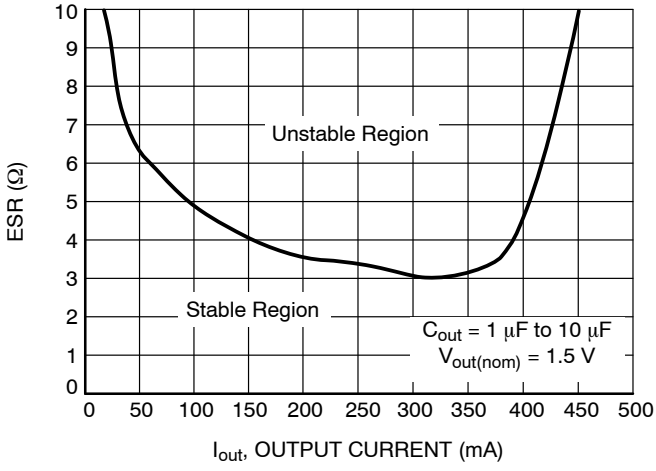


Figure 19. Output Capacitor ESR Stability vs. Output Current

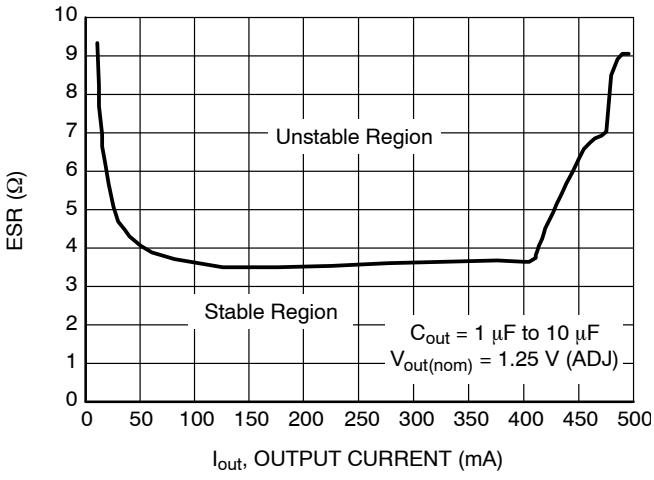


Figure 20. Output Capacitor ESR Stability vs. Output Current

NOTE: Typical characteristics were measured with the same conditions as electrical characteristics, unless otherwise noted.

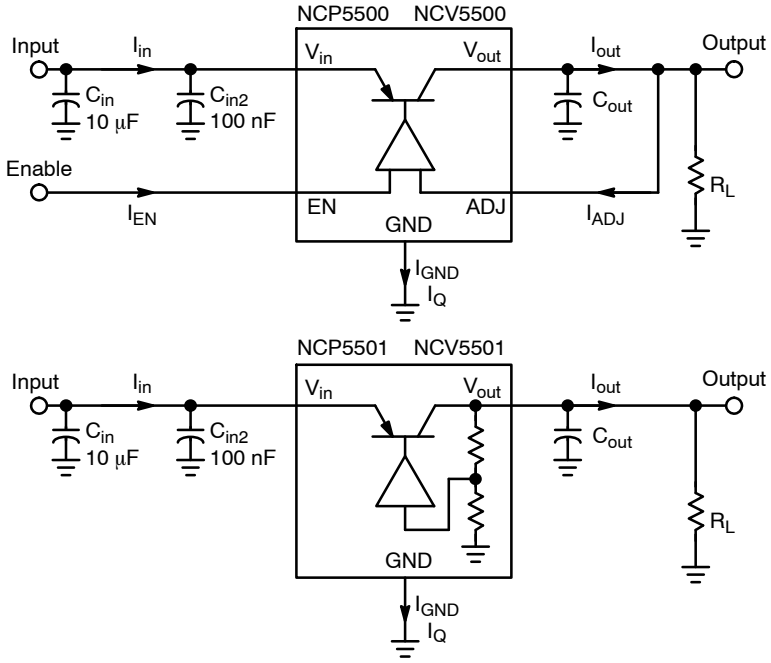


Figure 21. Measuring Circuits

Circuit Description

The NCP5500/NCP5501/NCV5500/NCV5501 are integrated linear regulators with a DC load current capability of 500 mA. The output voltage is regulated by a PNP pass transistor controlled by an error amplifier and band gap reference. The choice of a PNP pass element provides the lowest possible dropout voltage, particularly at reduced load currents. Pass transistor base drive current is controlled to prevent oversaturation. The regulator is internally protected by both current limit and thermal shutdown. Thermal shutdown occurs when the junction temperature exceeds 150°C. The NCV5500 includes an enable/shutdown pin to turn off the regulator to a low current drain standby state.

Regulator

The error amplifier compares the reference voltage to a sample of the output voltage (V_{out}) and drives the base of a PNP series pass transistor via a buffer. The reference is a bandgap design for enhanced temperature stability. Saturation control of the PNP pass transistor is a function of the load current and input voltage. Oversaturation of the output power device is prevented, and quiescent current in the ground pin is minimized.

Regulator Stability Considerations

The input capacitor is necessary to stabilize the input impedance to reduce transient line influences. The output capacitor helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability. The capacitor value and type should be based on cost, availability, size and temperature constraints. Refer to Typical Operating Characteristics for stability regions.

Enable Input (NCP5500, NCV5500)

The enable pin is used to turn the regulator on or off. By holding the pin at a voltage less than 0.4 V, the output of the regulator will be turned off to a minimal current drain state. When the voltage at the Enable pin is greater than 2.0 V, the output of the regulator will be enabled and rise to the regulated output voltage. The Enable pin may be connected directly to the input pin to provide a constant enable to the regulator.

Active Load Protection in Shutdown (NCP5500, NCV5500)

When a linear regulator is disabled (shutdown), the output (load) voltage should be zero. However, stray PC board leakage paths, output capacitor dielectric absorption, and inductively coupled power sources can cause an undesirable regulator output voltage if load current is low or zero. The NCV5500 features a load protection network that is active only during Shutdown mode. This network switches in a shunt current path (~500 μA) from V_{out} to Ground. This feature also provides a controlled (“soft”) discharge path for the output capacitor after a transition from Enable to Shutdown.

Calculating Resistors for the ADJ Versions

The adjustable version uses feedback resistors to adjust the output to the desired output voltage. With V_{out} connected to ADJ, the adjustable version will regulate at 1.25 V ±4.9% (1250 ± 61.25 mV).

Output voltage formula with an external resistor divider:

$$V_{out} = \left(1.25\ V - \left[60E{-}9 \cdot \frac{(R_1 \cdot R_2)}{(R_1 + R_2)}\right]\right) \cdot \left(\frac{(R_1 + R_2)}{R_2}\right)$$

Where

R_1 = value of the divider resistor connected between V_{out} and ADJ,

R_2 = value of the divider resistor connected between ADJ and GND,

The term "1.25 V" has a tolerance of ±4.9%; the term "60E−9" can vary in the range 15E−9 to 60E−9.

For values of R_2 less than 15 KΩ, the term within brackets ([ ]) will evaluate to less than 1 mV and can be ignored. This simplifies the output voltage formula to:

V_{out} = 1.25 V * ((R1 + R2) / R2)) with a tolerance of ±4.9%, which is the tolerance of the 1.25 V output when delivering up to 500 mA of output current.

DEFINITION OF TERMS

Dropout Voltage: The input−to−output voltage differential at which the circuit ceases to regulate against further reduction input voltage. Measured when the output voltage has dropped 2% relative to the value measured at nominal input voltage. Dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature. Pulse loading techniques are employed such that the average chip temperature is not significantly affected.

Quiescent and Ground Current: The quiescent current is the current which flows through the ground when the LDO operates without a load on its output: internal IC operation, bias, etc. When the LDO becomes loaded, this term is called the Ground current. It is actually the difference between the input current (measured through the LDO input pin) and the output current.

Ripple Rejection: The ratio of the peak−to−peak input ripple voltage to the peak−to−peak output ripple voltage.

Current Limit: Peak current that can be delivered to the output.

Calculating Power Dissipation

The maximum power dissipation for a single output regulator (Figure 21) is:

$$P_{D(max)} = \left[V_{in(max)} - V_{out(min)}\right]I_{out(max)} + V_{in(max)}I_{GND} \quad \text{(eq. 1)}$$

Where

$V_{in(max)}$ is the maximum input voltage,

$V_{out(min)}$ is the minimum output voltage,

$I_{out(max)}$ is the maximum output current for the application,

I_{GND} is the ground current at $I_{out(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = \frac{(150°C - T_A)}{P_D} \quad \text{(eq. 2)}$$

The value of $R_{\theta JA}$ can then be compared with those in the Thermal Characteristics table. Those packages with $R_{\theta JA}$ less than the calculated value in Equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heat sink will be required.

Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad \text{(eq. 3)}$$

where

$R_{\theta JC}$ is the junction−to−case thermal resistance,

$R_{\theta CS}$ is the case−to−heatsink thermal resistance,

$R_{\theta SA}$ is the heatsink−to−ambient thermal resistance.

$R_{\theta JC}$ appears in the Thermal Characteristics table. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heat sink and the interface between them. These values appear in data sheets of heat sink manufacturers.

Thermal, mounting, and heat sink considerations are further discussed in ON Semiconductor Application Note AN1040/D.

ORDERING INFORMATION

Device	Nominal Output Voltage*	Package Marking	Package	Shipping†
NCP5500DT15RKG	1.5	P5500LG	DPAK 5 (Pb−Free)	2500 / Tape & Reel
NCV5500DT15RKG**		V5500LG	DPAK 5 (Pb−Free)	2500 / Tape & Reel
NCP5501DT15RKG		P5501LG	DPAK 3 (Pb−Free)	2500 / Tape & Reel
NCV5501DT15RKG**		V5501LG	DPAK 3 (Pb−Free)	2500 / Tape & Reel
NCP5501DT15G		P5501LG	DPAK 3 (Pb−Free)	75 Units / Rail
NCV5501DT15G**		V5501LG	DPAK 3 (Pb−Free)	75 Units / Rail
NCP5500DT33RKG	3.3	P5500TG	DPAK 5 (Pb−Free)	2500 / Tape & Reel
NCV5500DT33RKG**		V5500TG	DPAK 5 (Pb−Free)	2500 / Tape & Reel
NCP5501DT33RKG		P5501TG	DPAK 3 (Pb−Free)	2500 / Tape & Reel
NCV5501DT33RKG**		V5501TG	DPAK 3 (Pb−Free)	2500 / Tape & Reel
NCP5501DT33G		P5501TG	DPAK 3 (Pb−Free)	75 Units / Rail
NCV5501DT33G**		V5501TG	DPAK 3 (Pb−Free)	75 Units / Rail
NCP5500DT50RKG	5.0	P5500UG	DPAK 5 (Pb−Free)	2500 / Tape & Reel
NCV5500DT50RKG**		V5500UG	DPAK 5 (Pb−Free)	2500 / Tape & Reel
NCP5501DT50RKG		P5501UG	DPAK 3 (Pb−Free)	2500 / Tape & Reel
NCV5501DT50RKG**		V5501UG	DPAK 3 (Pb−Free)	2500 / Tape & Reel
NCP5501DT50G		P5501UG	DPAK 3 (Pb−Free)	75 Units / Rail
NCV5501DT50G**		V5501UG	DPAK 3 (Pb−Free)	75 Units / Rail
NCP5500DTADJRKG	Adjustable	P5500WG	DPAK 5 (Pb−Free)	2500 / Tape & Reel
NCV5500DTADJRKG**		V5500WG	DPAK 5 (Pb−Free)	2500 / Tape & Reel
NCP5500DADJR2G	Adjustable	5500B	SO−8 (Pb−Free)	2500 / Tape & Reel
NCV5500DADJR2G**	Adjustable	5500A	SO−8 (Pb−Free)	2500 / Tape & Reel

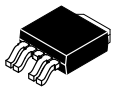
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*Contact ON Semiconductor for other fixed voltages.

**NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

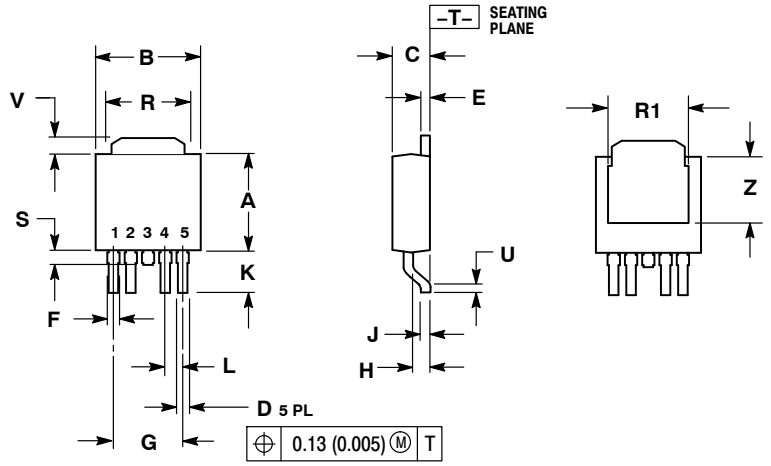
ON Semiconductor®



DPAK−5, CENTER LEAD CROP
CASE 175AA
ISSUE B

DATE 15 MAY 2014

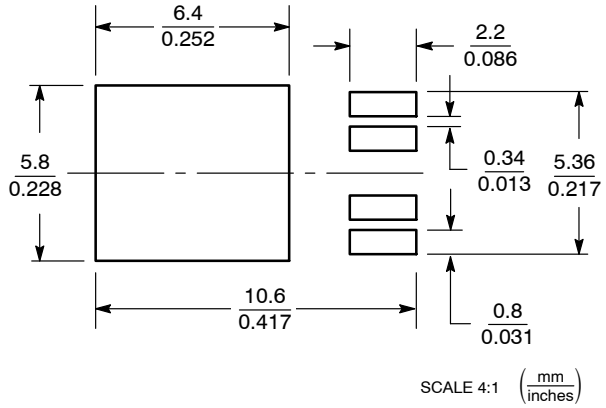
SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.020	0.028	0.51	0.71
E	0.018	0.023	0.46	0.58
F	0.024	0.032	0.61	0.81
G	0.180 BSC		4.56 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.045 BSC		1.14 BSC	
R	0.170	0.190	4.32	4.83
R1	0.185	0.210	4.70	5.33
S	0.025	0.040	0.63	1.01
U	0.020	−−−	0.51	−−−
V	0.035	0.050	0.89	1.27
Z	0.155	0.170	3.93	4.32

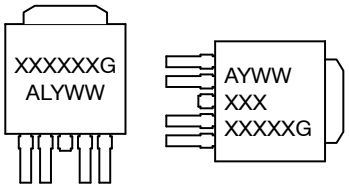
RECOMMENDED SOLDERING FOOTPRINT*



SCALE 4:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAMS*

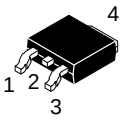


IC **Discrete**

XXXXXX	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

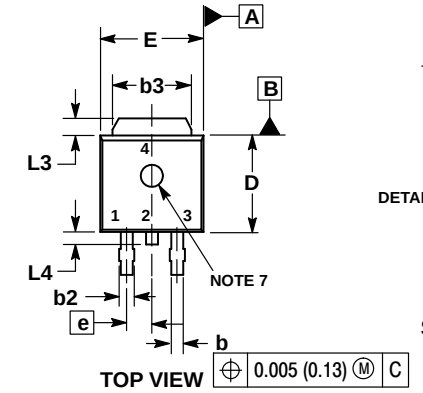
DOCUMENT NUMBER:	**98AON12855D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**DPAK−5 CENTER LEAD CROP**	**PAGE 1 OF 1**



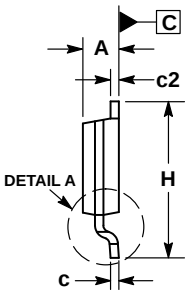
SCALE 1:1

DPAK (SINGLE GAUGE)
CASE 369C
ISSUE F

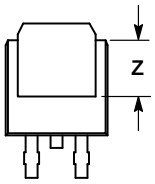
DATE 21 JUL 2015



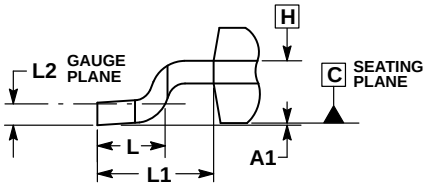
TOP VIEW



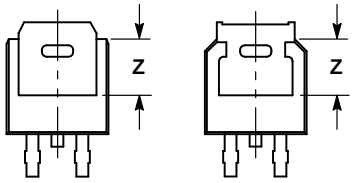
SIDE VIEW



BOTTOM VIEW



DETAIL A
ROTATED 90° CW



BOTTOM VIEW
ALTERNATE CONSTRUCTIONS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

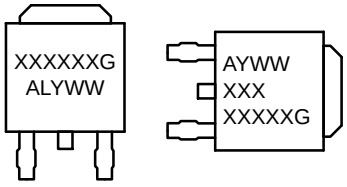
STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

GENERIC MARKING DIAGRAM*

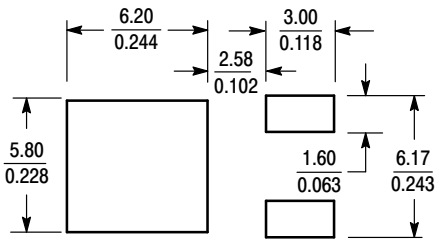


IC **Discrete**

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

SOLDERING FOOTPRINT*



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION. REQ. BY L. GAN	24 SEP 2001
A	ADDED STYLE 8. REQ. BY S. ALLEN.	06 AUG 2008
B	ADDED STYLE 9. REQ. BY D. WARNER.	16 JAN 2009
C	ADDED STYLE 10. REQ. BY S. ALLEN.	09 JUN 2009
D	RELABELED DRAWING TO JEDEC STANDARDS. ADDED SIDE VIEW DETAIL A. CORRECTED MARKING INFORMATION. REQ. BY D. TRUHITTE.	29 JUN 2010
E	ADDED ALTERNATE CONSTRUCTION BOTTOM VIEW. MODIFIED DIMENSIONS b2 AND L1. CORRECTED MARKING DIAGRAM FOR DISCRETE. REQ. BY I. CAMBALIZA.	06 FEB 2014
F	ADDED SECOND ALTERNATE CONSTRUCTION BOTTOM VIEW. REQ. BY K. MUSTAFA.	21 JUL 2015

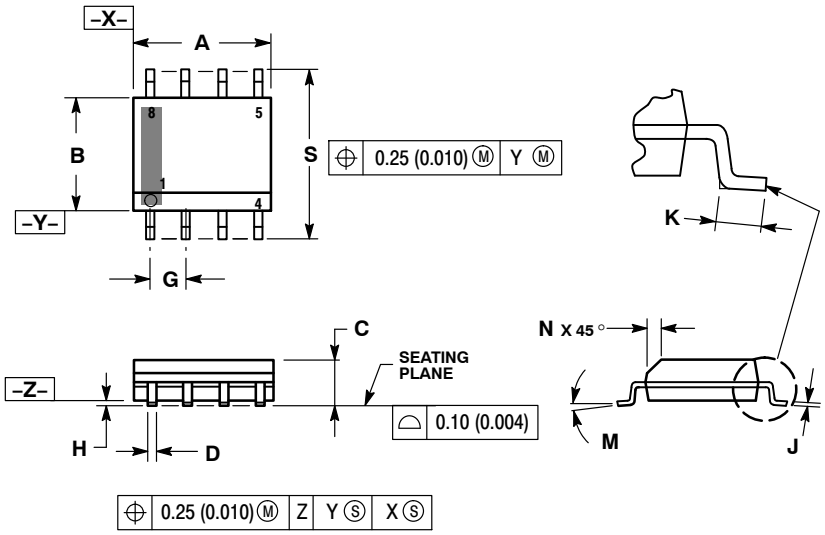
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

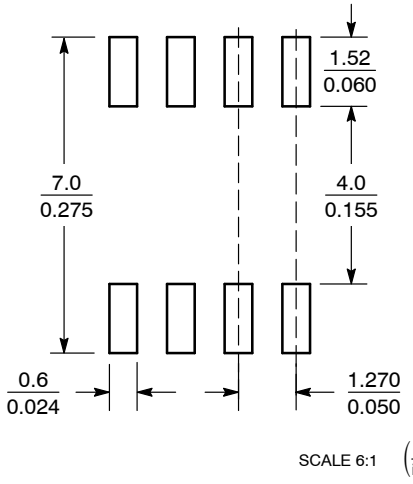
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

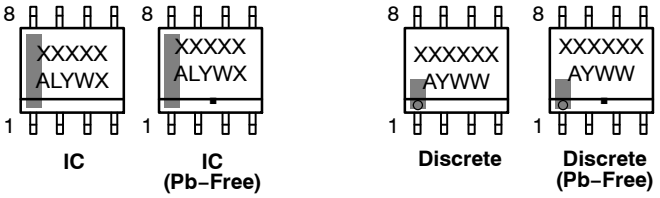
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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