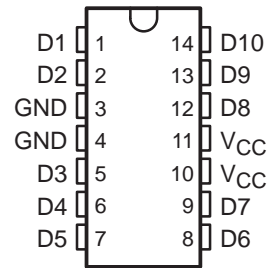


SN74ACT1071 10-BIT BUS-TERMINATION ARRAY WITH BUS-HOLD FUNCTION

SCAS192 – D3994, MARCH 1992 – REVISED APRIL 1993

- Designed to Ensure Defined Voltage Levels on Floating Bus Lines in CMOS Systems
- Reduces Undershoot and Overshoot Caused By Line Reflections
- Repetitive Peak Forward Current . . . $I_{FRM} = 100\text{ mA}$
- Inputs Are TTL-Voltage Compatible
- Low Power Consumption (Like CMOS)
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200\text{ pF}$, $R = 0$)
- Center-Pin V_{CC} and GND Configuration Minimizes High-Speed Switching Noise

D PACKAGE
(TOP VIEW)



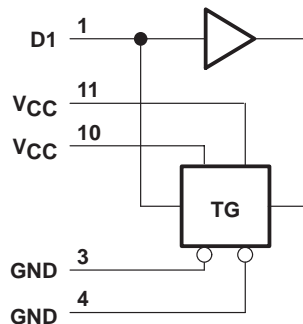
description

This device is designed to terminate bus lines in CMOS systems. The integrated low-impedance diodes clamp the voltage of undershoots and overshoots caused by line reflections and ensure signal integrity. The device also contains a bus-hold function that consists of a CMOS-buffer stage with a high-resistance feedback path between its output and its input. The SN74ACT1071 prevents bus lines from floating without using pullup or pulldown resistors.

The high-impedance inputs of these internal buffers are connected to the input terminals of the device. The feedback path on each internal buffer stage keeps a bus line tied to the bus holder at the last valid logic state generated by an active driver before the bus switches to the high-impedance state.

The SN74ACT1071 is characterized for operation from -40°C to 85°C .

logic diagram, one of ten channels (positive logic)



SN74ACT1071

10-BIT BUS-TERMINATION ARRAY

WITH BUS-HOLD FUNCTION

SCAS192 – D3994, MARCH 1992 – REVISED APRIL 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Continuous input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Positive-peak input clamp current, I_{IK} ($V_I > V_{CC}$) ($t_w < 1$ μs, duty cycle < 20%)	100 mA
Negative-peak input clamp current, I_{IK} ($V_I < 0$) ($t_w < 1$ μs, duty cycle < 20%)	–100 mA
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative-voltage rating may be exceeded if the input clamp-current rating is observed.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2.5		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
T_A	Operating free-air temperature	–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
		MIN	TYP [†]	MAX			
I_{IL}	$V_{CC} = 4.5$ to 5.5 V, $V_I = 0.8$ V	0.15	0.3	0.9	0.1	1	mA
I_{IH}	$V_{CC} = 4.5$ to 5.5 V, $V_I = 2.5$ V	–0.2	–0.5	–1.4	–0.15	–1.5	mA
V_{IKL}	$I_{IN} = -18$ mA			–1.5		–1.5	V
V_{IKH}	$I_{IN} = 18$ mA			$V_{CC} + 2$		$V_{CC} + 2$	V
I_{CC}^{\ddagger}	$V_{CC} = 5.5$ V, Inputs open			4		40	μA
ΔI_{CC}^{\S}	One input at 3.4 V, Other inputs at V_{CC} or GND			0.9		1	mA
C_i	$V_I = V_{CC}$ or GND		3				pF

[†] All typical values are at $V_{CC} = 5$ V.

[‡] Inputs may be set high or low prior to the I_{CC} measurement.

[§] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC} .



TYPICAL CHARACTERISTICS

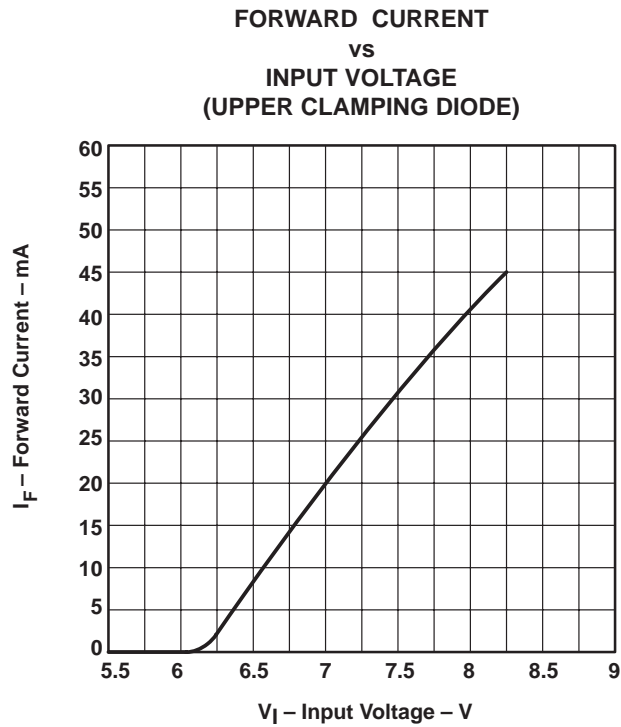


Figure 1

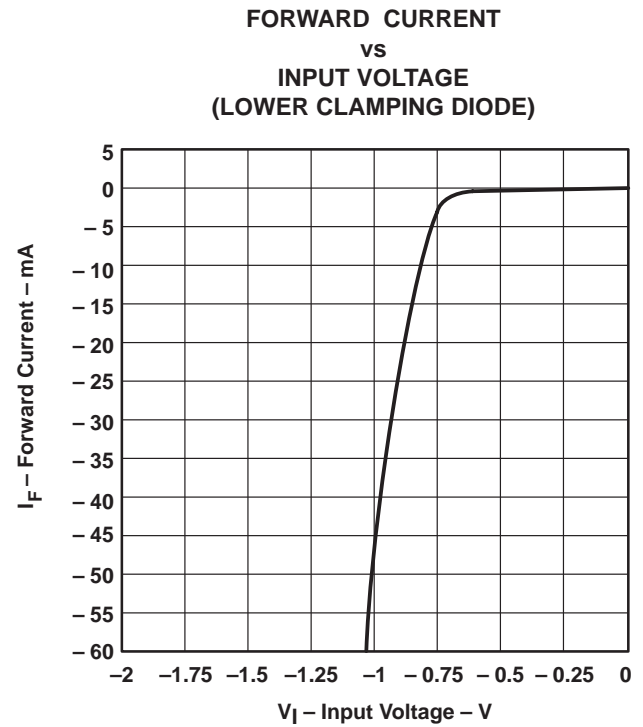


Figure 2

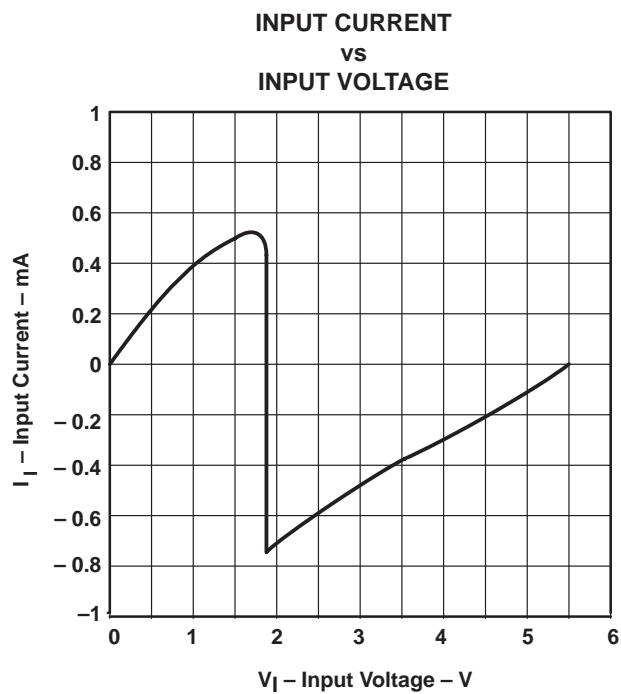


Figure 3

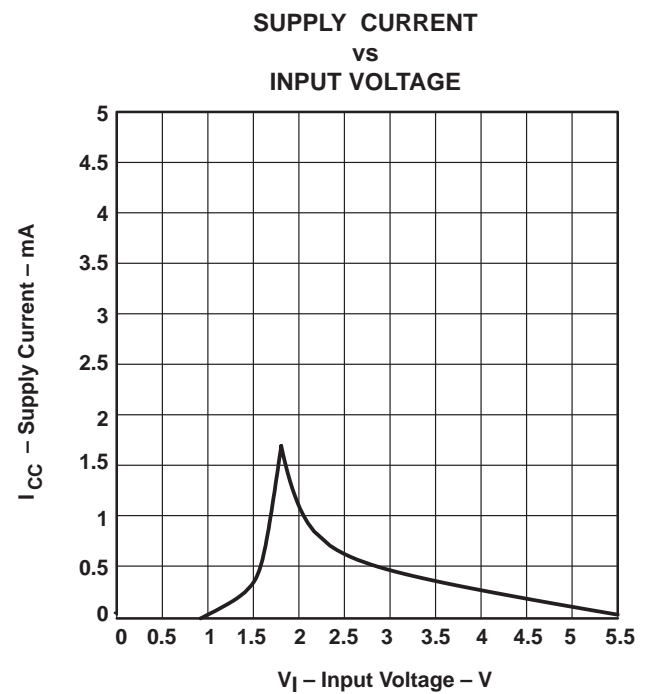


Figure 4

SN74ACT1071

10-BIT BUS-TERMINATION ARRAY WITH BUS-HOLD FUNCTION

SCAS192 – D3994, MARCH 1992 – REVISED APRIL 1993

APPLICATION INFORMATION

The SN74ACT1071 terminates the output of a driving device and holds the input of the driven device at the logic level of the driver output prior to establishment of the high-impedance state on that output (see Figure 5).

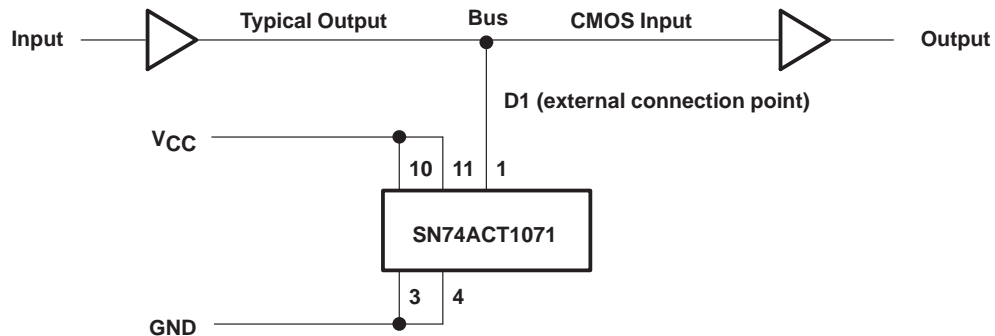


Figure 5. Bus-Hold Application

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ACT1071D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT1071	Samples
SN74ACT1071DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT1071	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ACT1071DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ACT1071DR	SOIC	D	14	2500	367.0	367.0	38.0

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated