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FDS6930A

Dual N-Channel, Logic Level, PowerTrench™ MOSFET

General Description

These N-Channel Logic Level MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

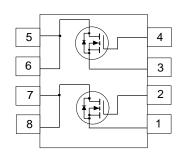
These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Features

- Fast switching speed.
- Low gate charge (typical 5 nC).
- High performance trench technology for extremely low Research
- High power and current handling capability.





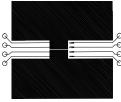


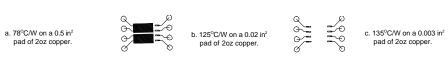
Absolute Maximum Ratings $T_A = 25^{\circ}\text{C}$ unless otherwise noted

Symbol	Parameter	FDS6930A	Units
V _{DSS}	Drain-Source Voltage	30	V
V_{GSS}	Gate-Source Voltage	±20	V
D	Drain Current - Continuous (Note 1a)	5.5	А
	- Pulsed	20	
P_{D}	Power Dissipation for Dual Operation (Note 1)	2	W
	Power Dissipation for Single Operation (Note 1a)	1.6	W
	(Note 1b)	1	
	(Note 1c)	0.9	
$\Gamma_{\rm J}$, $T_{ m STG}$	Operating and Storage Temperature Range	-55 to 150	°C
THERMA	L CHARACTERISTICS		•
R_{BJA}	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	°C/W
R _{euc}	Thermal Resistance, Junction-to-Case (Note 1)	40	°C/W

Symbol	Parameter	Conditions		Min	Тур	Max	Units
OFF CHAR	ACTERISTICS			•		•	•
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$		30			V
$\Delta BV_{DSS}/\Delta T_{J}$	Breakdown Voltage Temp. Coefficient	I _D = 250 μA, Referenced to 25 °C			20		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V				1	μA
			$T_J = 55^{\circ}C$			10	μA
I _{GSSF}	Gate - Body Leakage, Forward	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$	•			100	nA
I _{GSSR}	Gate - Body Leakage, Reverse	$V_{GS} = -20 \text{ V}, V_{DS} = 0 \text{ V}$				-100	nA
	CTERISTICS (Note 2)			,			
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$		1	1.5	3	V
$\Delta V_{GS(th)}/\Delta T_{J}$	Gate Threshold Voltage Temp. Coefficient	I _D = 250 μA, Referenced to 25 °C			-4		mV/°C
R _{DS(ON)}	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_D = 5.5 \text{ A}$			0.032	0.04	Ω
-(- /			T _J =125°C		0.048	0.068	
		$V_{GS} = 4.5 \text{ V}, I_D = 4.8 \text{ A}$	- I - -		0.044	0.055	
I _{D(ON)}	On-State Drain Current	$V_{GS} = 10 \text{ V}, \ V_{DS} = 5 \text{ V}$		20			Α
9 _{FS}	Forward Transconductance	$V_{DS} = 15 \text{ V}, I_{D} = 5.5 \text{ A}$			12		S
DYNAMIC (CHARACTERISTICS						•
C _{iss}	Input Capacitance	$V_{DS} = 15 \text{ V}, \ V_{GS} = 0 \text{ V},$ $f = 1.0 \text{ MHz}$			460		pF
C _{oss}	Output Capacitance				115		pF
C _{rss}	Reverse Transfer Capacitance				45		pF
SWITCHING	CHARACTERISTICS (Note 2)			1	1		
t _{D(on)}	Turn - On Delay Time	$V_{DS} = 15 \text{ V}, \ I_D = 1 \text{ A}$ $V_{GS} = 10 \text{ V}, \ R_{GEN} = 6 \Omega$			5	11	ns
t _r	Turn - On Rise Time				8	17	ns
t _{D(off)}	Turn - Off Delay Time				17	28	ns
t _f	Turn - Off Fall Time				13	24	ns
Q_g	Total Gate Charge	$V_{DS} = 5 \text{ V}, I_{D} = 5.5 \text{ A},$			5	7	nC
Q_{gs}	Gate-Source Charge	V _{GS} = 5 V			2		nC
Q_{gd}	Gate-Drain Charge				0.9		nC
DRAIN-SOU	RCE DIODE CHARACTERISTICS AND MAX	(IMUM RATINGS					
I _s	Maximum Continuous Drain-Source Diode Forward Current					1.3	Α
V _{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 1.3 \text{ A} \text{ (Note 2)}$				1.2	V

^{1.} $R_{g,u,i}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{g,c,i}$ is guaranteed by design while $R_{g,c,i}$ is determined by the user's board design.









Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width \leq 300µs, Duty Cycle \leq 2.0%.

Typical Electrical Characteristics

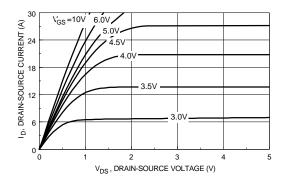


Figure 1. On-Region Characteristics.

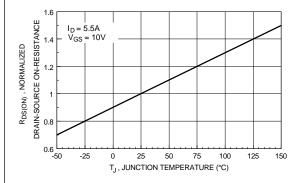


Figure 3. On-Resistance Variation with Temperature.

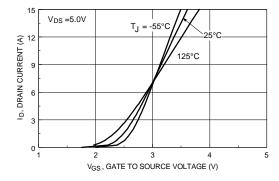


Figure 5. Transfer Characteristics.

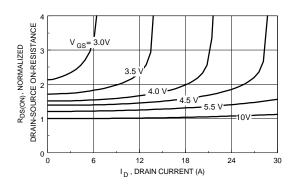


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

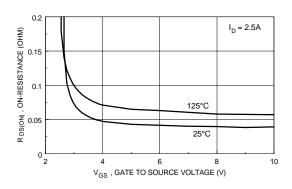


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

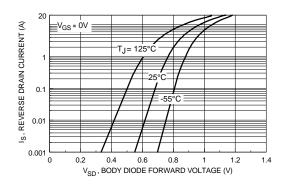
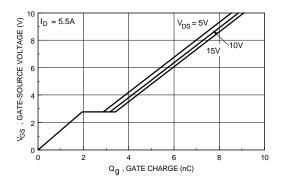


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

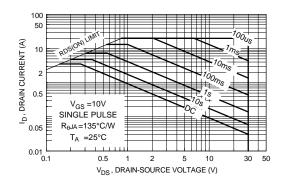
Typical Electrical Characteristics



1000 500 500 500 500 Ciss Coss Coss 0.1 0.2 0.5 1 2 5 10 30 VDS, DRAIN TO SOURCE VOLTAGE (V)

Figure 7. Gate Charge Characteristics.





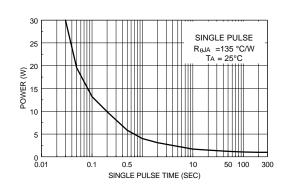


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

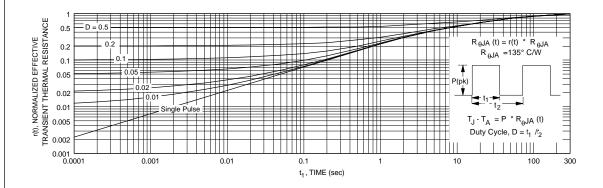


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

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 E^2CMOS^{TM} PowerTrenchTM

FACT™ QFET™ FACT Quiet Series™ QS™

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