

SN74LVC1G06 Single Inverter Buffer/Driver With Open-Drain Output

1 Features

- ESD Protection Exceeds JESD 22
 - 2000-V Human Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V V_{CC} Operation
- Input and Open-Drain Output Accept Voltages up to 5.5 V
- Maximum t_{pd} of 4.5 ns at 3.3 V at 125°C
- Low Power Consumption, 10- μ A Maximum I_{CC}
- ± 24 -mA Output Drive at 3.3 V for open-drain devices
- I_{off} Supports Partial-Power-Down Mode and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- Can Be Used For Up or Down Translation
- Schmitt Trigger Action on All Ports

2 Applications

- AV Receivers
- Blu-ray Players and Home Theaters
- DVD Recorders and Players
- Desktop or Notebook PCs
- Digital Radio or Internet Radio Players
- Digital Video Cameras (DVC)
- Embedded PCs
- GPS: Personal Navigation Devices
- Mobile Internet Devices
- Network Projector Front-Ends
- Portable Media Players
- Pro Audio Mixers
- Smoke Detectors
- Solid State Drive (SSD): Enterprise
- High-Definition (HDTV)
- Tablets: Enterprise
- Audio Docks: Portable
- DLP Front Projection Systems
- DVR and DVS
- Digital Picture Frame (DPF)
- Digital Still Cameras

3 Description

This single inverter buffer and driver is designed for 1.65-V to 5.5-V V_{CC} operation.

NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package.

The output of the SN74LVC1G06 device is open-drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 32 mA.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|----------------|-------------|-------------------|
| SN74LVC1G06DBV | SOT-23 (5) | 2.90 mm x 1.60 mm |
| SN74LVC1G06DCK | SC70 (5) | 2.00 mm x 1.25 mm |
| SN74LVC1G06DRL | SOT-5X3 (5) | 1.60 mm x 1.20 mm |
| SN74LVC1G06DRY | SON (6) | 1.45 mm x 1.00 mm |
| SN74LVC1G06DSF | SON (6) | 1.00 mm x 1.00 mm |
| SN74LVC1G06YZP | DSBGA (5) | 1.40 mm x 0.90 mm |
| SN74LVC1G06YZV | DSBGA (4) | 0.90 mm x 0.90 mm |
| SN74LVC1G06DPW | X2SON (5) | 0.80 mm x 0.80 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



Table of Contents

| | | | |
|--|----------|--|-----------|
| 1 Features | 1 | 8.2 Functional Block Diagram | 9 |
| 2 Applications | 1 | 8.3 Feature Description | 9 |
| 3 Description | 1 | 8.4 Device Functional Modes | 10 |
| 4 Revision History | 2 | 9 Application and Implementation | 11 |
| 5 Pin Configuration and Functions | 3 | 9.1 Application Information | 11 |
| 6 Specifications | 4 | 9.2 Typical Application | 11 |
| 6.1 Absolute Maximum Ratings | 4 | 10 Power Supply Recommendations | 13 |
| 6.2 ESD Ratings | 4 | 11 Layout | 13 |
| 6.3 Recommended Operating Conditions | 5 | 11.1 Layout Guidelines | 13 |
| 6.4 Thermal Information | 5 | 11.2 Layout Example | 13 |
| 6.5 Electrical Characteristics | 6 | 12 Device and Documentation Support | 14 |
| 6.6 Switching Characteristics: –40°C to +85°C | 6 | 12.1 Receiving Notification of Documentation Updates | 14 |
| 6.7 Switching Characteristics: –40°C to +125°C | 6 | 12.2 Community Resources | 14 |
| 6.8 Operating Characteristics | 6 | 12.3 Trademarks | 14 |
| 6.9 Typical Characteristics | 7 | 12.4 Electrostatic Discharge Caution | 14 |
| 7 Parameter Measurement Information | 8 | 12.5 Glossary | 14 |
| 8 Detailed Description | 9 | 13 Mechanical, Packaging, and Orderable Information | 14 |
| 8.1 Overview | 9 | | |

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

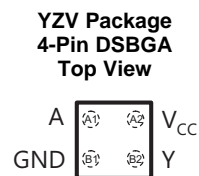
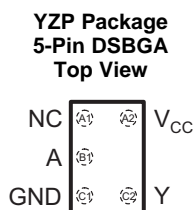
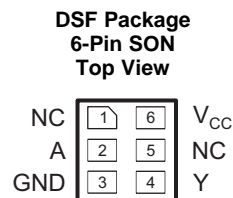
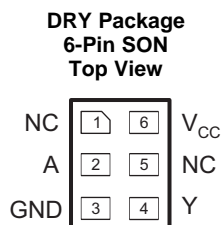
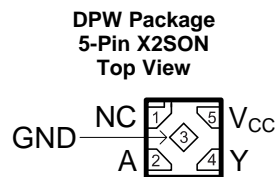
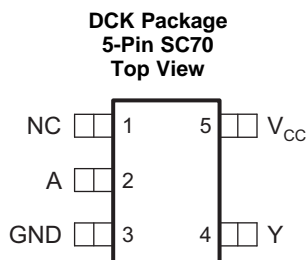
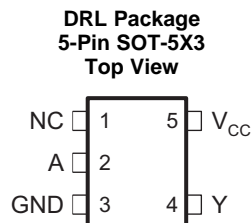
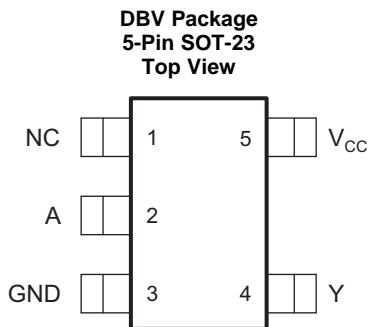
| Changes from Revision Y (February 2017) to Revision Z | Page |
|---|-------------|
| • Changed values in the Thermal Information table to align with JEDEC standards | 5 |
| • Updated Feature Description to include more detailed information about specific device features. | 9 |
| • Added DPW layout example | 13 |

| Changes from Revision X (August 2015) to Revision Y | Page |
|--|-------------|
| • Changed <i>Logic Diagram (Positive Logic)</i> labels from: A-1, Y-3 to: A-2, Y-4 | 1 |
| • Added <i>Receiving Notification of Documentation Updates</i> section | 14 |

| Changes from Revision W (December 2013) to Revision X | Page |
|---|-------------|
| • Added <i>Device Information</i> table, <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Typical Characteristics</i> section, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section | 1 |

| Changes from Revision V (November 2012) to Revision W | Page |
|--|-------------|
| • Updated document to new TI data sheet format | 1 |
| • Removed <i>Ordering Information</i> table. | 1 |
| • Updated I_{off} in <i>Features</i> | 1 |
| • Updated operating temperature range. | 5 |

5 Pin Configuration and Functions



Pin Functions⁽¹⁾⁽²⁾

| NAME | PIN | | | | I/O | DESCRIPTION |
|-----------------|--------------------|----------|-----|-----|-----|---------------|
| | DBV, DCK, DRL, DPW | DRY, DSF | YZP | YZV | | |
| A | 2 | 2 | B1 | A1 | I | Input |
| DNU | — | — | A1 | — | — | Do not use |
| GND | 3 | 3 | C1 | B1 | — | Ground |
| NC | 1 | 1 | — | — | — | Not connected |
| | | 5 | | | | |
| V _{CC} | 5 | 6 | A2 | A2 | — | Power pin |
| Y | 4 | 4 | C2 | B2 | O | Output |

(1) NC – No internal connection

(2) See mechanical drawings for dimensions.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|------------------|---|--------------------|------|------|
| V _{CC} | Supply voltage | -0.5 | 6.5 | V |
| V _I | Input voltage ⁽²⁾ | -0.5 | 6.5 | V |
| V _O | Voltage applied to any output in the high-impedance or power-off state ⁽²⁾ | -0.5 | 6.5 | V |
| V _O | Voltage applied to any output in the high or low state ⁽²⁾⁽³⁾ | -0.5 | 6.5 | V |
| I _{IK} | Input clamp current | V _I < 0 | -50 | mA |
| I _{OK} | Output clamp current | V _O < 0 | -50 | mA |
| I _O | Continuous output current | | ±50 | mA |
| | Continuous current through V _{CC} or GND | | ±100 | mA |
| T _j | Junction temperature | -65 | 150 | °C |
| T _{stg} | Storage temperature | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

6.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|-------------------------|--|------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | 2000 |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | 1000 |
| | | Machine Model (MM), per A115-A | 200 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT | |
|-----------------|------------------------------------|---|------------------------|------------------------|------|
| V _{CC} | Supply voltage | Operating | 1.65 | 5.5 | V |
| | | Data retention only | 1.5 | | |
| V _{IH} | High-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.65 × V _{CC} | | V |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | | |
| | | V _{CC} = 3 V to 3.6 V | 2 | | |
| | | V _{CC} = 4.5 V to 5.5 V | 0.7 × V _{CC} | | |
| V _{IL} | Low-level input voltage | V _{CC} = 1.65 V to 1.95 V | | 0.35 × V _{CC} | V |
| | | V _{CC} = 2.3 V to 2.7 V | | 0.7 | |
| | | V _{CC} = 3 V to 3.6 V | | 0.8 | |
| | | V _{CC} = 4.5 V to 5.5 V | | 0.3 × V _{CC} | |
| V _I | Input voltage | 0 | 5.5 | V | |
| V _O | Output voltage | 0 | 5.5 | V | |
| I _{OL} | Low-level output current | V _{CC} = 1.65 V | | 4 | mA |
| | | V _{CC} = 2.3 V | | 8 | |
| | | V _{CC} = 3 V | | 16 | |
| | | | | 24 | |
| | | V _{CC} = 4.5 V | | 32 | |
| Δt/Δv | Input transition rise or fall rate | V _{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V | | 20 | ns/V |
| | | V _{CC} = 3.3 V ± 0.3 V | | 10 | |
| | | V _{CC} = 5 V ± 0.5 V | | 5 | |
| T _A | Operating free-air temperature | −40 | 125 | °C | |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs application report](#).

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | SN74LVC1G06 | | | | | | | UNIT | |
|-------------------------------|--|---------------|------------------|--------------|----------------|----------------|----------------|-------|------|
| | DBV (SOT-23) | DCK (SC70) | DRL (SOT-5X3) | DRY (SON) | DPW (X2SON) | YZV (DSBGA) | YZP (DSBGA) | | |
| | 5 PINS | 5 PINS | 5 PINS | 5 PINS | 5 PINS | 4 PINS | 5 PINS | | |
| R _{θJA} | Junction-to-ambient thermal resistance | 231.5 | 276.1 | 296.2 | 369.6 | 511 | 168.2 | 144.4 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 139.4 | 178.9 | 137.3 | 257.6 | 241.9 | 2.1 | 1.3 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 71.1 | 70.9 | 145.3 | 230.8 | 374.2 | 55.9 | 39.9 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 45.2 | 47 | 14.7 | 77.2 | 45 | 1.1 | 0.5 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 70.7 | 69.3 | 145.9 | 231 | 373.3 | 56.3 | 39.7 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | N/A | 168 | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | V _{CC} | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|--|--|---------|-----------------|-----|--------------------|------|------|
| V _{OL} High-level output voltage | I _{OL} = 100 μA | | 1.65 V to 5.5 V | | | 0.1 | V |
| | I _{OL} = 4 mA | | 1.65 V | | | 0.45 | |
| | I _{OL} = 8 mA | | 2.3 V | | | 0.3 | |
| | I _{OL} = 16 mA | | 3 V | | | 0.4 | |
| | I _{OL} = 24 mA | | | | | 0.55 | |
| | I _{OL} = 32 mA | | 4.5 V | | | 0.55 | |
| I _I Inflection-point current | V _I = 5.5 V or GND | A input | 0 to 5.5 V | | | ±1 | μA |
| I _{off} Off-state current | V _I or V _O = 5.5 V | | 0 | | | ±10 | μA |
| I _{CC} | V _I = 5.5 V or GND, I _O = 0 | | 1.65 V to 5.5 V | | | 10 | μA |
| ΔI _{CC} | One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND | | 3 V to 5.5 V | | | 500 | μA |
| C _I Input capacitance | V _I = V _{CC} or GND | | 3.3 V | | 4 | | pF |
| C _O Off-state capacitance | V _O = V _{CC} or GND | | 3.3 V | | 5 | | pF |

 (1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

6.6 Switching Characteristics: –40°C to +85°C

 over recommended operating free-air temperature range, T_A = –40°C to +85°C (unless otherwise noted) (see [Figure 3](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} | MIN | MAX | UNIT |
|--------------------------------------|--------------|-------------|-----------------|-----|-----|------|
| t _{pd} Propagation delay | A | Y | 1.8 V ± 0.15 V | 2.2 | 6.5 | ns |
| | | | 2.5 V ± 0.2 V | 1.1 | 4 | |
| | | | 3.3 V ± 0.3 V | 1.2 | 4 | |
| | | | 5 V ± 0.5 V | 1 | 3 | |

6.7 Switching Characteristics: –40°C to +125°C

 over recommended operating free-air temperature range, T_A = –40°C to +125°C (unless otherwise noted) (see [Figure 3](#))

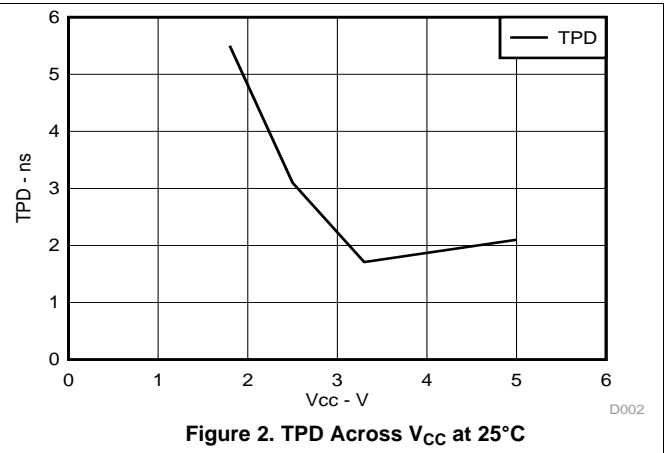
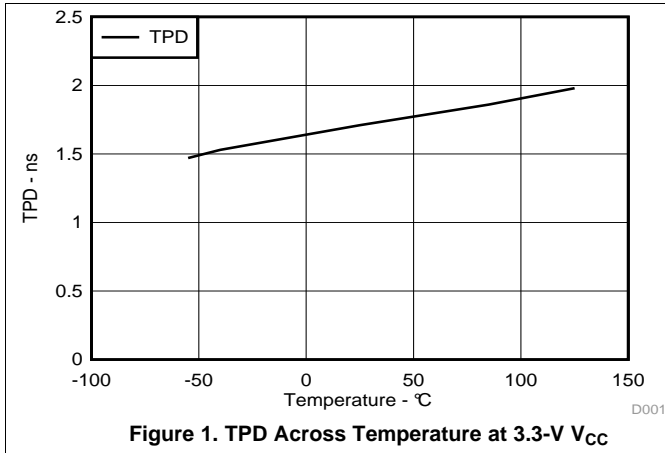
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} | MIN | MAX | UNIT |
|--------------------------------------|--------------|-------------|-----------------|-----|-----|------|
| t _{pd} Propagation delay | A | Y | 1.8 V ± 0.15 V | 2.2 | 7 | ns |
| | | | 2.5 V ± 0.2 V | 1.1 | 4.5 | |
| | | | 3.3 V ± 0.3 V | 1.2 | 4.5 | |
| | | | 5 V ± 0.5 V | 1 | 3.5 | |

6.8 Operating Characteristics

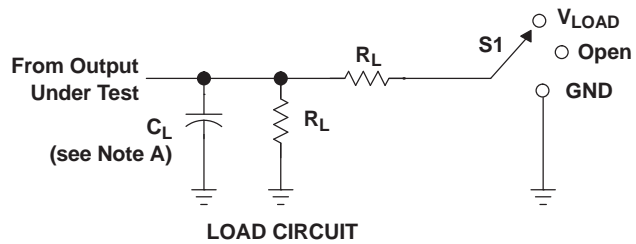
 T_A = 25°C

| PARAMETER | TEST CONDITIONS | V _{CC} | TYP | UNIT |
|--|-----------------|-----------------|-----|------|
| C _{pd} Power dissipation capacitance | f = 10 MHz | 1.8 V | 3 | pF |
| | | 2.5 V | 3 | |
| | | 3.3 V | 4 | |
| | | 5 V | 6 | |

6.9 Typical Characteristics

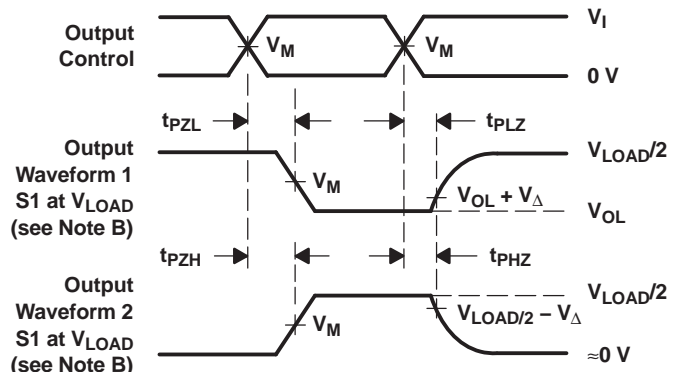
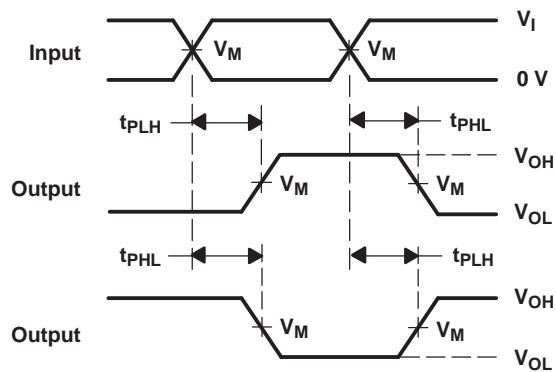
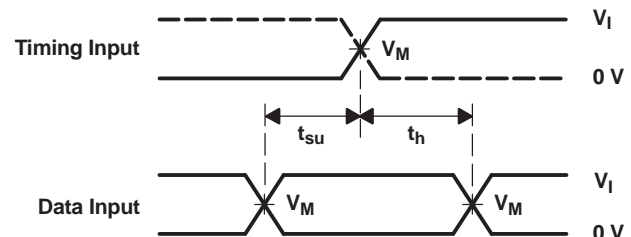
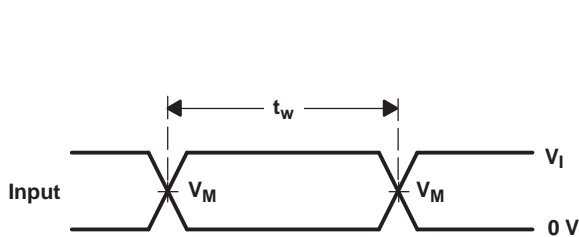


7 Parameter Measurement Information



| TEST | S1 |
|-------------------------------|------------|
| t_{pZL} (see Notes E and F) | V_{LOAD} |
| t_{pLZ} (see Notes E and G) | V_{LOAD} |
| t_{PHZ}/t_{PZH} | V_{LOAD} |

| V_{CC} | INPUT | | V_M | V_{LOAD} | C_L | R_L | V_Δ |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|------------|
| | V_I | t_r/t_f | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 3 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| $5\text{ V} \pm 0.5\text{ V}$ | V_{CC} | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 Ω | 0.3 V |



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - Since this device has open-drain outputs, t_{pLZ} and t_{pZL} are the same as t_{pd} .
 - t_{pZL} is measured at V_M .
 - t_{pLZ} is measured at $V_{OL} + V_\Delta$.
 - All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms (Open Drain)

8 Detailed Description

8.1 Overview

The SN74LVC1G06 device contains one open-drain inverter with a maximum sink current of 32 mA. This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

8.2 Functional Block Diagram

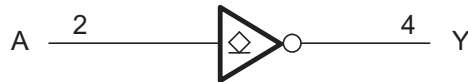


Figure 4. Logic Diagram (Positive Logic)

8.3 Feature Description

8.3.1 CMOS Open-Drain Outputs

The open-drain output allows the device to sink current to GND but not to source current from V_{CC} . When the output is not actively pulling the line low, it will go into a high impedance state (tri-state). This allows the device to be used for a wide variety of applications, including up-translation and down-translation, as the output voltage can be determined by an external pullup.

The drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined in the [Absolute Maximum Ratings](#) must be followed at all times.

8.3.2 Standard CMOS Inputs

The impedance for standard CMOS inputs is high. Typically, a CMOS input is modeled as a resistor in parallel with the input capacitance as shown in the [Electrical Characteristics](#). The worst case resistance is calculated with the maximum input voltage, given in the [Absolute Maximum Ratings](#), and the maximum input leakage current, given in the [Electrical Characteristics](#), using ohm's law ($R = V \div I$).

Signals applied to the inputs need to have fast edge rates, as defined by $\Delta t/\Delta v$ in the [Recommended Operating Conditions](#) to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal before the standard CMOS input.

Feature Description (continued)

8.3.3 Negative Clamping Diodes

The inputs and outputs to this device have negative clamping diodes as depicted in [Figure 5](#).

CAUTION

Voltages beyond the values specified in the [Absolute Maximum Ratings](#) table can cause damage to the device. The input negative-voltage and the output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

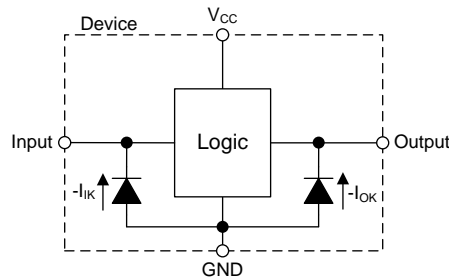


Figure 5. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.4 Partial Power Down (I_{off})

Each input and output enter a high impedance state when the supply voltage is 0 V. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the [Electrical Characteristics](#).

8.3.5 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage as long as the input signals remain below the maximum input voltage value specified in the [Recommended Operating Conditions](#).

8.4 Device Functional Modes

[Table 1](#) lists the functional modes of the SN74LVC1G06.

Table 1. Function Table

| INPUT A | OUTPUT Y |
|------------|-------------|
| L | Hi-Z |
| H | L |

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC1G06 is a high-drive CMOS device that can be used to implement a high output drive buffer, such as an LED application. It can sink 32 mA of current at 4.5 V making it ideal for high-drive applications. It is good for high-speed applications up to 100 MHz. The inputs are 5.5-V tolerant allowing it to translate up or down to V_{CC} . Below shows a simple LED driver application for a single channel of the device.

9.2 Typical Application

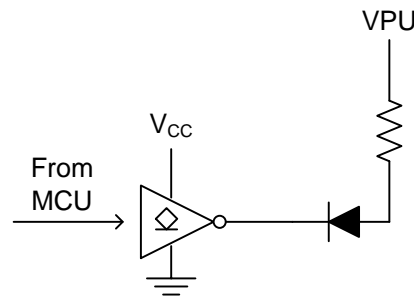


Figure 6. Typical Application Diagram

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
 - Rise time and fall time specs. See $(\Delta t/\Delta V)$ in the [Recommended Operating Conditions](#) table.
 - Specified high and low levels. See $(V_{IH}$ and $V_{IL})$ in the [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as $(V_I \text{ max})$ in the [Recommended Operating Conditions](#) table at any valid V_{CC} .
2. Recommended Output Conditions
 - Load currents should not exceed $(I_O \text{ max})$ per output and should not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in the [Absolute Maximum Ratings](#) table.
 - Outputs should not be pulled above 5.5 V.

Typical Application (continued)

9.2.3 Application Curve

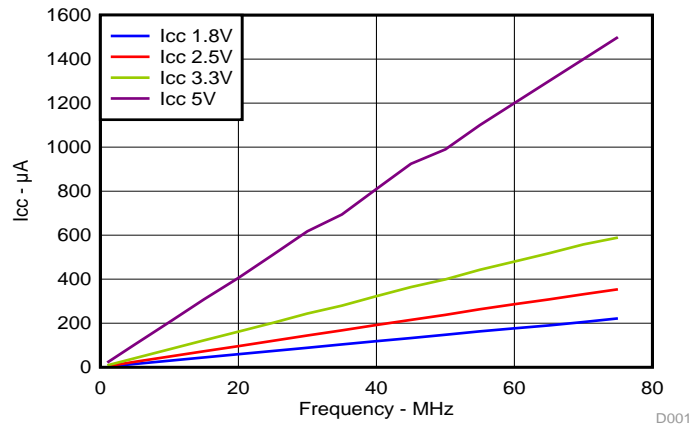


Figure 7. I_{CC} vs Frequency

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#) table.

The V_{CC} pin must have a good bypass capacitor to prevent power disturbance. A 0.1- μF capacitor is recommended, and it is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

Even low data rate digital signals can contain high-frequency signal components due to fast edge rates. When a printed-circuit board (PCB) trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. [Figure 8](#) shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

An example layout is given in [Figure 9](#) for the DPW (X2SON-5) package. This example layout includes a 0402 (metric) capacitor and uses the measurements found in the example board layout appended to this end of this datasheet. A via of diameter 0.1 mm (3.973 mil) is placed directly in the center of the device. This via can be used to trace out the center pin connection through another board layer, or it can be left out of the layout

11.2 Layout Example

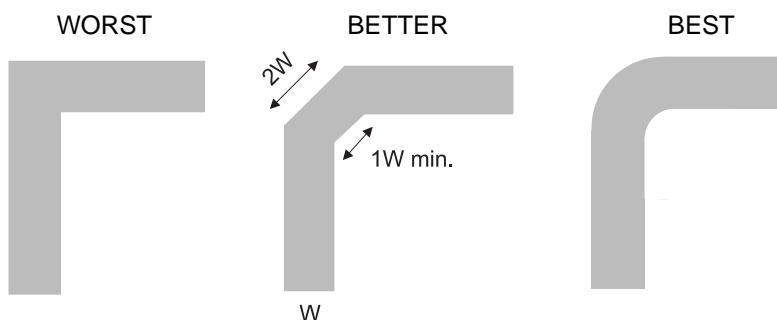


Figure 8. Trace Example

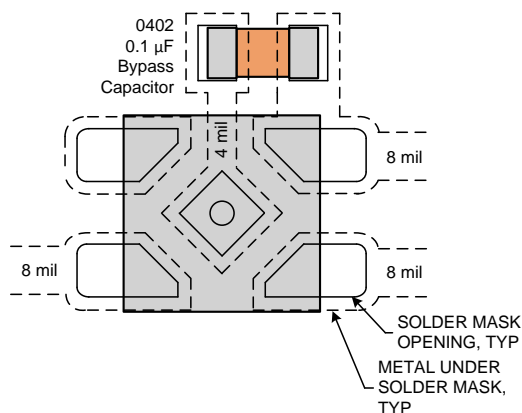


Figure 9. Example Layout With DPW (X2SON-5) Package

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|--|-------------------------|
| SN74LVC1G06DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU SN | Level-1-260C-UNLIM | -40 to 125 | (C065, C06F, C06J, C06R, C06T) (C06H, C06P, C06S) | Samples |
| SN74LVC1G06DBVRE4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C06F | Samples |
| SN74LVC1G06DBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C06F | Samples |
| SN74LVC1G06DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | NIPDAU SN | Level-1-260C-UNLIM | -40 to 125 | (C065, C06F, C06J, C06R) (C06H, C06P, C06S) | Samples |
| SN74LVC1G06DBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C06F | Samples |
| SN74LVC1G06DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (CT5, CTF, CTK, CT R, CTT) (CTH, CTS) | Samples |
| SN74LVC1G06DCKRE4 | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (CT5, CTF, CTK, CT R, CTT) (CTH, CTS) | Samples |
| SN74LVC1G06DCKRG4 | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (CT5, CTF, CTK, CT R, CTT) (CTH, CTS) | Samples |
| SN74LVC1G06DCKT | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (CT5, CTF, CTK, CT R) (CTH, CTS) | Samples |
| SN74LVC1G06DCKTE4 | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (CT5, CTF, CTK, CT R) (CTH, CTS) | Samples |
| SN74LVC1G06DCKTG4 | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (CT5, CTF, CTK, CT R) (CTH, CTS) | Samples |
| SN74LVC1G06DPWR | ACTIVE | X2SON | DPW | 5 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CO | Samples |
| SN74LVC1G06DRLR | ACTIVE | SOT-5X3 | DRL | 5 | 4000 | Green (RoHS & no Sb/Br) | NIPDAU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | (CT7, CTR) | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74LVC1G06DRYR | ACTIVE | SON | DRY | 6 | 5000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CT | Samples |
| SN74LVC1G06DSFR | ACTIVE | SON | DSF | 6 | 5000 | Green (RoHS & no Sb/Br) | NIPDAU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | CT | Samples |
| SN74LVC1G06YZPR | ACTIVE | DSBGA | YZP | 5 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | CTN | Samples |
| SN74LVC1G06YZVR | ACTIVE | DSBGA | YZV | 4 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | CT N | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC1G06 :

- Enhanced Product: [SN74LVC1G06-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

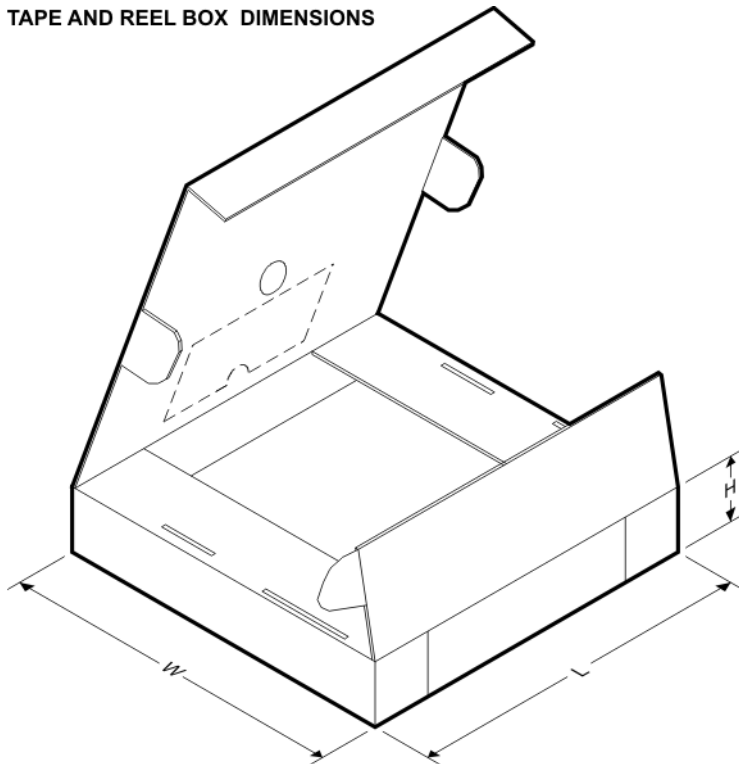


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC1G06DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74LVC1G06DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.2 | 3.3 | 3.23 | 1.55 | 4.0 | 8.0 | Q3 |
| SN74LVC1G06DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1G06DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1G06DBVRG4 | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1G06DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1G06DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.2 | 3.3 | 3.23 | 1.55 | 4.0 | 8.0 | Q3 |
| SN74LVC1G06DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1G06DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74LVC1G06DBVTG4 | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1G06DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1G06DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74LVC1G06DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.47 | 2.3 | 1.25 | 4.0 | 8.0 | Q3 |
| SN74LVC1G06DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74LVC1G06DCKT | SC70 | DCK | 5 | 250 | 180.0 | 8.4 | 2.47 | 2.3 | 1.25 | 4.0 | 8.0 | Q3 |
| SN74LVC1G06DPWR | X2SON | DPW | 5 | 3000 | 178.0 | 8.4 | 0.91 | 0.91 | 0.5 | 2.0 | 8.0 | Q3 |
| SN74LVC1G06DRLR | SOT-5X3 | DRL | 5 | 4000 | 180.0 | 8.4 | 1.98 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |
| SN74LVC1G06DRLR | SOT-5X3 | DRL | 5 | 4000 | 180.0 | 9.5 | 1.78 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC1G06DRYR | SON | DRY | 6 | 5000 | 180.0 | 9.5 | 1.15 | 1.6 | 0.75 | 4.0 | 8.0 | Q1 |
| SN74LVC1G06DSFR | SON | DSF | 6 | 5000 | 180.0 | 9.5 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| SN74LVC1G06YZPR | DSBGA | YZP | 5 | 3000 | 178.0 | 9.2 | 1.02 | 1.52 | 0.63 | 4.0 | 8.0 | Q1 |
| SN74LVC1G06YZVR | DSBGA | YZV | 4 | 3000 | 178.0 | 9.2 | 1.0 | 1.0 | 0.63 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC1G06DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G06DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G06DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G06DBVR | SOT-23 | DBV | 5 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G06DBVRG4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G06DBVT | SOT-23 | DBV | 5 | 250 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G06DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G06DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G06DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G06DBVTG4 | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G06DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G06DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G06DCKR | SC70 | DCK | 5 | 3000 | 202.0 | 201.0 | 28.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC1G06DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G06DCKT | SC70 | DCK | 5 | 250 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G06DPWR | X2SON | DPW | 5 | 3000 | 205.0 | 200.0 | 33.0 |
| SN74LVC1G06DRLR | SOT-5X3 | DRL | 5 | 4000 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G06DRLR | SOT-5X3 | DRL | 5 | 4000 | 184.0 | 184.0 | 19.0 |
| SN74LVC1G06DRYR | SON | DRY | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74LVC1G06DSFR | SON | DSF | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74LVC1G06YZPR | DSBGA | YZP | 5 | 3000 | 220.0 | 220.0 | 35.0 |
| SN74LVC1G06YZVR | DSBGA | YZV | 4 | 3000 | 220.0 | 220.0 | 35.0 |

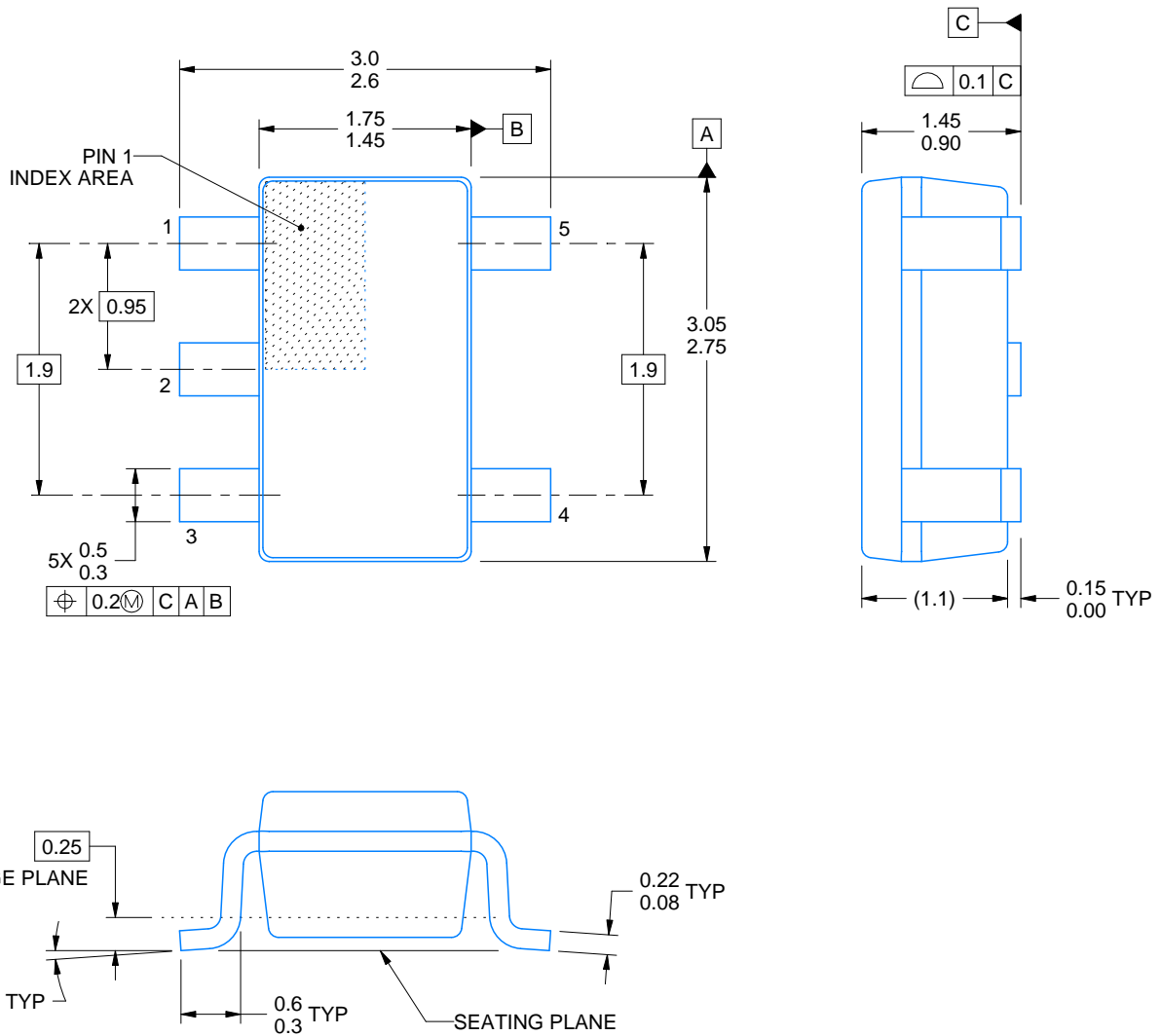
DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DPW 5

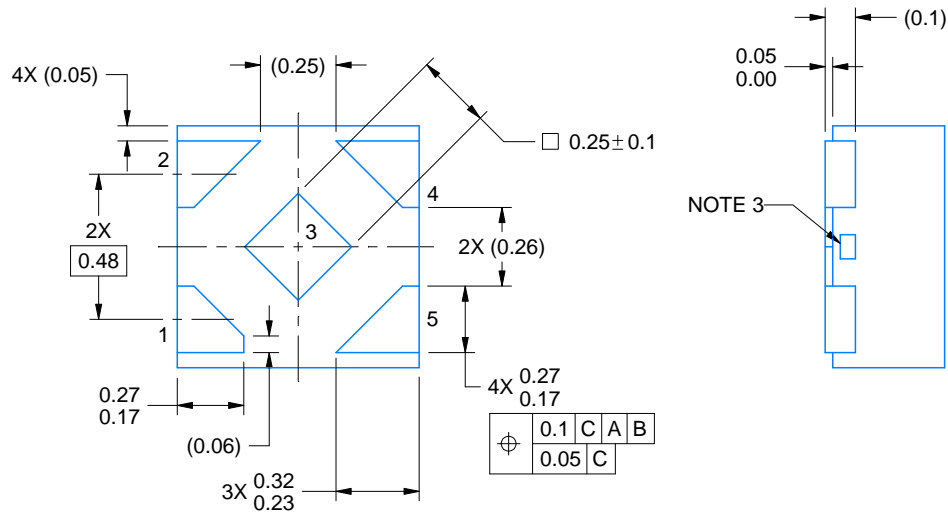
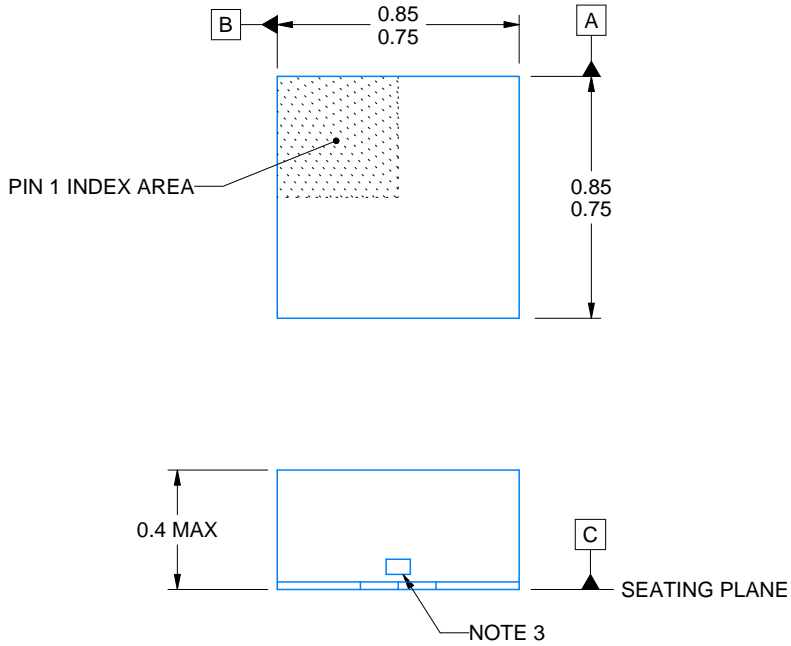
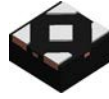
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4211218-3/D



4223102/B 09/2017

NOTES:

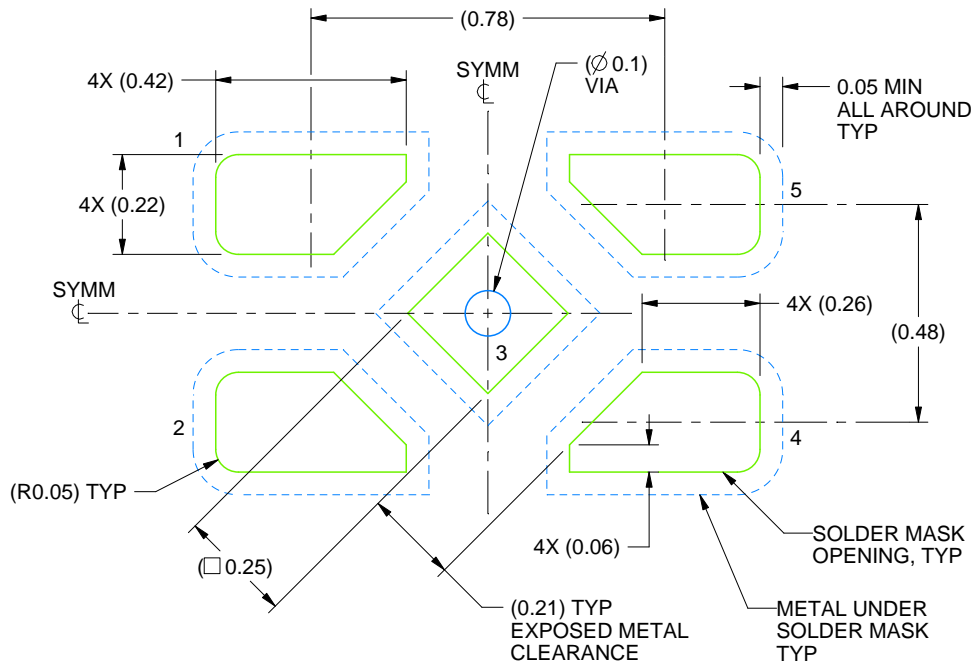
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

EXAMPLE BOARD LAYOUT

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/B 09/2017

NOTES: (continued)

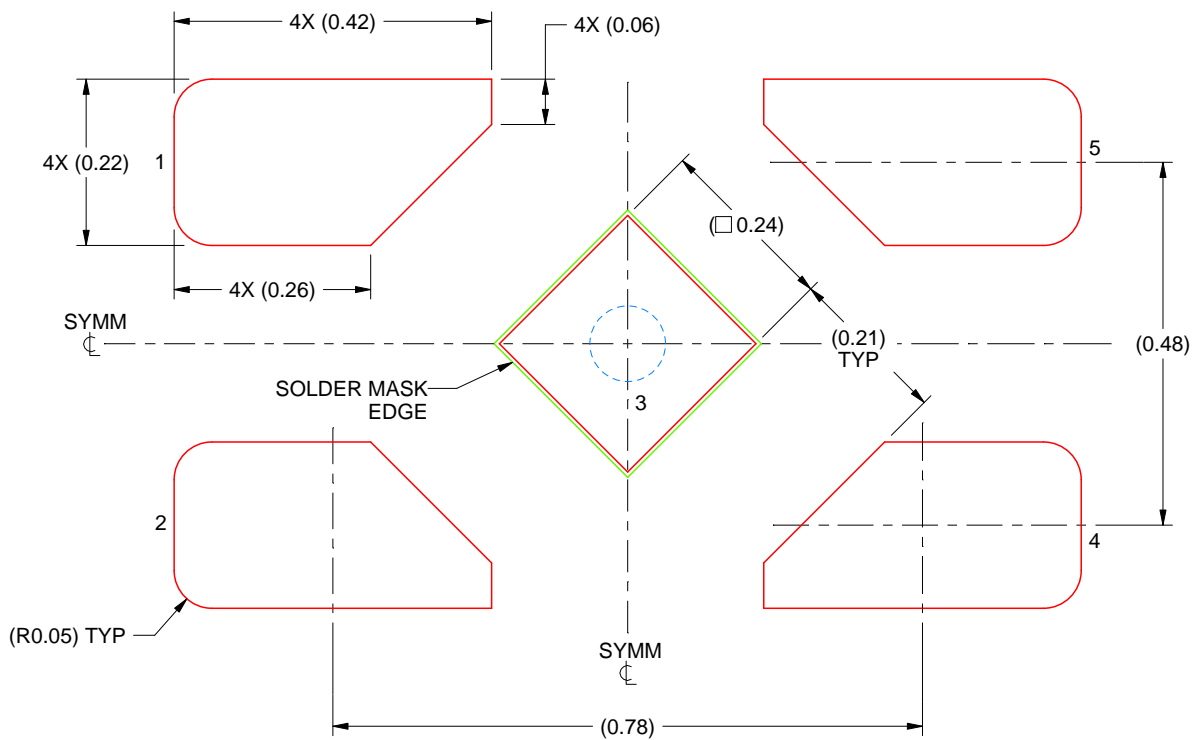
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
92% PRINTED SOLDER COVERAGE BY AREA
SCALE:100X

4223102/B 09/2017

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

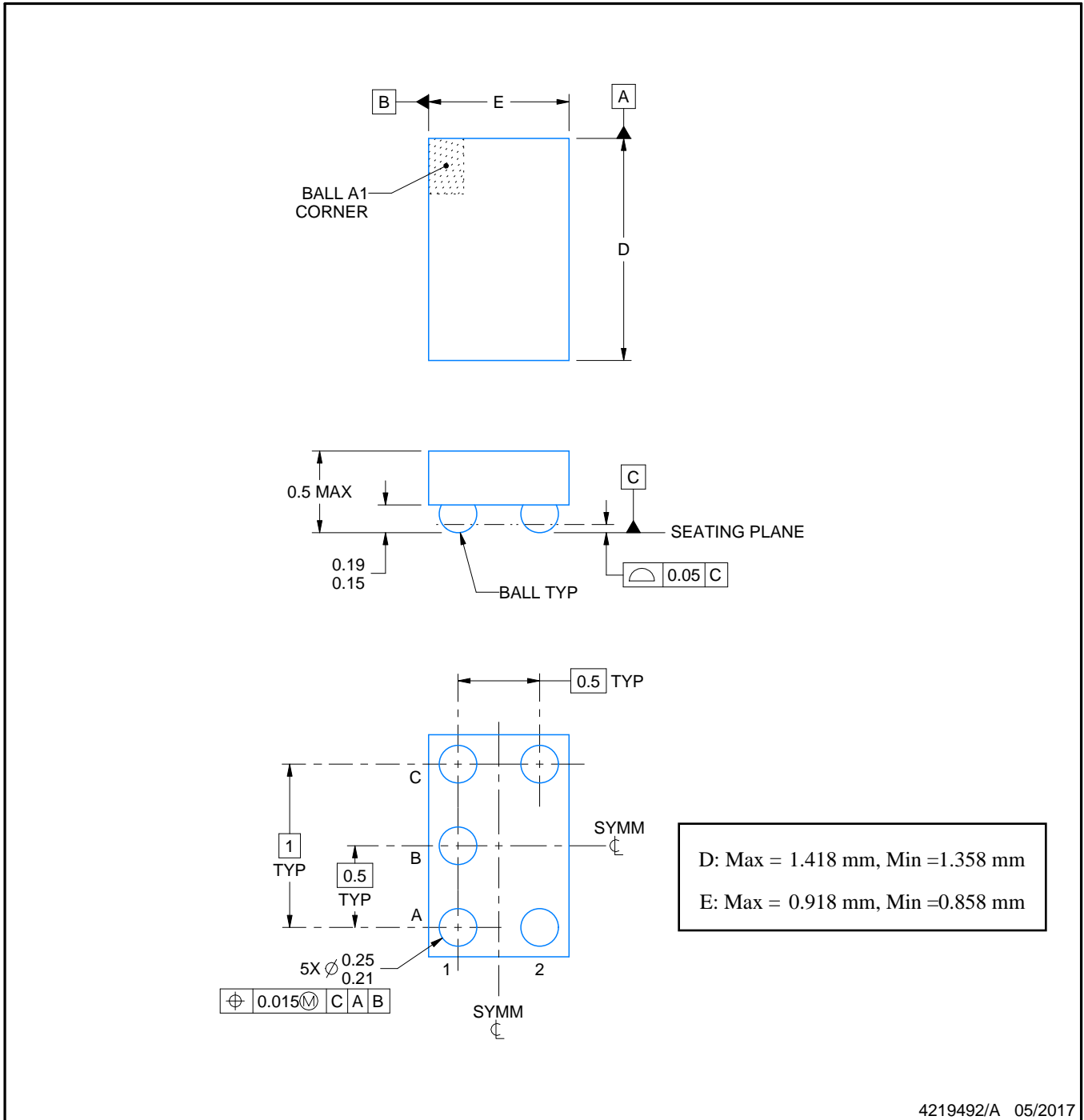
YZP0005



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4219492/A 05/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

YZV (S-XBGA-N4)

DIE-SIZE BALL GRID ARRAY

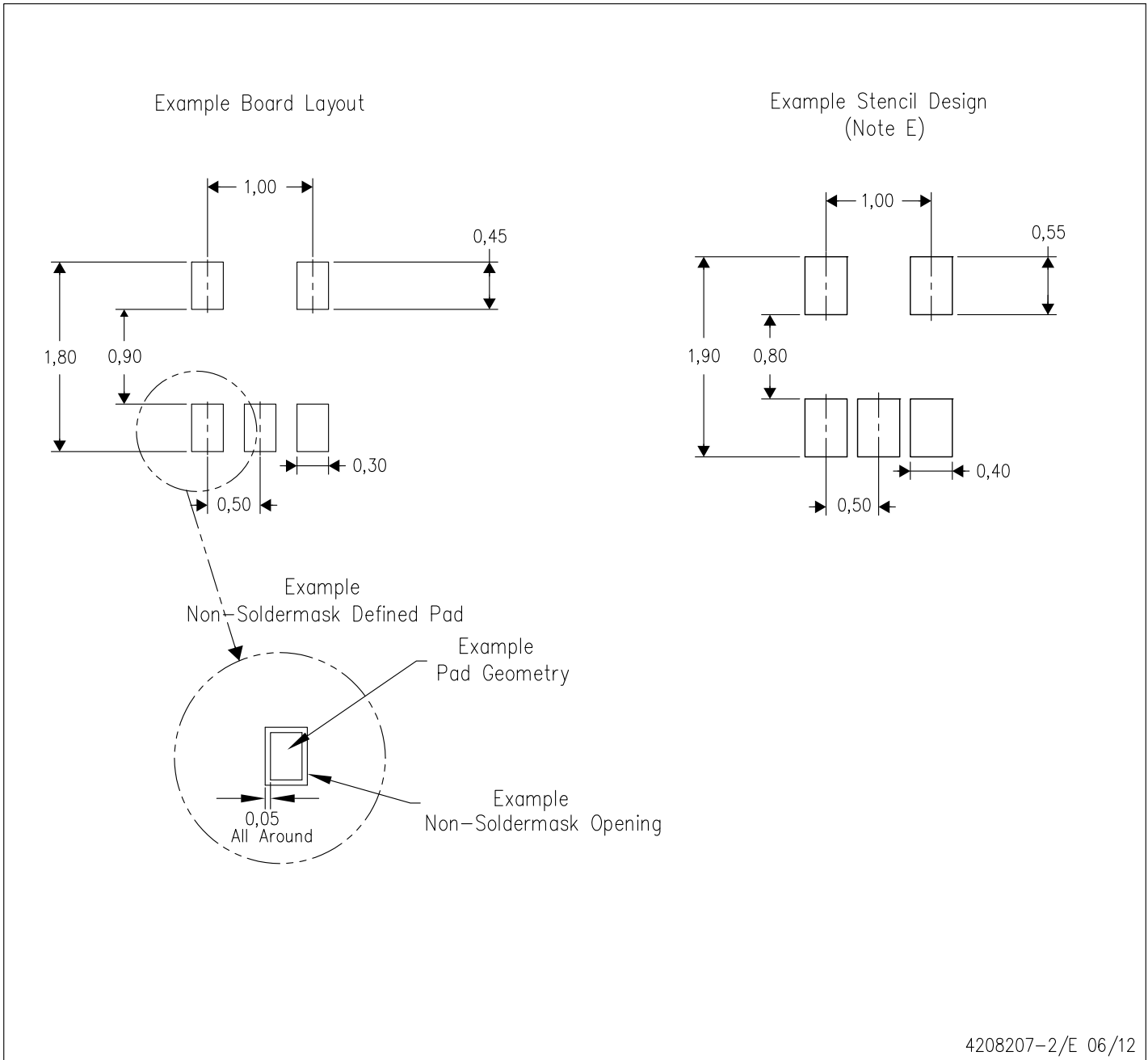


- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.

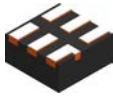
NanoFree is a trademark of Texas Instruments.



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
 - D. JEDEC package registration is pending.



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

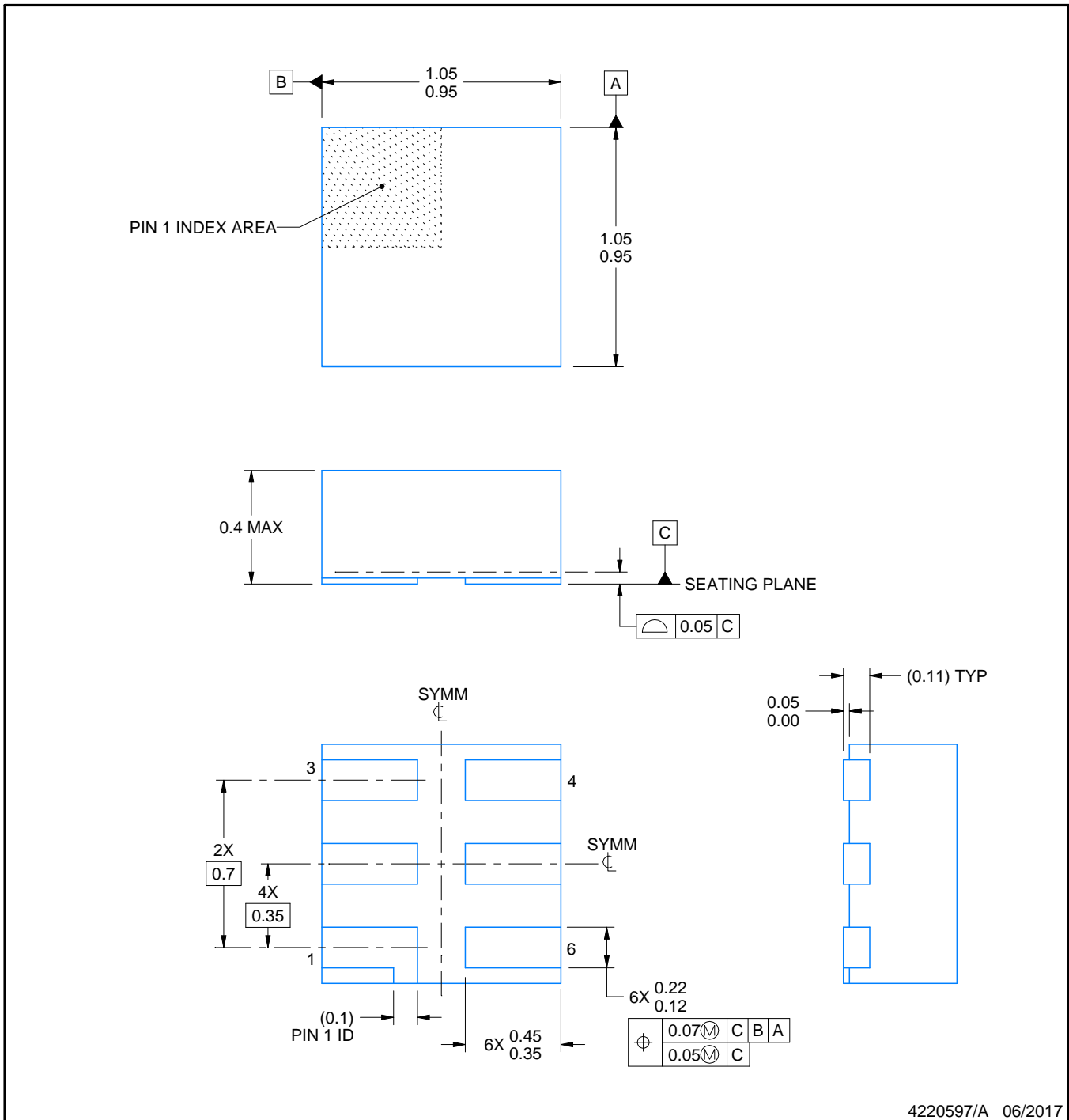


DSF0006A

PACKAGE OUTLINE

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

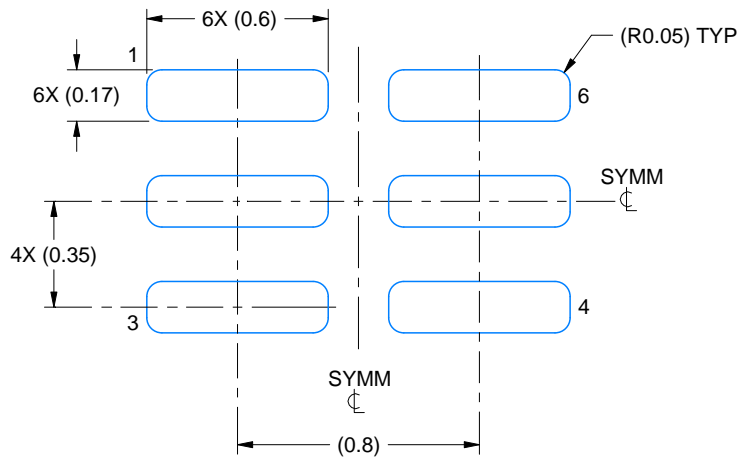
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

EXAMPLE BOARD LAYOUT

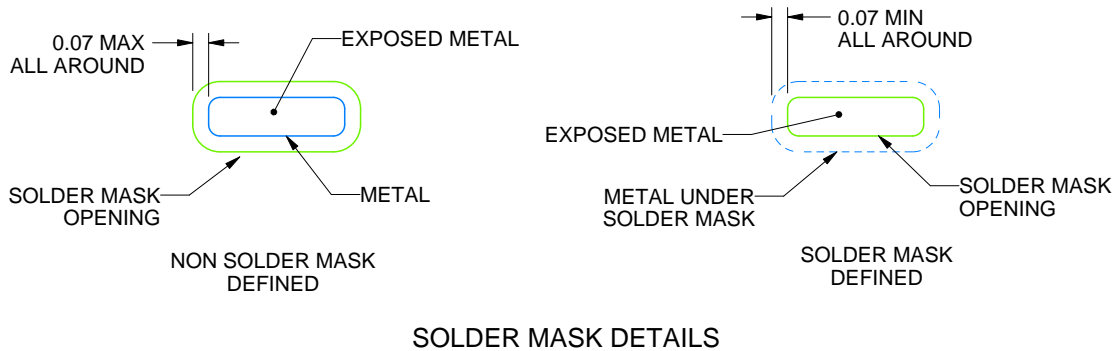
DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/A 06/2017

NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/A 06/2017

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

GENERIC PACKAGE VIEW

DRY 6

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4207181/G

DRY0006A



PACKAGE OUTLINE

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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