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August 2014
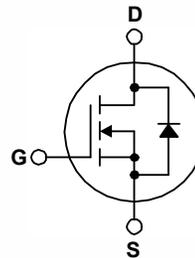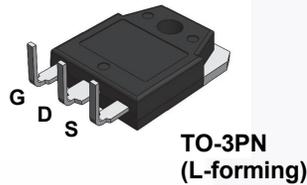
FDA16N50LDTU
N-Channel UniFET™ MOSFET
500 V, 16.5 A, 380 mΩ

Features

- $R_{DS(on)}$ = 310 mΩ (Typ.) @ V_{GS} = 10 V, I_D = 8.3 A
- Low Gate Charge (Typ. 32 nC)
- Low C_{rss} (Typ. 20 pF)
- 100% Avalanche Tested
- RoHS Compliant

Applications

- PDP TV
- Uninterruptible Power Supply

Description

UniFET™ MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

TO-3PN (L-forming)

MOSFET Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter			FDA16N50LDTU	Unit
V_{DSS}	Drain to Source Voltage			500	V
V_{GSS}	Gate to Source Voltage			±30	V
I_D	Drain Current	- Continuous (T_C = 25°C)		16.5	A
		- Continuous (T_C = 100°C)		9.9	
I_{DM}	Drain Current	- Pulsed	(Note 1)	66	A
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	780	mJ
I_{AR}	Avalanche Current		(Note 1)	16.5	A
E_{AR}	Repetitive Avalanche Energy		(Note 1)	20.5	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	4.5	V/ns
P_D	Power Dissipation	(T_C = 25°C)		205	W
		- Derate Above 25°C		2.1	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range			-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds			300	°C

Thermal Characteristics

Symbol	Parameter	FDA16N50LDTU	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDA16N50LDTU	FDA16N50	TO-3PN (L-forming)	Tube	N/A	N/A	30 units

Electrical Characteristics T_C = 25°C unless otherwise noted.

| Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0 V, T_J = 25°C	500	-	-	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C	-	0.50	-	V/^{o}C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500 V, V_{GS} = 0 V	-	-	20	µA
		V_{DS} = 500 V, T_C = 125°C	-	-	200	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±30 V, V_{DS} = 0 V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 µA	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 8.3 A	-	0.31	0.38	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 8.3 A	-	23	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	-	1495	1945	pF
C_{oss}	Output Capacitance		-	235	310	pF
C_{rss}	Reverse Transfer Capacitance		-	20	30	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DS} = 400 V, I_D = 16 A, V_{GS} = 10 V	-	32	45	nC
Q_{gs}	Gate to Source Gate Charge		-	8.5	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	(Note 4)	-	14	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 250 V, I_D = 16 A, V_{GS} = 10 V, R_G = 25 Ω	-	40	90	ns
t_r	Turn-On Rise Time		-	150	310	ns
$t_{d(off)}$	Turn-Off Delay Time		-	65	140	ns
t_f	Turn-Off Fall Time	(Note 4)	-	80	170	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	16.5	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	66	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 16.5 A	-	-	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 16 A, dI_F/dt = 100 A/µs	-	490	-	ns
Q_{rr}	Reverse Recovery Charge		-	5.0	-	µC

Notes:
1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. L = 5.1 mH, I_{AS} = 16.5 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 16.5 A, di/dt ≤ 200 A/µs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.
4. Essentially independent of operating temperature typical Characteristics

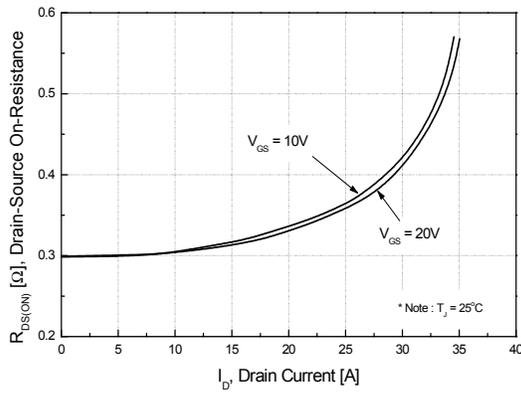## Typical Performance Characteristics

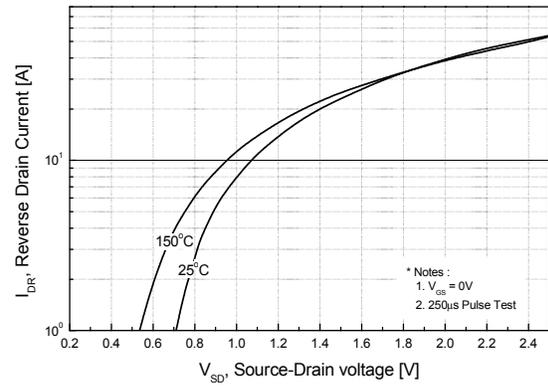**Figure 1. On-Region Characteristics**
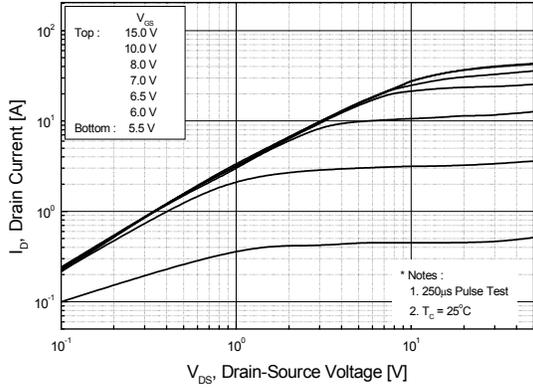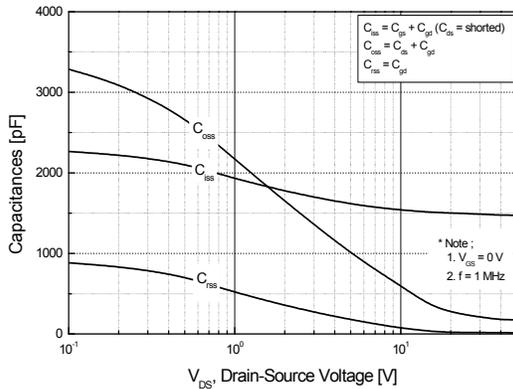

Figure 2. Transfer Characteristics
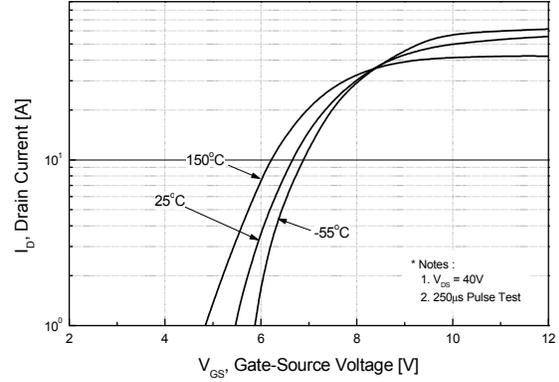
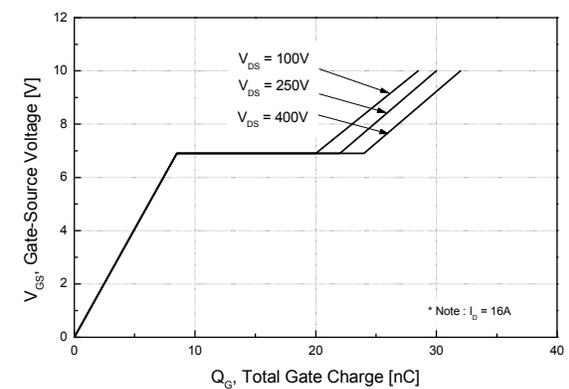**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**

Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue
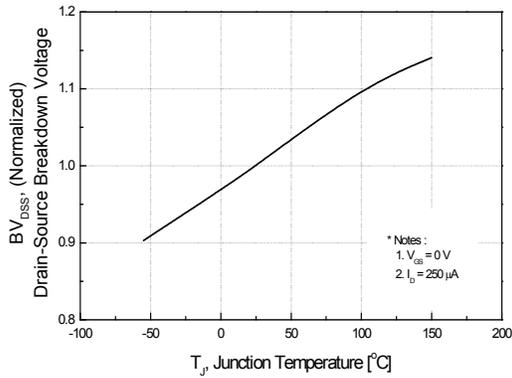

Figure 5. Capacitance Characteristics
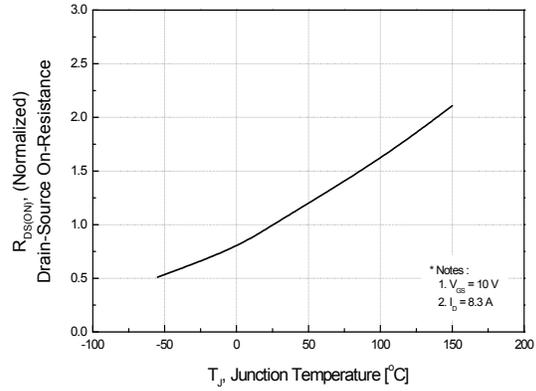

Figure 6. Gate Charge Characteristics
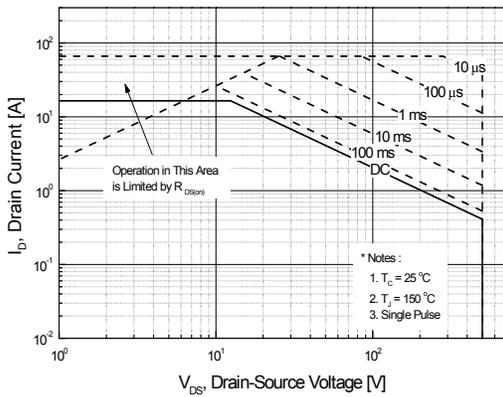
Typical Performance Characteristics (Continued)
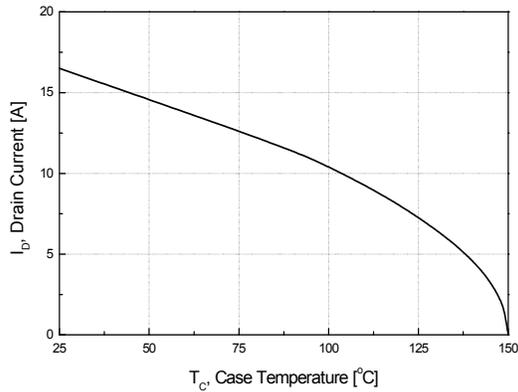
Figure 7. Breakdown Voltage Variation vs. Temperature

* Notes :
1. V_{GS} = 0 V
2. I_D = 250 μA

BV$_{DSS}$, (Normalized) Drain-Source Breakdown Voltage

T_J, Junction Temperature [°C]

Figure 8. On-Resistance Variation vs. Temperature

* Notes :
1. V_{GS} = 10 V
2. I_D = 8.3 A

R$_{DS(ON)}$, (Normalized) Drain-Source On-Resistance

T_J, Junction Temperature [°C]

Figure 9. Maximum Safe Operating Area

10 μs
100 μs
1 ms
10 ms
100 ms
DC

Operation in This Area is Limited by R$_{DS(on)}$

* Notes :
1. T_C = 25 °C
2. T_J = 150 °C
3. Single Pulse

I_D, Drain Current [A]

V_{DS}, Drain-Source Voltage [V]

Figure 10. Maximum Drain Current vs. Case Temperature

I_D, Drain Current [A]

T_C, Case Temperature [°C]

Figure 11. Transient Thermal Response Curve

D = 0.5
0.2
0.1
0.05
0.02
0.01

single pulse

P_{DM}
t_1
t_2

* Notes :
1. $Z_{\theta JC}(t)$ = 0.6 °C/W Max.
2. Duty Factor, D = t_1/t_2
3. $T_{JM} - T_C = P_{DM} * Z_{\theta JC}(t)$

$Z_{\theta JC}(t)$, Thermal Response [°C/W]

t1, Rectangular Pulse Duration [sec]

R_L

V_{GS}

V_{DS}

DUT

I_G = const.

V_{GS}

Q_g

Q_{gs} Q_{gd}
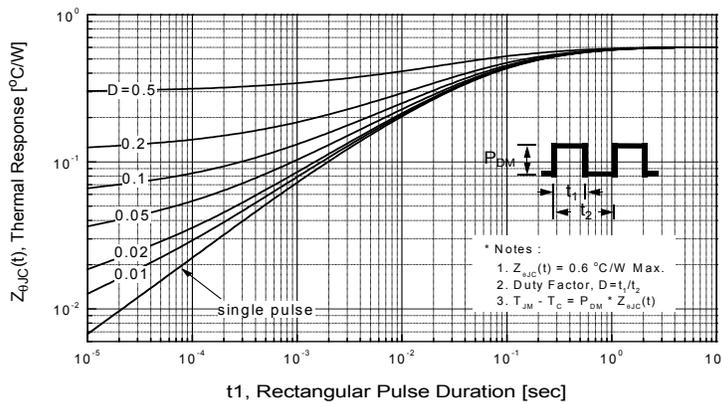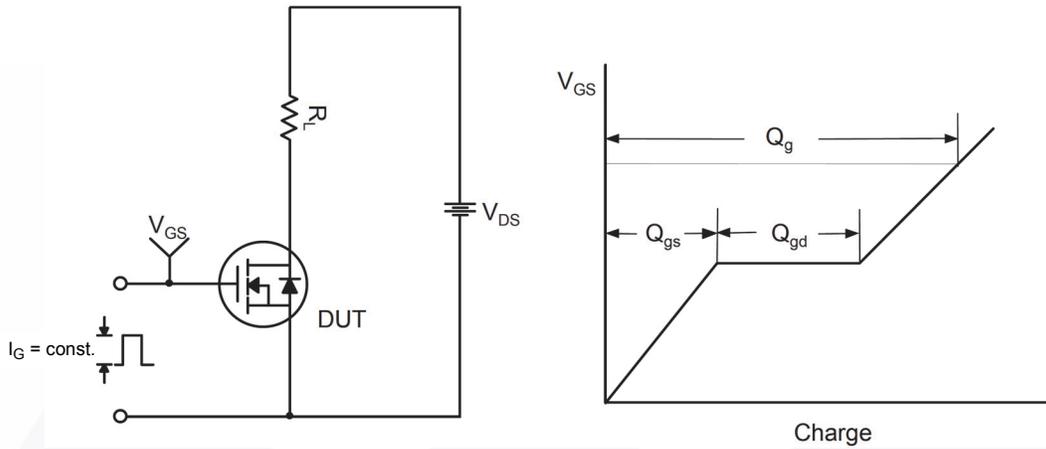
Charge

Figure 12. Gate Charge Test Circuit & Waveform

V_{DS} R_L

V_{GS}

V_{DD}

R_G

V_{GS}

DUT

V_{DS} 90%

V_{GS} 10%

$t_{d(on)}$ t_r $t_{d(off)}$ t_f

t_{on} t_{off}
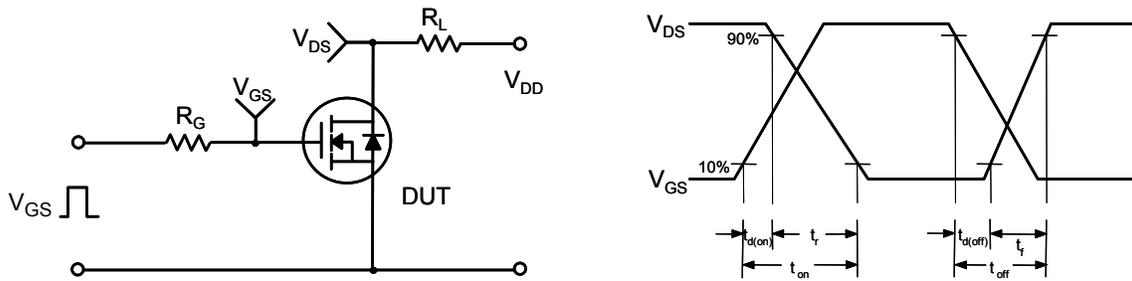
Figure 13. Resistive Switching Test Circuit & Waveforms

V_{DS} L

I_D

R_G

V_{DD}

V_{GS}

DUT

t_p

$$E_{AS} = \frac{1}{2} L I_{AS}^2 \ \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

BV_{DSS}

I_{AS}

$I_D (t)$

V_{DD}

$V_{DS} (t)$

t_p

Time
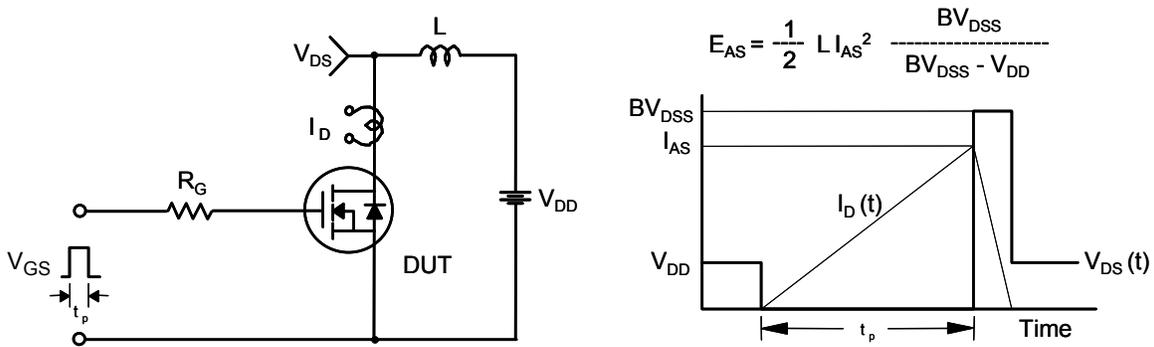
Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

DUT

V_{DS}

+

−

I_{SD}

L

Driver

R_G

Same Type
as DUT

V_{DD}

V_{GS}

• dv/dt controlled by R_G
• I_{SD} controlled by pulse period

V_{GS}
(Driver)

$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$

10V

I_{SD}
(DUT)

I_{FM} , Body Diode Forward Current

di/dt

I_{RM}

Body Diode Reverse Current

V_{DS}
(DUT)

Body Diode Recovery dv/dt

V_{SD}

V_{DD}

Body Diode
Forward Voltage Drop
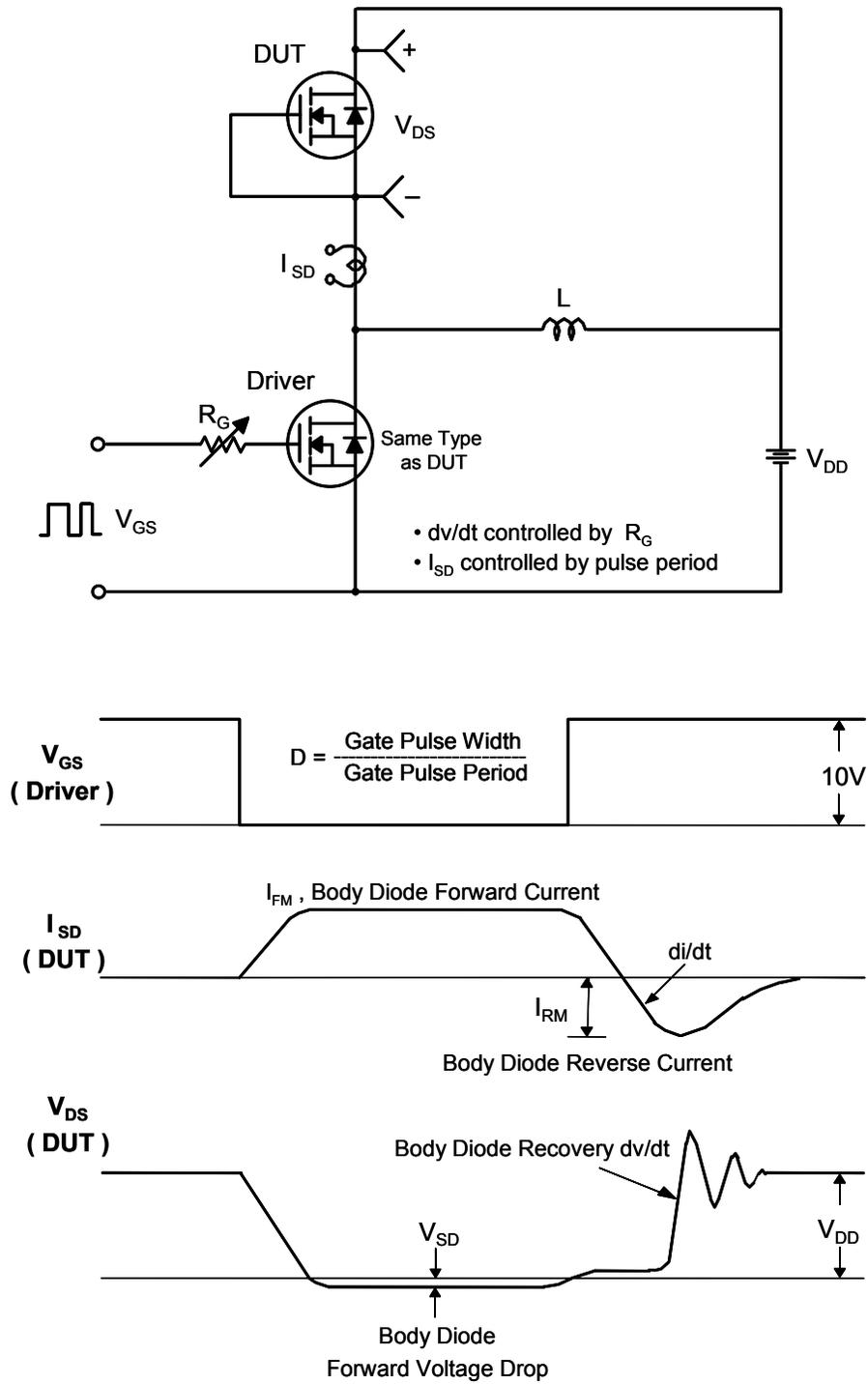
Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Front View

5.20 / 4.80

16.20 / 15.40

20.10 / 19.70

18.90 / 18.50

1   3

(1.85)

3.70 / 3.30

2.20 / 1.80

3.20 / 2.80

1.20 / 0.80

$\bigoplus$ | ϕ 0.55 Ⓜ

5.45   5.45

Side View

5.00 / 4.60

1.65 / 1.45

3°

△E 4.45 / 3.95

3°

△E 5.25 / 4.75

4°

(R0.60)

△E 9.25 / 8.75

0.75 / 0.55

Top View

13.80 / 13.40

ϕ 3.30 / 3.10

16.96 / 16.56

ϕ 7.20 / 6.80

(R0.50)
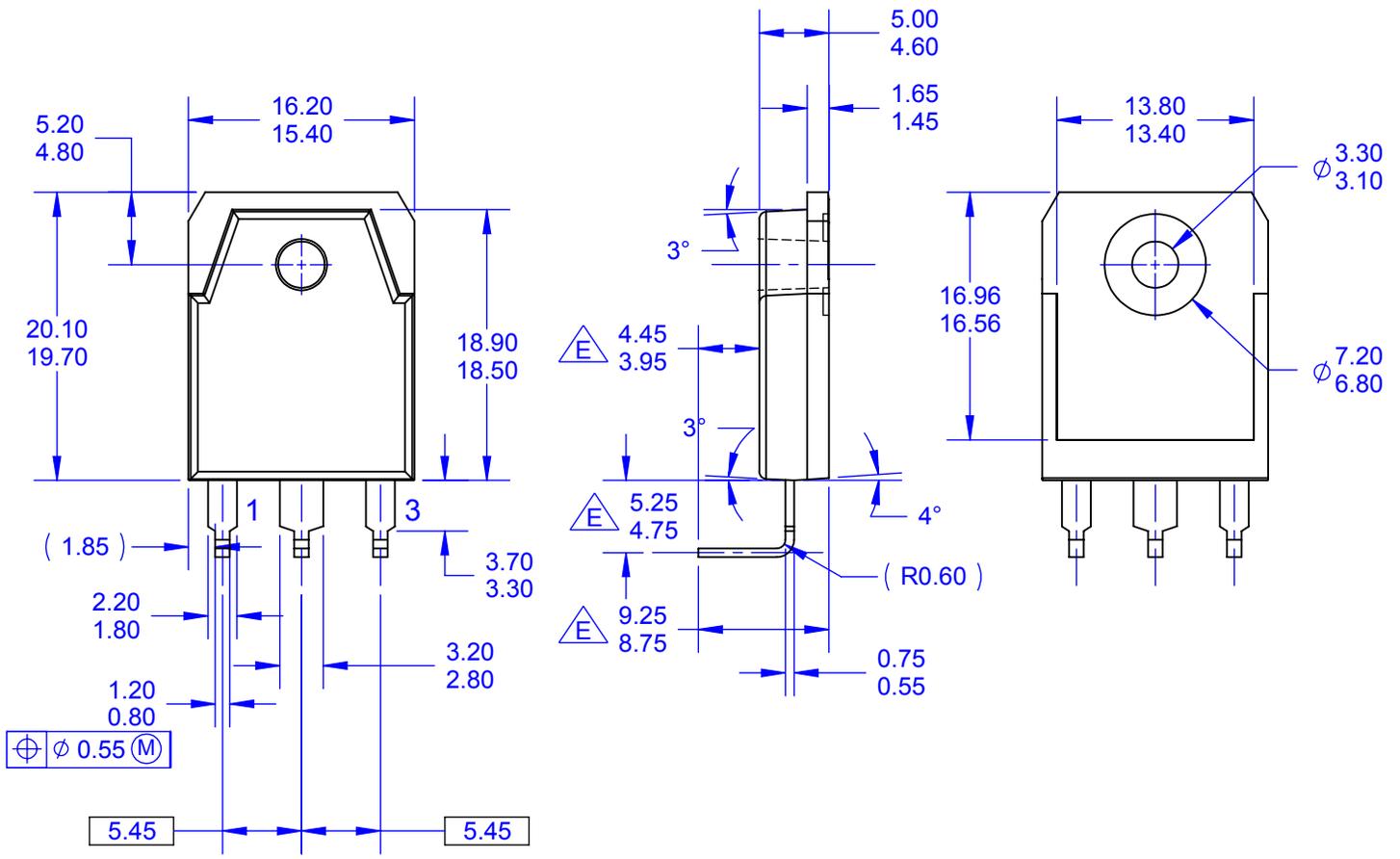
Notes

NOTES: UNLESS OTHERWISE SPECIFIED

A) PACKAGE REFERENCE EIAJ SC-65
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B) ALL DIMENSIONS ARE IN MILLIMETERS.
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   MOLD FLASH, AND TIE BAR EXTRUSSIONS.

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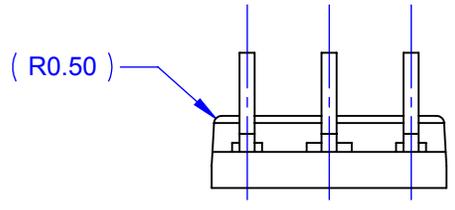
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