# CY62256N

# 256-Kbit (32 K × 8) Static RAM

## Features

- Temperature ranges
  - Commercial: 0 °C to +70 °C
  - Industrial: –40 °C to +85 °C
  - Automotive-A: –40 °C to +85 °C
  - Automotive-E: –40 °C to +125 °C
- High speed: 55 ns
- Voltage range: 4.5 V to 5.5 V operation
- Low active power
  - 275 mW (max)
- Low standby power (LL version)
  - 82.5 µW (max)
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ Features
- TTL-compatible inputs and outputs
- Automatic power-down when deselected
- CMOS for optimum speed and power
- Available in Pb-free and non Pb-free 28-pin (600-mil) PDIP, 28-pin (300-mil) narrow SOIC, 28-pin TSOP I, and 28-pin reverse TSOP I packages

## Functional Description

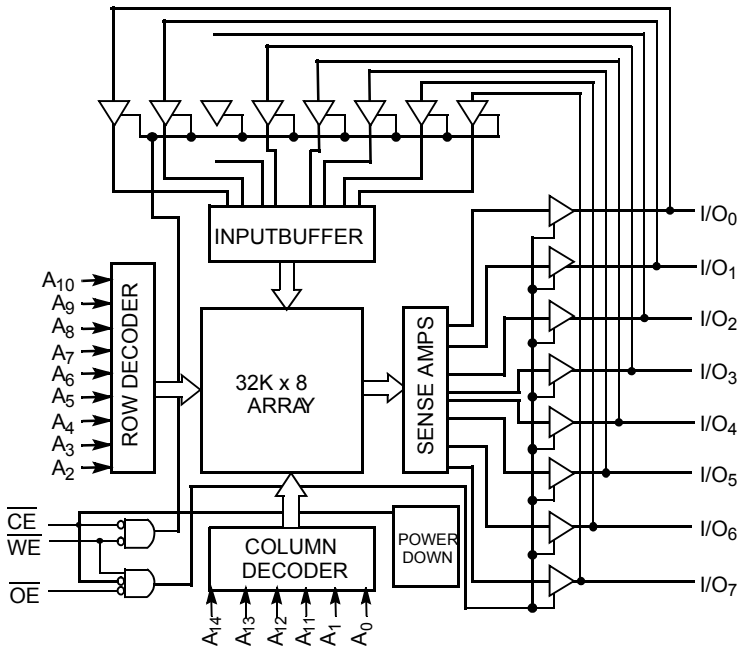
The CY62256N is a high performance CMOS static RAM organized as 32K words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and active LOW output enable ($\overline{OE}$) and tristate drivers. This device has an automatic power-down feature, reducing the power consumption by 99.9 percent when deselected.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins ($I/O_0$ through $I/O_7$) is written into the memory location addressed by the address present on the address pins ($A_0$ through $A_{14}$). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}$ and $\overline{OE}$ active LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input/output pins.

The input/output pins remain in a high impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

For a complete list of related documentation, click here.

## Logic Block Diagram



## Contents

## Product Portfolio

| Product | | $V_{CC}$ Range (V) | | | Speed (ns) | Power Dissipation | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Operating, $I_{CC}$ (mA) | | Standby, $I_{SB2}$ (µA) | |
| | | Min | Typ[1] | Max | | Typ[1] | Max | Typ[1] | Max |
| CY62256NLL | Commercial | 4.5 | 5.0 | 5.5 | 70 | 25 | 50 | 0.1 | 5 |
| CY62256NLL | Industrial | | | | 55/70 | 25 | 50 | 0.1 | 10 |
| CY62256NLL | Automotive-A | | | | 55/70 | 25 | 50 | 0.1 | 10 |
| CY62256NLL | Automotive-E | | | | 55 | 25 | 50 | 0.1 | 15 |

## Pin Configurations

**Figure 1. 28-pin DIP and Narrow SOIC pinout**

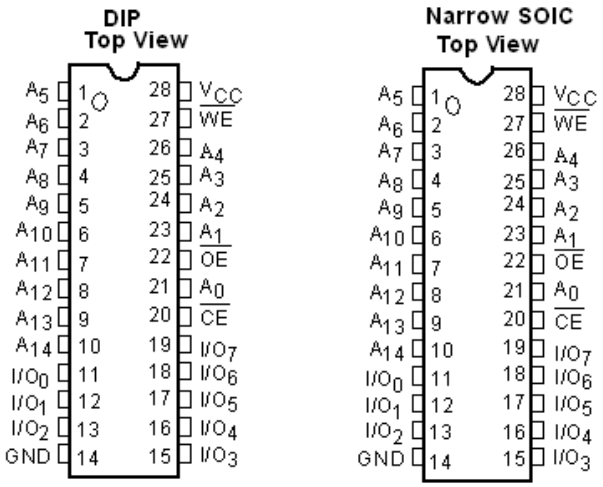
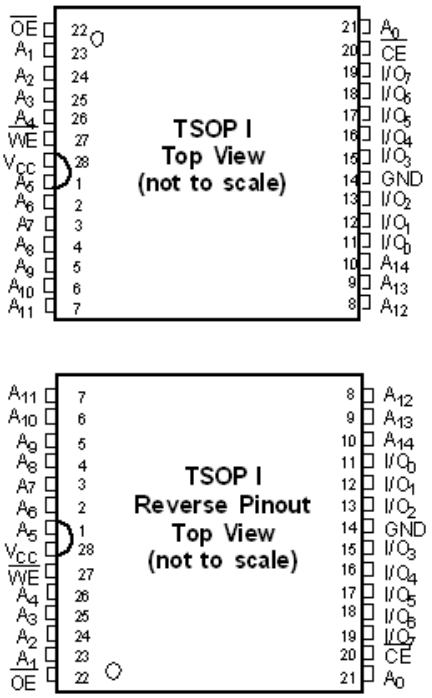



**Figure 2. 28-pin TSOP I and Reverse TSOP I pinout**




## Pin Definitions

| Pin Number | Type | Description |
|---|---|---|
| 1–10, 21, 23–26 | Input | **$A_0$–$A_{14}$**. Address Inputs |
| 11–13, 15–19, | Input/Output | **$I/O_0$–$I/O_7$**. Data lines. Used as input or output lines depending on operation |
| 27 | Input/Control | **WE**. When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted |
| 20 | Input/Control | **$\overline{CE}$**. When LOW, selects the chip. When HIGH, deselects the chip |
| 22 | Input/Control | **$\overline{OE}$**. Output Enable. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pins |
| 14 | Ground | **GND**. Ground for the device |
| 28 | Power Supply | **$V_{CC}$**. Power supply for the device |

**Note**
1. Typical specifications are the mean values measured over a large sample size across normal production process variations and are taken at nominal conditions ($T_A$ = 25 °C, $V_{CC}$). Parameters are guaranteed by design and characterization, and not 100% tested.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage to ground potential (pin 28 to pin 14) [2] .....–0.5 V to +7.0 V

DC voltage applied to outputs in high Z State [2] .....–0.5 V to $V_{CC}$ + 0.5 V

DC input voltage [2] .....–0.5 V to $V_{CC}$ + 0.5 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL-STD-883, method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

## Operating Range

| Range | Ambient Temperature ($T_A$) [3] | $V_{CC}$ |
|---|---|---|
| Commercial | 0 °C to +70 °C | 5 V ± 10% |
| Industrial | –40 °C to +85 °C | 5 V ± 10% |
| Automotive-A | –40 °C to +85 °C | 5 V ± 10% |
| Automotive-E | –40 °C to +125 °C | 5 V ± 10% |

## Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | | -55 | | | -70 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ [4] | Max | Min | Typ [4] | Max | |
| $V_{OH}$ | Output HIGH voltage | $V_{CC}$ = Min, $I_{OH}$ = –1.0 mA | | 2.4 | – | – | 2.4 | – | – | V |
| $V_{OL}$ | Output LOW voltage | $V_{CC}$ = Min, $I_{OL}$ = 2.1 mA | | – | – | 0.4 | – | – | 0.4 | V |
| $V_{IH}$ | Input HIGH voltage | | | 2.2 | – | $V_{CC}$ + 0.5 | 2.2 | – | $V_{CC}$ + 0.5 | V |
| $V_{IL}$ | Input LOW voltage | | | –0.5 | – | 0.8 | –0.5 | – | 0.8 | V |
| $I_{IX}$ | Input leakage current | GND ≤ $V_I$ ≤ $V_{CC}$ | | –0.5 | – | +0.5 | –0.5 | – | +0.5 | µA |
| $I_{OZ}$ | Output leakage current | GND ≤ $V_O$ ≤ $V_{CC}$, output disabled | | –0.5 | – | +0.5 | –0.5 | – | +0.5 | µA |
| $I_{CC}$ | $V_{CC}$ operating supply current | $V_{CC}$ = Max, $I_{OUT}$ = 0 mA, f = $f_{MAX}$ = $1/t_{RC}$ | LL - Commercial | – | – | – | – | 25 | 50 | mA |
| | | | LL - Industrial | – | 25 | 50 | – | 25 | 50 | mA |
| | | | LL - Automotive-A | – | 25 | 50 | – | 25 | 50 | mA |
| | | | LL - Automotive-E | – | 25 | 50 | – | – | – | mA |
| $I_{SB1}$ | Automatic CE power-down current – TTL inputs | Max. $V_{CC}$, $\overline{CE}$ ≥ $V_{IH}$, $V_{IN}$ ≥ $V_{IH}$ or $V_{IN}$ ≤ $V_{IL}$, f = $f_{MAX}$ | LL - Commercial | – | – | – | – | 0.3 | 0.5 | mA |
| | | | LL - Industrial | – | 0.3 | 0.5 | – | 0.3 | 0.5 | mA |
| | | | LL - Automotive-A | – | 0.3 | 0.5 | – | 0.3 | 0.5 | mA |
| | | | LL - Automotive-E | – | 0.3 | 0.5 | – | – | – | mA |
| $I_{SB2}$ | Automatic CE power-down current – CMOS inputs | Max. $V_{CC}$, $\overline{CE}$ ≥ $V_{CC}$ – 0.3 V, $V_{IN}$ ≥ $V_{CC}$ – 0.3 V, or $V_{IN}$ ≤ 0.3 V, f = 0 | LL - Commercial | – | – | – | – | 0.1 | 5 | µA |
| | | | LL - Industrial | – | 0.1 | 10 | – | 0.1 | 10 | µA |
| | | | LL - Automotive-A | – | 0.1 | 10 | – | 0.1 | 10 | µA |
| | | | LL - Automotive-E | – | 0.1 | 15 | – | – | – | µA |

**Notes**

2. $V_{IL}$ (min) = –2.0 V for pulse durations of less than 20 ns.
3. $T_A$ is the "Instant-On" case temperature.
4. Typical specifications are the mean values measured over a large sample size across normal production process variations and are taken at nominal conditions ($T_A$ = 25 °C, $V_{CC}$). Parameters are guaranteed by design and characterization, and not 100% tested.

## Capacitance

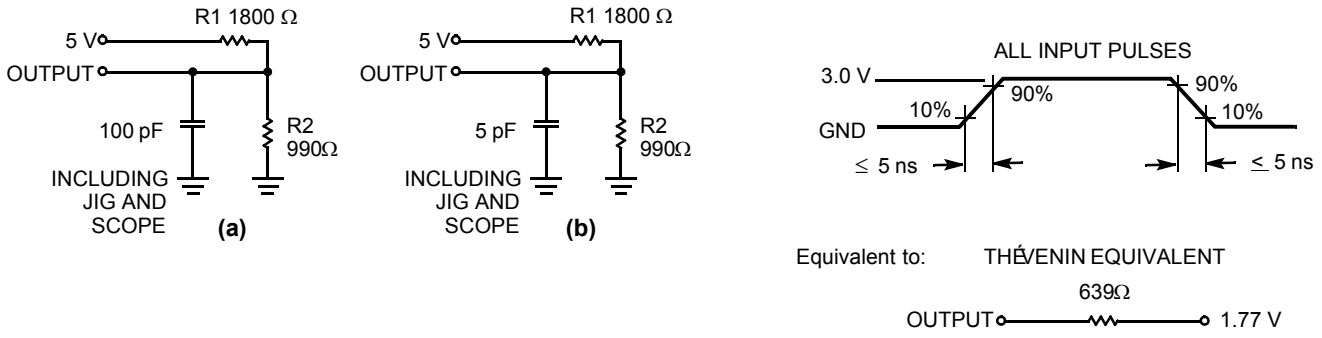
| Parameter [5] | Description | Test Conditions | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $T_A$ = 25 °C, f = 1 MHz, $V_{CC}$ = 5.0 V | 6 | pF |
| $C_{OUT}$ | Output capacitance | | 8 | pF |

## Thermal Resistance

| Parameter [5] | Description | Test Conditions | DIP | SOIC | TSOP | RTSOP | Unit |
|---|---|---|---|---|---|---|---|
| $\theta_{JA}$ | Thermal resistance (junction to ambient) | Still air, soldered on a 4.25 × 1.125 inch, 4-layer printed circuit board | 75.61 | 76.56 | 93.89 | 93.89 | °C/W |
| $\theta_{JC}$ | Thermal resistance (junction to case) | | 43.12 | 36.07 | 24.64 | 24.64 | °C/W |

## AC Test Loads and Waveforms

**Figure 3. AC Test Loads and Waveforms**



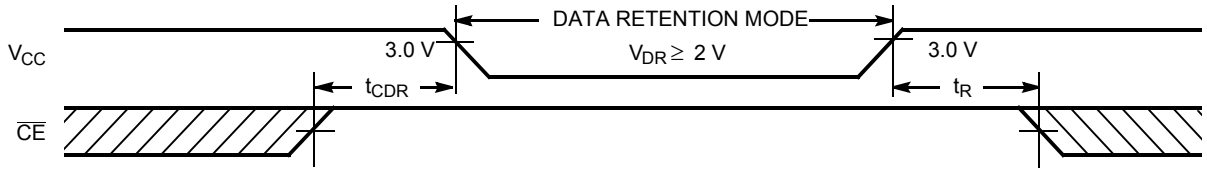

**Note**
5. Tested initially and after any design or process changes that may affect these parameters.

## Data Retention Characteristics

| Parameter | Description | | Conditions [6] | Min | Typ [7] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for data retention | | | 2.0 | – | – | V |
| $I_{CCDR}$ | Data retention current | LL – Commercial | $V_{CC}$ = 2.0 V, $\overline{CE} \geq V_{CC} - 0.3$ V, $V_{IN} \geq V_{CC} - 0.3$ V, or $V_{IN} \leq 0.3$ V | – | 0.1 | 5 | µA |
| | | LL – Industrial/ Automotive-A | | – | 0.1 | 10 | µA |
| | | LL – Automotive-E | | – | 0.1 | 10 | µA |
| $t_{CDR}$[7] | Chip deselect to data retention time | | | 0 | – | – | ns |
| $t_R$[7] | Operation recovery time | | CY62256NLL-55 | 55 | – | – | ns |
| | | | CY62256NLL-70 | 70 | – | – | |

## Data Retention Waveform

**Figure 4. Data Retention Waveform**




**Notes**
6. No input may exceed $V_{CC}$ + 0.5 V.
7. Typical specifications are the mean values measured over a large sample size across normal production process variations and are taken at nominal conditions ($T_A$ = 25 °C, $V_{CC}$). Parameters are guaranteed by design and characterization, and not 100% tested.

## Switching Characteristics

Over the Operating Range

| Parameter [8] | Description | CY62256N-55 | | CY62256N-70 | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| **Read Cycle** | | | | | | |
| $t_{RC}$ | Read cycle time | 55 | – | 70 | – | ns |
| $t_{AA}$ | Address to data valid | – | 55 | – | 70 | ns |
| $t_{OHA}$ | Data hold from address change | 5 | – | 5 | – | ns |
| $t_{ACE}$ | $\overline{CE}$ LOW to data valid | – | 55 | – | 70 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to data valid | – | 25 | – | 35 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to low Z [9] | 5 | – | 5 | – | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to high Z [9, 10] | – | 20 | – | 25 | ns |
| $t_{LZCE}$ | $\overline{CE}$ LOW to low Z [9] | 5 | – | 5 | – | ns |
| $t_{HZCE}$ | $\overline{CE}$ HIGH to high Z [9, 10] | – | 20 | – | 25 | ns |
| $t_{PU}$ | $\overline{CE}$ LOW to power-up | 0 | – | 0 | – | ns |
| $t_{PD}$ | $\overline{CE}$ HIGH to power-down | – | 55 | – | 70 | ns |
| **Write Cycle** [11, 12] | | | | | | |
| $t_{WC}$ | Write cycle time | 55 | – | 70 | – | ns |
| $t_{SCE}$ | $\overline{CE}$ LOW to write end | 45 | – | 60 | – | ns |
| $t_{AW}$ | Address setup to write end | 45 | – | 60 | – | ns |
| $t_{HA}$ | Address hold from write end | 0 | – | 0 | – | ns |
| $t_{SA}$ | Address setup to write start | 0 | – | 0 | – | ns |
| $t_{PWE}$ | $\overline{WE}$ pulse width | 40 | – | 50 | – | ns |
| $t_{SD}$ | Data setup to write end | 25 | – | 30 | – | ns |
| $t_{HD}$ | Data hold from write end | 0 | – | 0 | – | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to high Z [9, 10] | – | 20 | – | 25 | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to low Z [9] | 5 | – | 5 | – | ns |

**Notes**

8. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified $I_{OL}/I_{OH}$ and 100-pF load capacitance.
9. At any temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$, $t_{HZOE}$ is less than $t_{LZOE}$, and $t_{HZWE}$ is less than $t_{LZWE}$ for any device.
10. $t_{HZOE}$, $t_{HZCE}$, and $t_{HZWE}$ are specified with $C_L$ = 5 pF as in (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
11. The internal Write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a Write and either signal can terminate a Write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the Write.
12. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) is the sum of $t_{HZWE}$ and $t_{SD}$.

## Switching Waveforms

**Figure 5. Read Cycle No. 1** [13, 14]

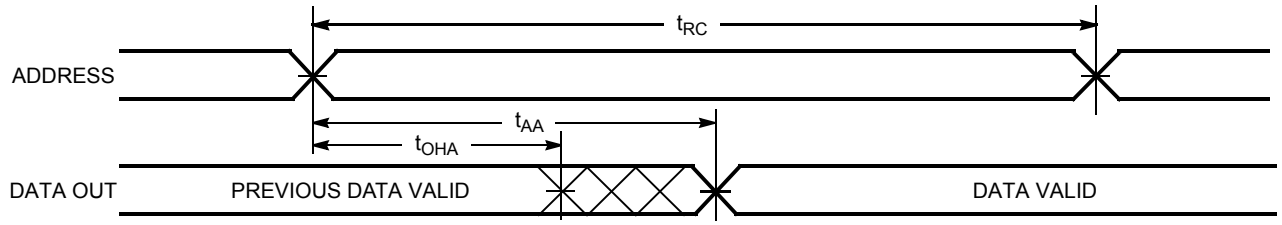
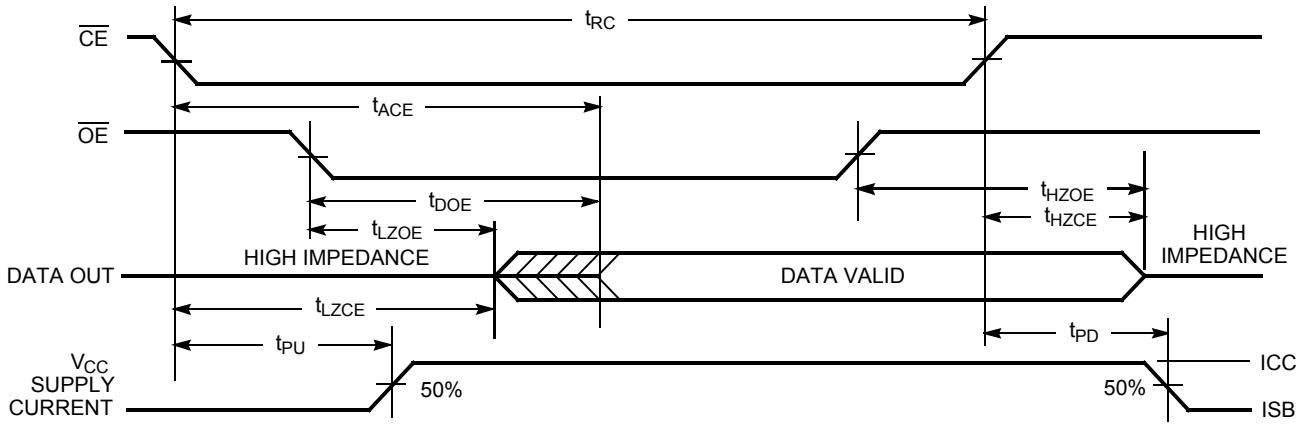



**Figure 6. Read Cycle No. 2** [14, 15]




**Notes**
13. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = $V_{IL}$.
14. $\overline{WE}$ is HIGH for Read cycle.
15. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

## Switching Waveforms *(continued)*

**Figure 7. Write Cycle No. 1 ($\overline{WE}$ Controlled)** [16, 17, 18]

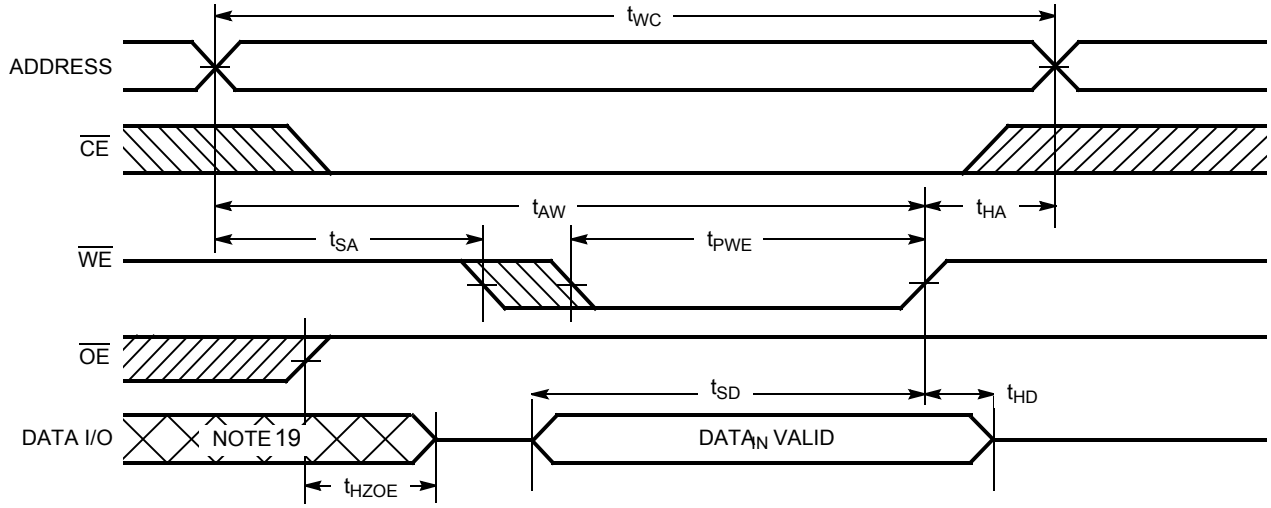



**Figure 8. Write Cycle No. 2 ($\overline{CE}$ Controlled)** [16, 17, 18]

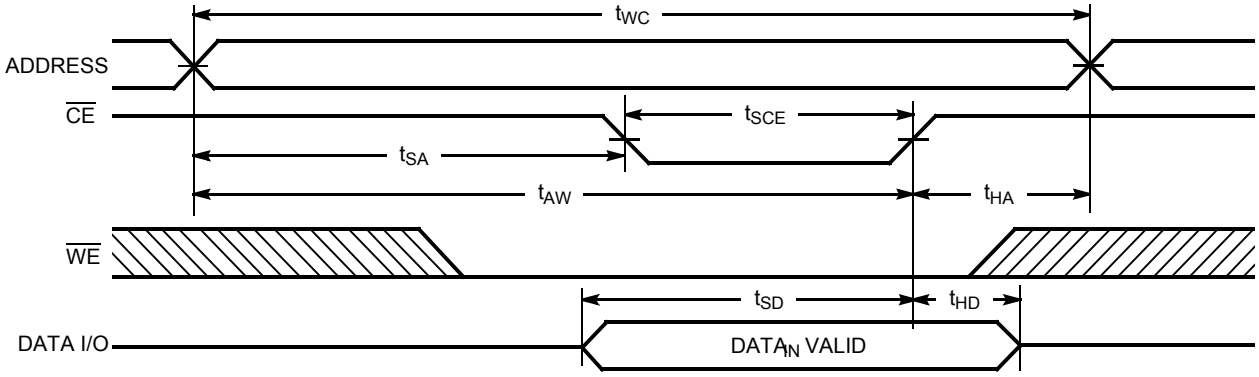
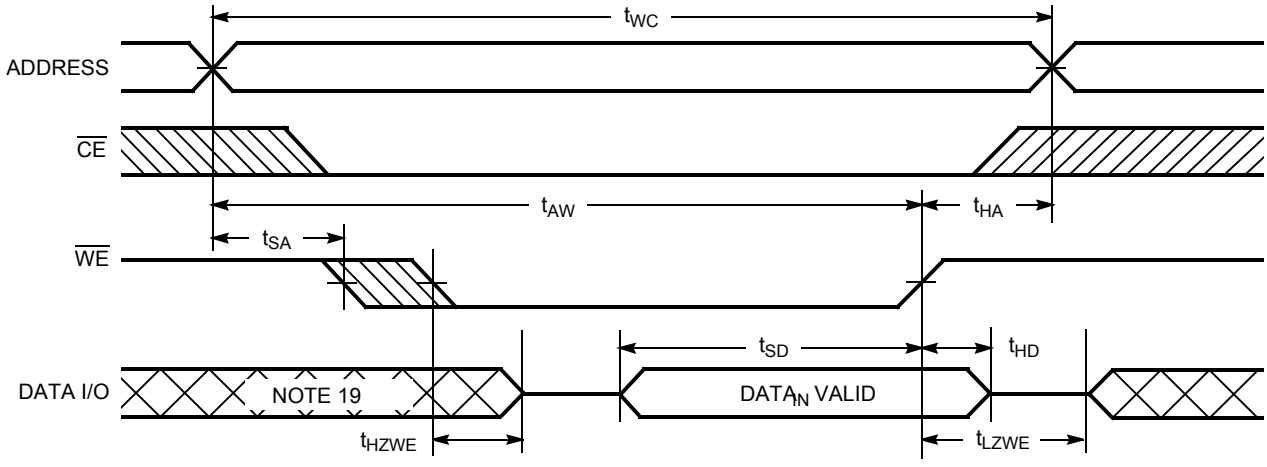



**Figure 9. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)** [18, 20]

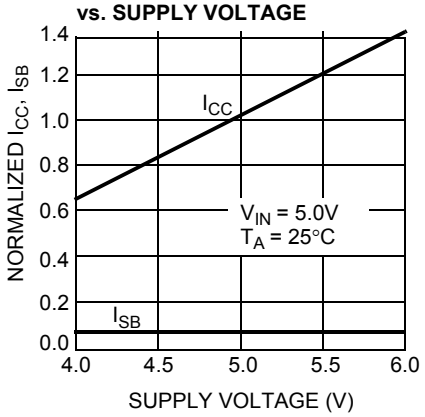



**Notes**

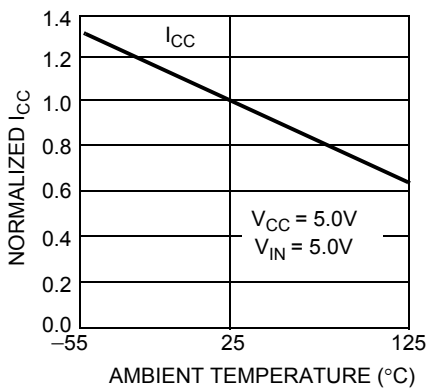
16. The internal Write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a Write and either signal can terminate a Write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the Write.
17. Data I/O is high impedance if $\overline{OE}$ = $V_{IH}$.
18. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
19. During this period, the I/Os are in output state and input signals should not be applied.
20. The minimum write cycle pulse width should be equal to the sum of $t_{SD}$ and $t_{HZWE}$.

## Typical DC and AC Characteristics

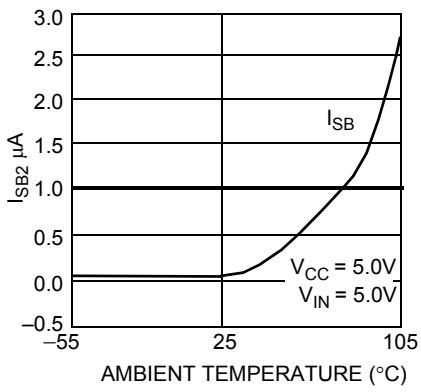
**NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE**



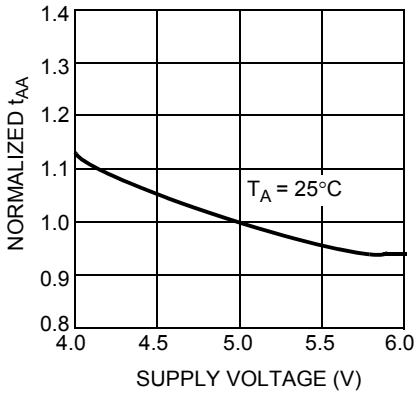

**NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE**



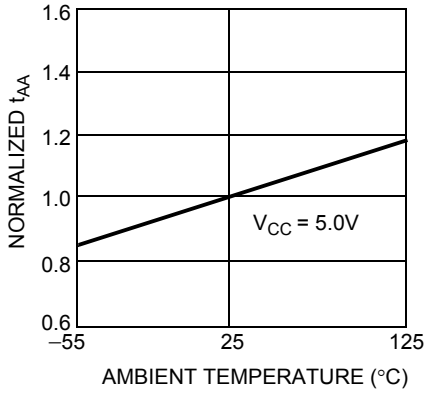

**STANDBY CURRENT vs. AMBIENT TEMPERATURE**



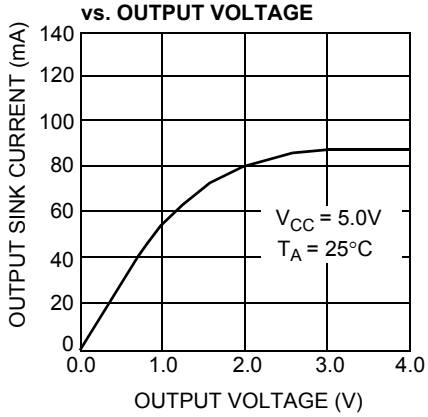

**NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE**



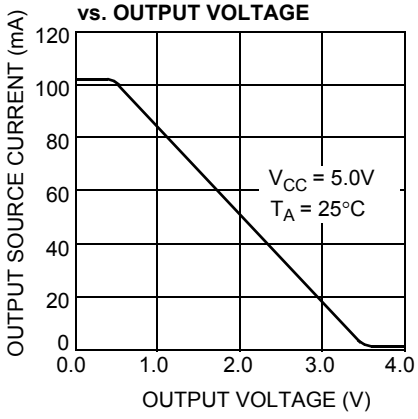

**NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE**




**OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE**

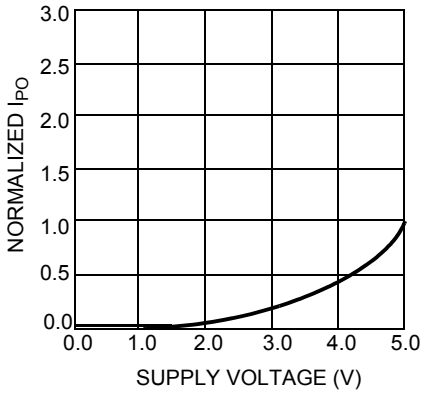



**OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE**

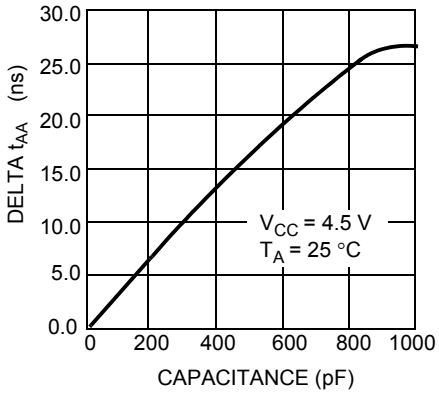


## Typical DC and AC Characteristics *(continued)*

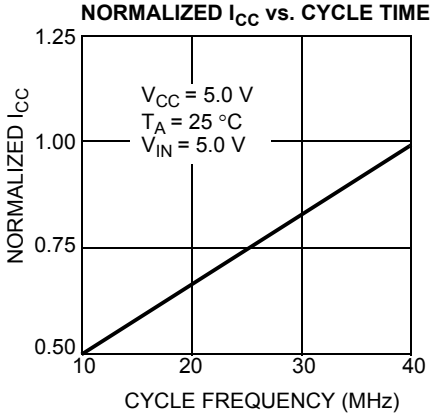
**TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE**




**TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING**




**NORMALIZED $I_{CC}$ vs. CYCLE TIME**



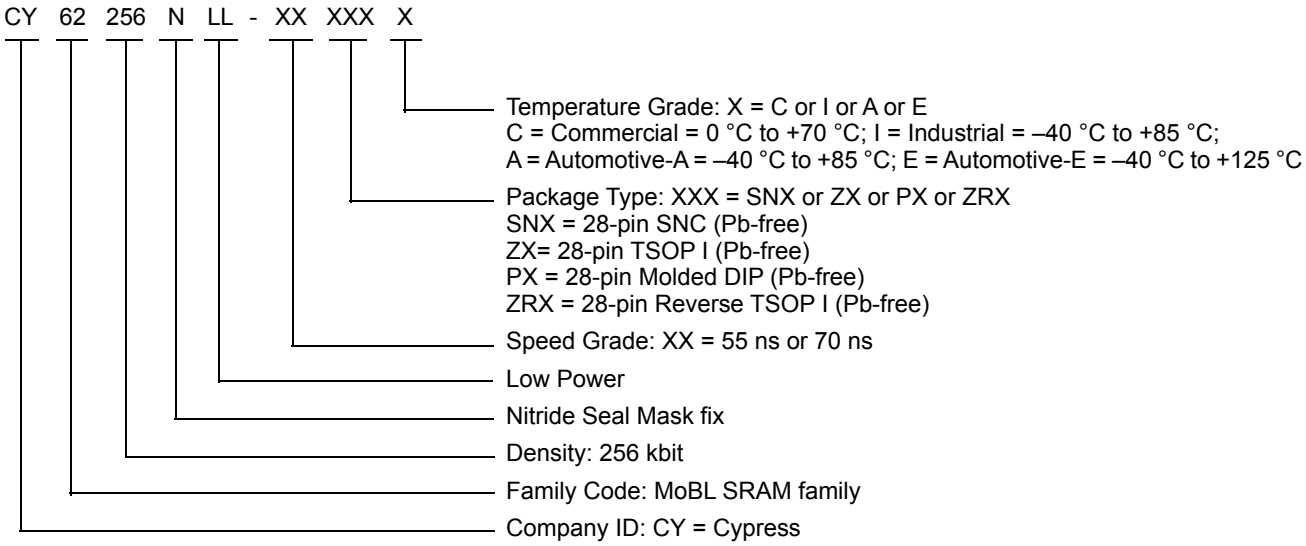

## Truth Table

| $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | Inputs/Outputs | Mode | Power |
|---|---|---|---|---|---|
| H | X | X | High Z | Deselect/power-down | Standby ($I_{SB}$) |
| L | H | L | Data Out | Read | Active ($I_{CC}$) |
| L | L | X | Data In | Write | Active ($I_{CC}$) |
| L | H | H | High Z | Output Disabled | Active ($I_{CC}$) |

## Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 55 | CY62256NLL–55SNXI | 51-85092 | 28-pin SNC (300 Mils) Narrow Body (Pb-free) | Industrial |
| | CY62256NLL–55ZXI | 51-85071 | 28-pin TSOP I (Pb-free) | |
| | CY62256NLL–55ZXA | 51-85071 | 28-pin TSOP I (Pb-free) | Automotive-A |
| | CY62256NLL–55SNXE | 51-85092 | 28-pin SNC (300 Mils) Narrow Body (Pb-free) | Automotive-E |
| | CY62256NLL–55ZXE | 51-85071 | 28-pin TSOP I (Pb-free) | |
| 70 | CY62256NLL–70PXC | 51-85017 | 28-pin (600 Mil) Molded DIP (Pb-free) | Commercial |
| | CY62256NLL–70SNXC | 51-85092 | 28-pin SNC (300 Mils) Narrow Body (Pb-free) | |
| | CY62256NLL–70ZRXI | 51-85074 | 28-pin Reverse TSOP I (Pb-free) | Industrial |
| | CY62256NLL–70SNXA | 51-85092 | 28-pin SNC (300 Mils) Narrow Body (Pb-free) | Automotive-A |

### Ordering Code Definitions



## Package Diagrams

**Figure 10. 28-pin PDIP (1.480 × 0.550 × 0.195 Inches) P28.6/PZ28.6 Package Outline, 51-85017**

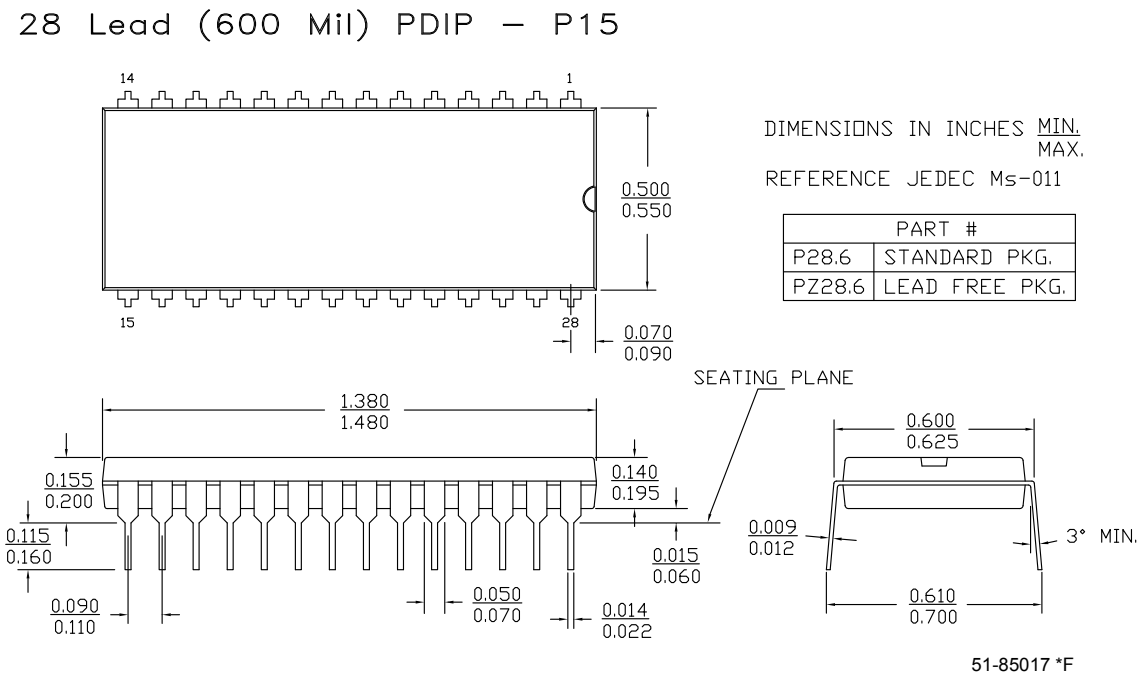
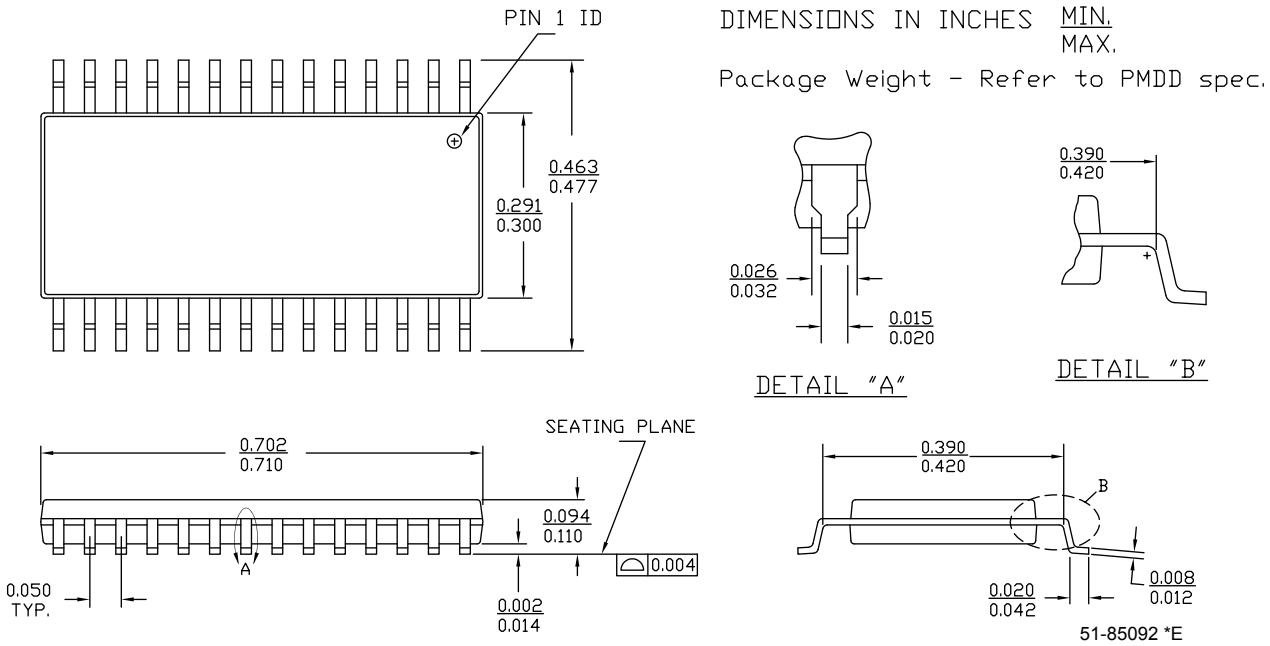



**Figure 11. 28-pin SNC (300 Mils) SN28.3 (Narrow Body) Package Outline, 51-85092**



## Package Diagrams *(continued)*

**Figure 12. 28-pin TSOP I (8 × 13.4 × 1.2 mm) Z28 (Standard) Package Outline, 51-85071**

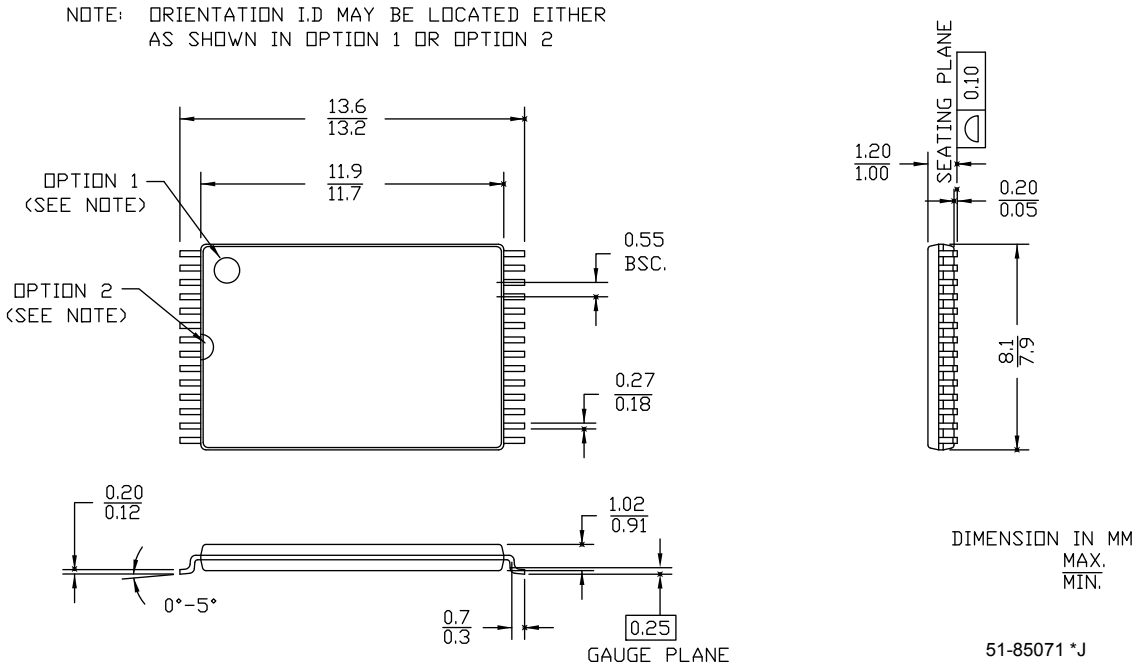
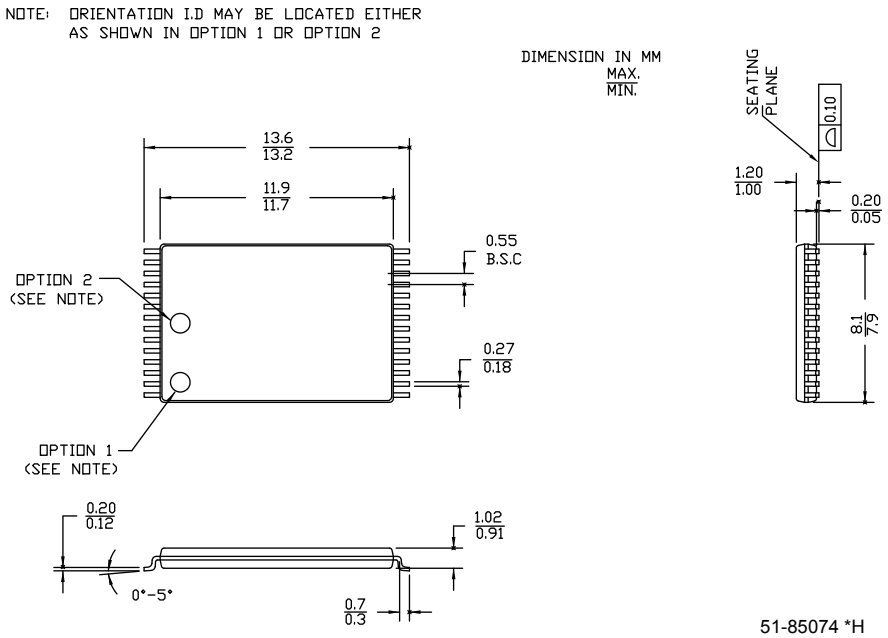



**Figure 13. 28-pin TSOP I (8 × 13.4 mm) Package Outline - Reverse, 51-85074**



## Acronyms

| Acronym | Description |
|---|---|
| CMOS | Complementary Metal Oxide Semiconductor |
| I/O | Input/Output |
| SRAM | Static Random Access Memory |
| TSOP | Thin Small Outline Package |
| VFBGA | Very Fine-Pitch Ball Grid Array |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|---|---|
| °C | degree Celsius |
| µA | microampere |
| mA | milliampere |
| MHz | megahertz |
| ns | nanosecond |
| Ω | ohm |
| pF | picofarad |
| V | volt |
| W | watt |

## Document History Page

| Document Title: CY62256N, 256-Kbit (32 K × 8) Static RAM<br>Document Number: 001-06511 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | 426504 | NXR | See ECN | New data sheet. |
| *A | 488954 | NXR | See ECN | Added Automotive product<br>Updated ordering Information table |
| *B | 2715270 | VKN / AESA | 06/05/2009 | Updated POD of 28-Pin (600-Mil) Molded DIP package (Spec# 51-85017) |
| *C | 2891344 | VKN | 03/12/2010 | Added Table of Contents<br>Removed “L” product information<br>Updated Ordering Information table<br>Updated Package Diagrams (Figure 10, Figure 11, and Figure 12)<br>Updated Sales, Solutions, and Legal Information |
| *D | 3119519 | AJU | 01/04/2011 | Updated Ordering Information.<br>Added Ordering Code Definitions. |
| *E | 3329873 | RAME | 07/27/11 | Updated template and styles according to current Cypress standards.<br>Added acronyms and units.<br>Removed reference to AN1064 SRAM system guidelines.<br>Updated operation recovery time parameter under Data Retention Characteristics on page 6. |
| *F | 3433878 | TAVA | 11/09/11 | Updated Package Diagrams. |
| *G | 4122787 | VINI | 09/13/2013 | Updated Package Diagrams:<br>spec 51-85092 – Changed revision from *D to *E.<br>Updated in new template.<br>Completing Sunset Review. |
| *H | 4525875 | VINI | 10/06/2014 | Updated Maximum Ratings:<br>Referred Note 2 in “Supply voltage to ground potential (pin 28 to pin 14)”.<br>Updated Package Diagrams:<br>spec 51-85071 – Changed revision from *I to *J.<br>spec 51-85074 – Changed revision from *G to *H.<br>Completing Sunset Review. |
| *I | 4576406 | VINI | 01/16/2015 | Added related documentation hyperlink in page 1.<br>Added Note 12 in Switching Characteristics.<br>Added note reference 12 in the Switching Characteristics table.<br>Added Note 20 in Switching Waveforms.<br>Added note reference 20 in Figure 9.<br>Updated Figure 10 in Package Diagrams (spec 51-85017 *E to *F). |
| *J | 5718683 | AESATMP7 | 04/28/2017 | Updated Cypress Logo and Copyright. |

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