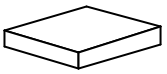
104-common x 132-segment BIT MAP LCD DRIVER

GENERAL DESCRIPTION

The **NJU6678V** is a 104-common x 132-segment bit map LCD driver to display graphics or characters.
It contains 21,120 bits display data RAM, microprocessor interface circuits, instruction decoder, and common and segment drivers.
An image data from CPU through the serial or 8-bit parallel interface are stored into the 21,120 bits internal display data RAM and are displayed on the LCD panel through the commons and segments drivers.
The **NJU6678V** displays 104 x 132 dots graphics or 8-character 6-line by 16 x 16 dots character.
The **NJU6678V** contains a built-in OSC circuit for reducing external components. And it features Partial Display Function containing selectable active display block(s) (two blocks max.) and optimizing the duty cycle ratio. This function dramatically reduces the operating current, setting the optimum boosted voltage combined with a programmable voltage booster circuit and an electrical variable resister. As result, it reduces the operating current.
The operating voltage from 2.5V to 3.3V and low operating current are suitable for small size battery operation items.

PACKAGE OUTLINE



NJU6678VCL

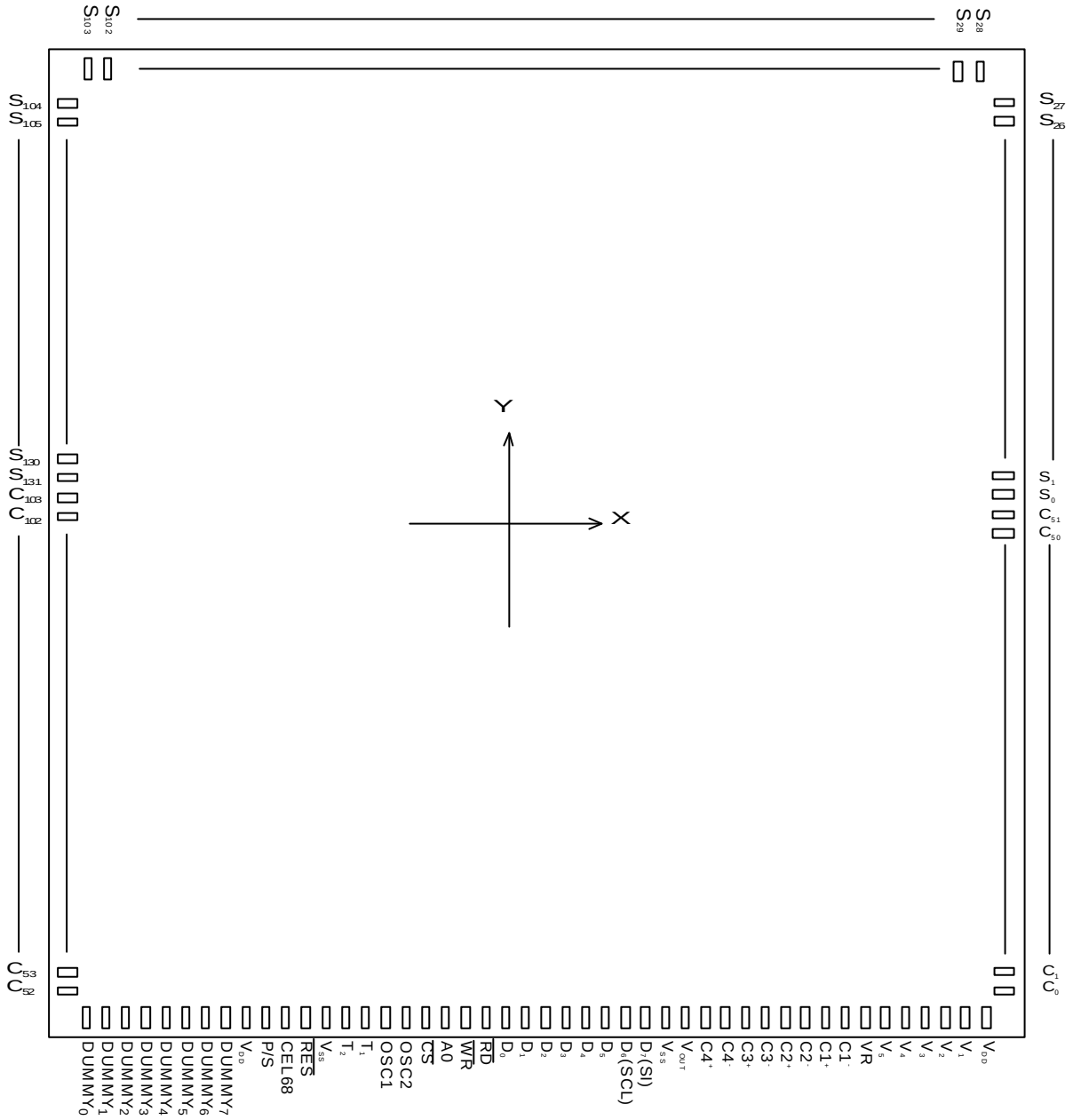
FEATURES

- Direct Correspondence of Display Data RAM to LCD Pixel
- Display Data RAM - 21,120 bits ;(1.5 times over than display size)
- LCD drivers - 104-common and 132-segment
- Direct connection to 8-bit Microprocessor interface for both of 68 and 80 type MPU
- Serial Interface
- Partial Display Function Two limited active display blocks setting. Duty ratio set automatically.
- Easy Vertical Scroll by setting the start line address of over size display data RAM
- Programmable Bias selection ; 1/4,1/5,1/6,1/7,1/8,1/9,1/10,1/11 bias
- Common Driver Order Assignment by mask option

Version	C_0 to C_{103}(Pin name)
NJU6678VA	Com_0 to Com_{103}
NJU6678VB	Com_{103} to Com_0

- Useful Instruction Sets
  Display ON/OFF Cont, Display Start Line Set, Page Address Set, Column Address Set, Status Read, Display Data Read/Write, Inverse Display, All On/Off, Partial Display, Bias Select, n-Line Inverse, Voltage Booster Circuits Multiple Select(Maximum 5-time), Read Modify Write, Power Saving, ADC Select, etc.
- Power Supply Circuits for LCD; Programmable Voltage Booster Circuits(5-time Maximum, Voltage boosting polarity:Negative voltage(V_{DD} Common)),Regulator, Voltage Follower (x 4)
- Precision Electrical Variable Resistance
- Low Power Consumption
- Operating Voltage --- 2.5V to 3.3V
- LCD Driving Voltage --- 6.0V to 17V
- Package Outline --- Bumped Chip
- C-MOS Technology (Substrate:N)

■ PAD LOCATION



Chip Center	: X=0um,Y=0um
Chip Size	: X=5.36mm,Y=5.31mm
Chip Thickness	: 675um ± 30um
Bump Size	: 45um x 83um
Pad pitch	: 60um(Min)
Bump Height	: 15um TYP.
Bump Material	: Au
Voltage boosting polarity	:Negative voltage (VDD Common)
Substrate	:N

■ TERMINAL DESCRIPTION

Chip Size 5.36 x 5.31mm (Chip Center X=0um,Y=0um)

PAD No.	Terminal	X= um	Y= um
1	DUMMY0	-2250	-2497
2	DUMMY1	-2190	-2497
3	DUMMY2	-2130	-2497
4	DUMMY3	-2070	-2497
5	DUMMY4	-2010	-2497
6	DUMMY5	-1950	-2497
7	DUMMY6	-1890	-2497
8	DUMMY7	-1830	-2497
9	V_{DD}	-1747	-2497
10	P/S	-1666	-2497
11	SEL68	-1596	-2497
12	$\overline{RES}$	-1487	-2497
13	V_{SS}	-1417	-2497
14	T_2	-1347	-2497
15	T_1	-1238	-2497
16	OSC_1	-1168	-2497
17	OSC_2	-1049	-2497
18	$\overline{CS}$	-979	-2497
19	A0	-861	-2497
20	$\overline{WR}$	-791	-2497
21	$\overline{RD}$	-667	-2497
22	D_0	-510	-2497
23	D_1	-289	-2497
24	D_2	-69	-2497
25	D_3	152	-2497
26	D_4	372	-2497
27	D_5	592	-2497
28	$D_{6(SCL)}$	813	-2497
29	$D_{7(SI)}$	1033	-2497
30	V_{SS}	1191	-2497
31	V_{OUT}	1261	-2497
32	$C4^+$	1331	-2497
33	$C4^-$	1401	-2497
34	$C3^+$	1471	-2497
35	$C3^-$	1541	-2497
36	$C2^+$	1611	-2497
37	$C2^-$	1681	-2497
38	$C1^+$	1751	-2497
39	$C1^-$	1821	-2497
40	VR	1891	-2497
41	V_5	1961	-2497
42	V_4	2031	-2497
43	V_3	2101	-2497
44	V_2	2171	-2497
45	V_1	2241	-2497
46	V_{DD}	2311	-2497
47	C_0	2523	-2370
48	C_1	2523	-2310
49	C_2	2523	-2250
50	C_3	2523	-2190

PAD No.	Terminal	X= um	Y= um
51	C_4	2523	-2130
52	C_5	2523	-2070
53	C_6	2523	-2010
54	C_7	2523	-1950
55	C_8	2523	-1890
56	C_9	2523	-1830
57	C_{10}	2523	-1770
58	C_{11}	2523	-1710
59	C_{12}	2523	-1650
60	C_{13}	2523	-1590
61	C_{14}	2523	-1530
62	C_{15}	2523	-1470
63	C_{16}	2523	-1410
64	C_{17}	2523	-1350
65	C_{18}	2523	-1290
66	C_{19}	2523	-1230
67	C_{20}	2523	-1170
68	C_{21}	2523	-1110
69	C_{22}	2523	-1050
70	C_{23}	2523	-990
71	C_{24}	2523	-930
72	C_{25}	2523	-870
73	C_{26}	2523	-810
74	C_{27}	2523	-750
75	C_{28}	2523	-690
76	C_{29}	2523	-630
77	C_{30}	2523	-570
78	C_{31}	2523	-510
79	C_{32}	2523	-450
80	C_{33}	2523	-390
81	C_{34}	2523	-330
82	C_{35}	2523	-270
83	C_{36}	2523	-210
84	C_{37}	2523	-150
85	C_{38}	2523	-90
86	C_{39}	2523	-30
87	C_{40}	2523	30
88	C_{41}	2523	90
89	C_{42}	2523	150
90	C_{43}	2523	210
91	C_{44}	2523	270
92	C_{45}	2523	330
93	C_{46}	2523	390
94	C_{47}	2523	450
95	C_{48}	2523	510
96	C_{49}	2523	570
97	C_{50}	2523	630
98	C_{51}	2523	690
99	S_0	2523	750
100	S_1	2523	810

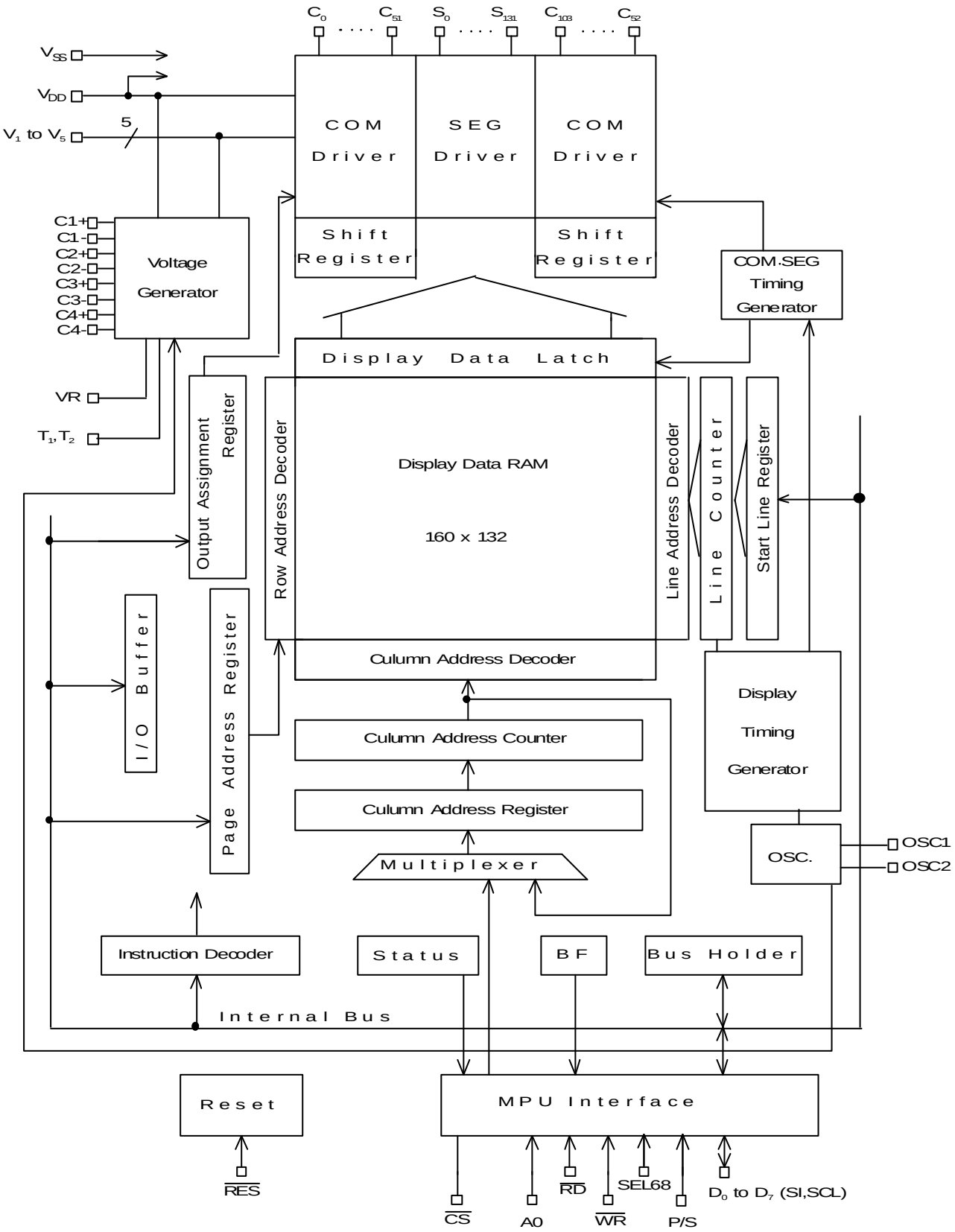
PAD No.	Terminal	X= um	Y= um
101	S2	2523	870
102	S3	2523	930
103	S4	2523	990
104	S5	2523	1050
105	S6	2523	1110
106	S7	2523	1170
107	S8	2523	1230
108	S9	2523	1290
109	S10	2523	1350
110	S11	2523	1410
111	S12	2523	1470
112	S13	2523	1530
113	S14	2523	1590
114	S15	2523	1650
115	S16	2523	1710
116	S17	2523	1770
117	S18	2523	1830
118	S19	2523	1890
119	S20	2523	1950
120	S21	2523	2010
121	S22	2523	2070
122	S23	2523	2130
123	S24	2523	2190
124	S25	2523	2250
125	S26	2523	2310
126	S27	2523	2370
127	S28	2250	2497
128	S29	2190	2497
129	S30	2130	2497
130	S31	2070	2497
131	S32	2010	2497
132	S33	1950	2497
133	S34	1890	2497
134	S35	1830	2497
135	S36	1770	2497
136	S37	1710	2497
137	S38	1650	2497
138	S39	1590	2497
139	S40	1530	2497
140	S41	1470	2497
141	S42	1410	2497
142	S43	1350	2497
143	S44	1290	2497
144	S45	1230	2497
145	S46	1170	2497
146	S47	1110	2497
147	S48	1050	2497
148	S49	990	2497
149	S50	930	2497
150	S51	870	2497

PAD No.	Terminal	X= um	Y= um
151	S52	810	2497
152	S53	750	2497
153	S54	690	2497
154	S55	630	2497
155	S56	570	2497
156	S57	510	2497
157	S58	450	2497
158	S59	390	2497
159	S60	330	2497
160	S61	270	2497
161	S62	210	2497
162	S63	150	2497
163	S64	90	2497
164	S65	30	2497
165	S66	-30	2497
166	S67	-90	2497
167	S68	-150	2497
168	S69	-210	2497
169	S70	-270	2497
170	S71	-330	2497
171	S72	-390	2497
172	S73	-450	2497
173	S74	-510	2497
174	S75	-570	2497
175	S76	-630	2497
176	S77	-690	2497
177	S78	-750	2497
178	S79	-810	2497
179	S80	-870	2497
180	S81	-930	2497
181	S82	-990	2497
182	S83	-1050	2497
183	S84	-1110	2497
184	S85	-1170	2497
185	S86	-1230	2497
186	S87	-1290	2497
187	S88	-1350	2497
188	S89	-1410	2497
189	S90	-1470	2497
190	S91	-1530	2497
191	S92	-1590	2497
192	S93	-1650	2497
193	S94	-1710	2497
194	S95	-1770	2497
195	S96	-1830	2497
196	S97	-1890	2497
197	S98	-1950	2497
198	S99	-2010	2497
199	S100	-2070	2497
200	S101	-2130	2497

PAD No.	Terminal	X= um	Y= um
201	S102	-2190	2497
202	S103	-2250	2497
203	S104	-2524	2370
204	S105	-2524	2310
205	S106	-2524	2250
206	S107	-2524	2190
207	S108	-2524	2130
208	S109	-2524	2070
209	S110	-2524	2010
210	S111	-2524	1950
211	S112	-2524	1890
212	S113	-2524	1830
213	S114	-2524	1770
214	S115	-2524	1710
215	S116	-2524	1650
216	S117	-2524	1590
217	S118	-2524	1530
218	S119	-2524	1470
219	S120	-2524	1410
220	S121	-2524	1350
221	S122	-2524	1290
222	S123	-2524	1230
223	S124	-2524	1170
224	S125	-2524	1110
225	S126	-2524	1050
226	S127	-2524	990
227	S128	-2524	930
228	S129	-2524	870
229	S130	-2524	810
230	S131	-2524	750
231	C103	-2524	690
232	C102	-2524	630
233	C101	-2524	570
234	C100	-2524	510
235	C99	-2524	450
236	C98	-2524	390
237	C97	-2524	330
238	C96	-2524	270
239	C95	-2524	210
240	C94	-2524	150
241	C93	-2524	90
242	C92	-2524	30
243	C91	-2524	-30
244	C90	-2524	-90
245	C89	-2524	-150
246	C88	-2524	-210
247	C87	-2524	-270
248	C86	-2524	-330
249	C85	-2524	-390
250	C84	-2524	-450

PAD No.	Terminal	X= um	Y= um
251	C83	-2524	-510
252	C82	-2524	-570
253	C81	-2524	-630
254	C80	-2524	-690
255	C79	-2524	-750
256	C78	-2524	-810
257	C77	-2524	-870
258	C76	-2524	-930
259	C75	-2524	-990
260	C74	-2524	-1050
261	C73	-2524	-1110
262	C72	-2524	-1170
263	C71	-2524	-1230
264	C70	-2524	-1290
265	C69	-2524	-1350
266	C68	-2524	-1410
267	C67	-2524	-1470
268	C66	-2524	-1530
269	C65	-2524	-1590
270	C64	-2524	-1650
271	C63	-2524	-1710
272	C62	-2524	-1770
273	C61	-2524	-1830
274	C60	-2524	-1890
275	C59	-2524	-1950
276	C58	-2524	-2010
277	C57	-2524	-2070
278	C56	-2524	-2130
279	C55	-2524	-2190
280	C54	-2524	-2250
281	C53	-2524	-2310
282	C52	-2524	-2370

■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>1 to 8</td><td>DUMMY0
to
DUMMY7</td><td></td><td>Dummy Terminals.
These are open terminals electrically.</td></tr>
<tr><td>9,46</td><td>V_{DD}</td><td>Power</td><td>Power Supply Terminal (+2.5V - +3.3V)</td></tr>
<tr><td>13,30</td><td>V_{SS}</td><td>GND</td><td>Ground Terminal (0V)</td></tr>
<tr><td>45
44
43
42
41</td><td>V_1
V_2
V_3
V_4
V_5</td><td>Power</td><td>LCD Driving Voltage Supplying Terminals. In case of the external power supply operation without internal power supply operation, each level of LCD driving voltage is supplied from outside fitting with following relation.
$V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5 \geq V_{OUT}$
In case of the internal power supply, LCD driving voltages V1-V4 depending on the Bias selection are supplied as shown in follows;
<table>
<tr><th>Bias</th><th>V_1</th><th>V_2</th><th>V_3</th><th>V_4</th></tr>
<tr><td>1/4Bias</td><td>V_5+3/4V_{LCD}</td><td>V_5+2/4V_{LCD}</td><td>V_5+2/4V_{LCD}</td><td>V_5+1/4V_{LCD}</td></tr>
<tr><td>1/5Bias</td><td>V_5+4/5V_{LCD}</td><td>V_5+3/5V_{LCD}</td><td>V_5+2/5V_{LCD}</td><td>V_5+1/5V_{LCD}</td></tr>
<tr><td>1/6Bias</td><td>V_5+5/6V_{LCD}</td><td>V_5+4/6V_{LCD}</td><td>V_5+2/6V_{LCD}</td><td>V_5+1/6V_{LCD}</td></tr>
<tr><td>1/7Bias</td><td>V_5+6/7V_{LCD}</td><td>V_5+5/7V_{LCD}</td><td>V_5+2/7V_{LCD}</td><td>V_5+1/7V_{LCD}</td></tr>
<tr><td>1/8Bias</td><td>V_5+7/8V_{LCD}</td><td>V_5+6/8V_{LCD}</td><td>V_5+2/8V_{LCD}</td><td>V_5+1/8V_{LCD}</td></tr>
<tr><td>1/9Bias</td><td>V_5+8/9V_{LCD}</td><td>V_5+7/9V_{LCD}</td><td>V_5+2/9V_{LCD}</td><td>V_5+1/9V_{LCD}</td></tr>
<tr><td>1/10Bias</td><td>V_5+9/10V_{LCD}</td><td>V_5+8/10V_{LCD}</td><td>V_5+2/10V_{LCD}</td><td>V_5+1/10V_{LCD}</td></tr>
<tr><td>1/11Bias</td><td>V_5+10/11V_{LCD}</td><td>V_5+9/11V_{LCD}</td><td>V_5+2/11V_{LCD}</td><td>V_5+1/11V_{LCD}</td></tr>
</table>
($V_{LCD}=V_{DD}-V_5$)</td></tr>
<tr><td>38,39
36,37
34,35
32,33</td><td>$C1^+$,$C1^-$
$C2^+$,$C2^-$
$C3^+$,$C3^-$
$C4^+$,$C4^-$</td><td>O</td><td>Capacitor connecting terminals for Internal Voltage Booster.Boosting time is programmed by instruction (2 to 5 times)</td></tr>
<tr><td>31</td><td>V_{OUT}</td><td>O</td><td>Boosted voltage output terminal. Connects the capacitor between V_{OUT} terminal and V_{SS}.</td></tr>
<tr><td>40</td><td>VR</td><td>I</td><td>V_{LCD} voltage adjustment terminal. The gain of V_{LCD} setup circuit for V5 level is adjusted by external resistors.</td></tr>
<tr><td>15
14</td><td>T_1
T_2</td><td>I</td><td>LCD bias voltage control terminals.
<table>
<tr><th>T_1</th><th>T_2</th><th>Voltage booster Cir.</th><th>Voltage Adj.</th><th>V/F Cir.</th></tr>
<tr><td>L</td><td>L/H</td><td>Available</td><td>Available</td><td>Available</td></tr>
<tr><td>H</td><td>L</td><td>Not Avail.</td><td>Available</td><td>Available</td></tr>
<tr><td>H</td><td>H</td><td>Not Avail.</td><td>Not Avail.</td><td>Available</td></tr>
</table></td></tr>
<tr><td>22 to 29</td><td>D_0 to
D_7
(SI)
(SCL)</td><td>I/O</td><td>Data Input/Output terminals.
In Pararel Interface Mode (P/S="H")
I/O terminals of 8-bit bus.
In Serial Interface Mode (P/S="L")
D_7: Input terminal of serial data (SI).
D_6: Input terminal of serial data clock (SCL).
D_0 to D_5 terminals are Hi-impedance.
When $\overline{CS}$="H", D_0 to D_7 terminals are Hi-impedance.</td></tr>
<tr><td>19</td><td>A0</td><td>I</td><td>Data discremination signal input terminal. The signal from MPU discreminates transmoitted data between Display data and Instruction.
<table>
<tr><th>A0</th><th>H</th><th>L</th></tr>
<tr><td>Distin.</td><td>Display Data</td><td>Instruction</td></tr>
</table></td></tr>
<tr><td>12</td><td>$\overline{RES}$</td><td>I</td><td>Reset terminal.
Reset operation is executing during "L" state of $\overline{RES}$.</td></tr>
<tr><td>18</td><td>$\overline{CS}$</td><td>I</td><td>Chip select signal input terminal.
Data Input/Output are available during $\overline{CS}$ ="L".</td></tr>
</table>

<table>
<tr><th>No</th><th>Symbol</th><th>I/O</th><th>F u n c t i o n</th></tr>
<tr><td>21</td><td>$\overline{RD}$(E)</td><td>I</td><td>RD(80 type) or E(68 type) signal input terminal.
<In 80 type MPU mode >(SEL68="L")
$\overline{RD}$ signal from 80 type MPU input terminal. Active "L".
D_0 to D_7 terminals are output during "L" level.
<In 68 type MPU mode >(SEL68="H")
Enable signal from 68 type MPU input terminal. Active "H".</td></tr>
<tr><td>20</td><td>$\overline{WR}$(RW)</td><td>I</td><td>WR(80 type) or R/W(68 type) signal input terminal
<In 80 type MPU mode >(SEL68="L")
$\overline{WR}$ signal from 80 type MPU input terminal. Active "L".
The data transmitted during WR="L" are fetched at the rising edge of $\overline{WR}$.
<In 68 type MPU mode > (SEL68="H")
R/W signal from 68 type MPU input terminal.
<table>
<tr><td>R/W</td><td>H</td><td>L</td></tr>
<tr><td>State</td><td>Read</td><td>Write</td></tr>
</table></td></tr>
<tr><td>11</td><td>SEL68</td><td>I</td><td>MPU interface type selection terminal. This terminal must connect to V_{DD} or V_{SS}.
<table>
<tr><td>SEL68</td><td>H</td><td>L</td></tr>
<tr><td>State</td><td>68 Type</td><td>80 Type</td></tr>
</table></td></tr>
<tr><td>10</td><td>P/S</td><td>I</td><td>Parallel or Serial interface selection signal input terminal.
<table>
<tr><td>P/S</td><td>Chip Select</td><td>Data/Command</td><td>Data</td><td>Read/Write</td><td>serial Clock</td></tr>
<tr><td>"H"</td><td>$\overline{CS}$</td><td>A</td><td>D_0 to D_7</td><td>$\overline{RD}$,$\overline{WR}$</td><td>-</td></tr>
<tr><td>"L"</td><td>$\overline{CS}$</td><td>A0</td><td>SI(D_7)</td><td>-</td><td>SCL(D_6)</td></tr>
</table>
In case of serial interface(P/S="L")
RAM data and status read operation do not work in mode of the serial interface. $\overline{RD}$ and WR terminals must fix to "H" or "L". D_0 to D_5 terminals are Hi-impedance.</td></tr>
<tr><td>16
17</td><td>OSC_1
OSC_2</td><td>I</td><td>External clock input terminal. In Internal oscillation operation, OSC1 and OSC2 terminals should be Open.In External clock operation, the external clock input to OSC1 terminal.</td></tr>
<tr><td>47 to 98</td><td>C_0 to C_{51}</td><td>O</td><td>LCD driving signal output terminals.
Common output terminals:C_0 to C_{103}
Segment output terminals:S_0 to S_{131}

Common output terminal
Following output voltage is selected by the combination of alternating (FR) signal and Common scanning data.
<table>
<tr><td>Scan data</td><td>FR</td><td>Output Voltage</td></tr>
<tr><td rowspan="2">H</td><td>H</td><td>V_5</td></tr>
<tr><td>L</td><td>V_{DD}</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V_1</td></tr>
<tr><td>L</td><td>V_4</td></tr>
</table>
Segment output terminal
Following output voltage is selected by the combination of alternating (FR) signal and display data in the DD RAM.
<table>
<tr><td rowspan="2">RAM Data</td><td rowspan="2">FR</td><td colspan="2">Output Voltage</td></tr>
<tr><td>Normal</td><td>Reverse</td></tr>
<tr><td rowspan="2">H</td><td>H</td><td>V_{DD}</td><td>V_2</td></tr>
<tr><td>L</td><td>V_5</td><td>V_3</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V_2</td><td>V_{DD}</td></tr>
<tr><td>L</td><td>V_3</td><td>V_5</td></tr>
</table></td></tr>
<tr><td>99 to 230</td><td>S_0 toS_{131}</td><td>O</td><td></td></tr>
<tr><td>282 to 231</td><td>C_{52} to C_{103}</td><td>O</td><td></td></tr>
</table>

■ Functional Description

(1) Description for each blocks

(1-1) Busy Flag (BF)

The Busy Flag (BF) is set to logical "1" in busy of internal execution by an instruction, and any instruction excepting for the "Status Read" is disable at this time. Busy Flag is outputted through D_7 terminal by "Status Read" instruction. Although another instructions should be inputted after check of Busy Flag, no need to check Busy flag if the system cycle time (t_{CYC}) as shown in ■AC Characteristics is secured completely.

(1-2)Display Start Line Register

The Display Start Line Register is a register to set a display data RAM address corresponding to the COM_0 display line (the top line normally) for the vertical scroll on the LCD, Page address change and so forth. The Display Start Line Address set instruction sets the 8-bit display start address into this register.

(1-3) Line Counter

Line Counter is reset when the internal FR signal is switched and outputs the line address of the display data RAM by count up operation synchronizing with common cycle of **NJU6678V**.

(1-4) Column Address Counter

Column Address Counter is the 8-bit preset-able counter to point the column address of the display data RAM (DD RAM) as shown in Figure 1. The counter is incremented automatically after the display data read/write instructions execution. When the Column address counter reaches to the maximum existing address by the increment operations, the count up operation (increment) is frozen. However, when new address is set to the column address counter again, it restarts the count up operation from a set address. The operation of Column Address Counter is independent against Page Address Register.

By the address inverse instruction (ADC select) as shown in Figure 1, Column Address Decoder reverses the correspondence between Column address and Segment output of display data RAM.

(1-5) Page address Register

Page Address Register assigns the page address of the display data RAM as shown in Figure 1. In case of accessing from the MPU with changing the page address, Page Address Set instruction is required.

(1-6) Display Data RAM

The Display data RAM (DD RAM) is the bit map RAM consisting of 21,120 bits to store the display data corresponding to the LCD pixel on LCD panel.

The DD RAM data and the state of the LCD:

In Normal Display : "1"=Turn-On Display, "0" =Turn-Off Display

In Reveres Display : "1"=Turn-Off Display, "0" =Turn-On Display

DD RAM output 132 bits parallel data addressed by line address counter then the data latched in the display data latch. Asynchronous data access to the DD RAM is available due to the access to the DD RAM from the CPU and latch to the display data latch operation are done independently.

(1-7) Common Driver Assignment

This circuit determines the scanning direction of the common output.

Table 1

	COM Outputs Terminals			
PAD No.	47	98	231	282
Pin name	C_0	C_{51}	C_{103}	C_{52}
Ver.A	COM_0 →	COM_{51}	COM_{103} ←	COM_{52}
Ver.B	COM_{103} ←	COM_{52}	COM_0 →	COM_{51}

The Mask fixes the common scanning direction between version A and B that can not be changed by the instruction.

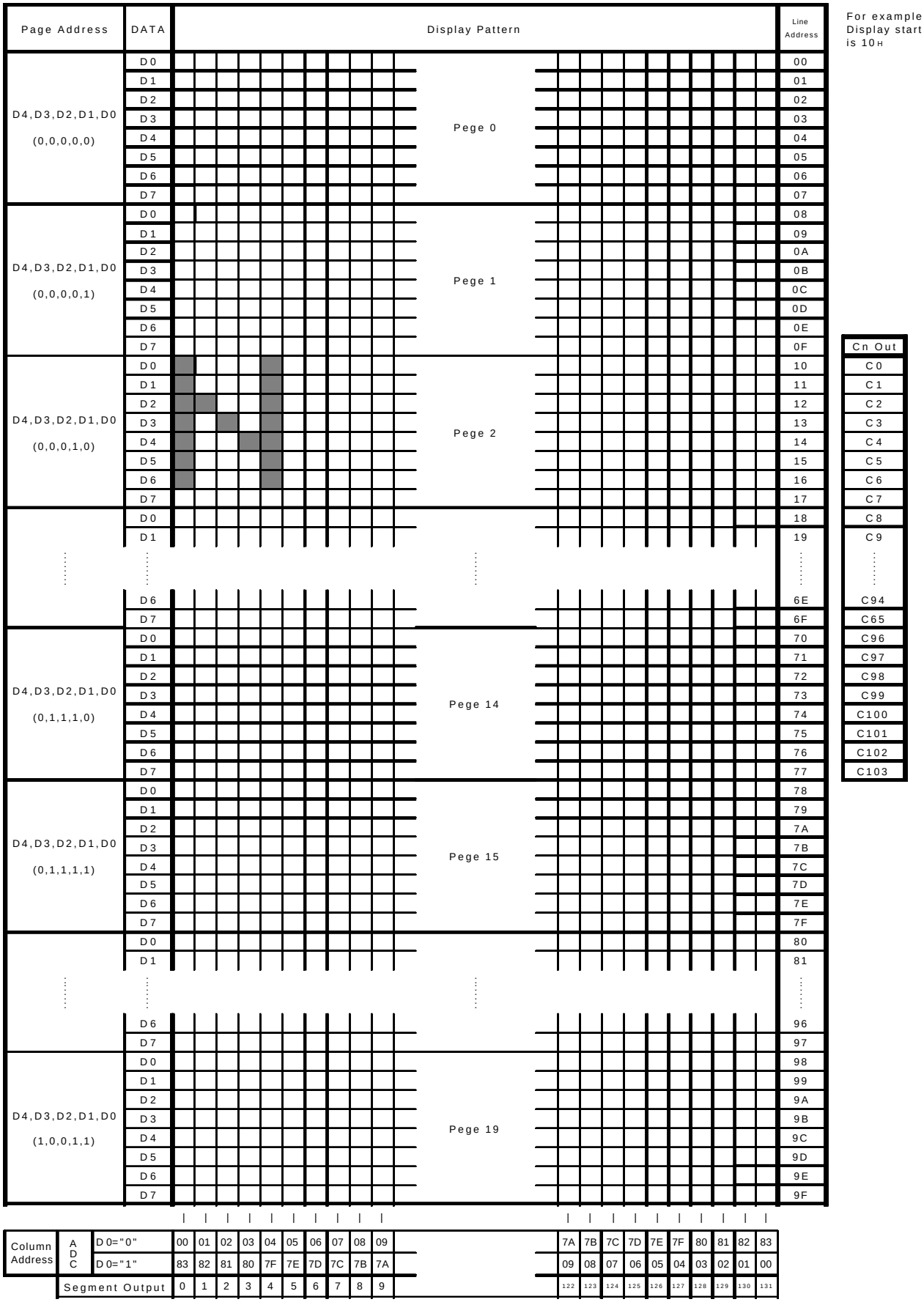


Fig.1 Correspondence with Display Data RAM Address

(1-8) Reset Circuit

When the input signal to $\overline{RES}$ terminal goes to "L", the reset circuit executes initialization as below;

The Initialization state (default)

1 Display Off
2 Normal Display (not inverse)
3 ADC Select : Normal (ADC Instruction D0 ="0")
4 Read Modify Write Mode Off
5 Voltage Booster off, Voltage Regulator off, Voltage follower off
6 Static Drive Off
7 Driver Output Off
8 Clear the data of serial interface register
9 Set the Column Address Counter to 00H
10 Set the Display Start Line Register to 00H
11 Set the Page Address Register to page "0"
12 Set the EVR register to FFH
13 Set the Partial Display(1/104 duty)
14 Set the Bias select(1/11 Bias)
15 Set the Voltage Booster(5 times)
16 Set the n-line inverse register to 0H

The $\overline{RES}$ terminal connects to the reset terminal of the MPU synchronization with the MPU initialization as shown in " the MPU interface " in the Application Circuit section. The "L" level input signal as reset signal must keep the period over than 10us as shown in DC Characteristics. The **NJU6678V** takes 1us for the reset operation after the rising edge of the $\overline{RES}$ signal.
The reset operation by $\overline{RES}$ ="L" initializes each resister setting as above reset status, but the internal oscillation circuit and output terminals (D0 to D7) are not affected.
To avoid the lock-up, the reset operation by the $\overline{RES}$ terminal must be required every time when power terns on.
The reset operation by the reset instruction, function 9 to 16 operations mentioned above is performed.
The $\overline{RES}$ terminal must be keep "L" level when the power terns on in not use of the built-in LCD power supply circuit for no affect to the internal execution.

(1-9) LCD Driving Circuit

(a) LCD Driving Circuits

LCD driver is 236 sets of multiplexer consisting of 132 segments and 104 commons drivers to output LCD driving voltage. The common driver outputs the common scan signals formed with the shift register. The segment driver outputs the segment driving signal determined by a combination of display data in the DD RAM, common timing, FR signal, and alternating signal for LCD. The output wave forms of segment/common are shown in ■LCD DRIVING WAVEFORM.

(b) Display Data Latch Circuits

Display Data Latch Circuit latches the 132-bit display data outputted from the DD RAM addressed by the Line address counter to LCD driver at every common signal cycle temporarily. The original data in the DD RAM is not changed because of the Normal/Reverse display, Display On/Off, Static drive On/Off instruction processes only stored data in this Display Data Latch Circuit.

(c) Signal forming to Line Counter and Display Data Latch Circuit

The count clock to Line Counter and the latch clock to Display Data Latch Circuit are formed using the internal display clock (CL). The display data of 132 bits from Display Data RAM pointed by the line address synchronizing with the internal display clock are latched into the Display Data Latch Circuit and are outputted to LCD driving circuits.
The display data read out operation from DD RAM to the LCD Driver Circuit is completely independent operation with an access to the display data RAM from MPU.

(d) Display Timing Generation Circuit

The display timing generation circuit generates the internal timing of the display system by the master clock and the internal FR signal. As for it, the internal FR signal and the LCD alternating signal generate the wave form of 2-frame alternating drive wave form or the n-line inverse drive method for the LCD Driving circuit.

(e)Common Timing Generator

The Common Timing Generator generates the common timing signal from the display clock (CL).

-2-frame alternating drive mode

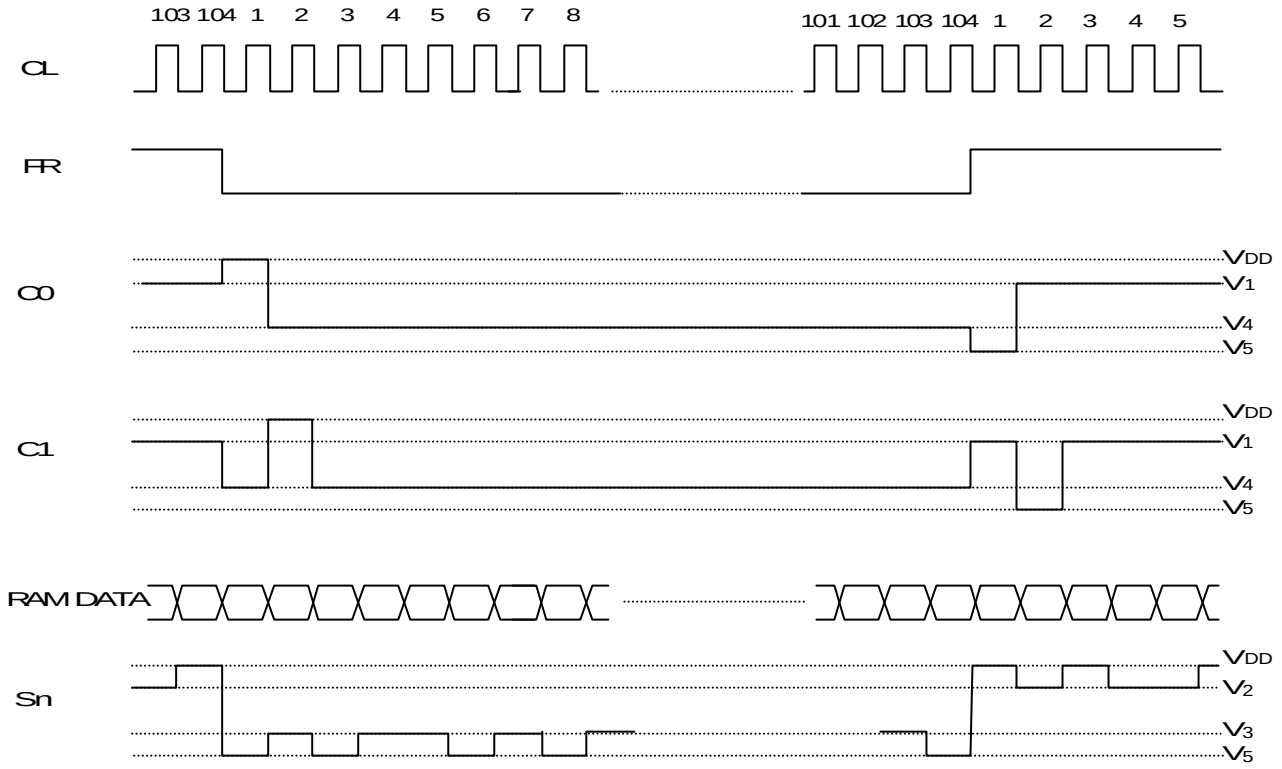


Fig.2

-n-line inverse drive mode (n=7, line inverting register sets to 6)

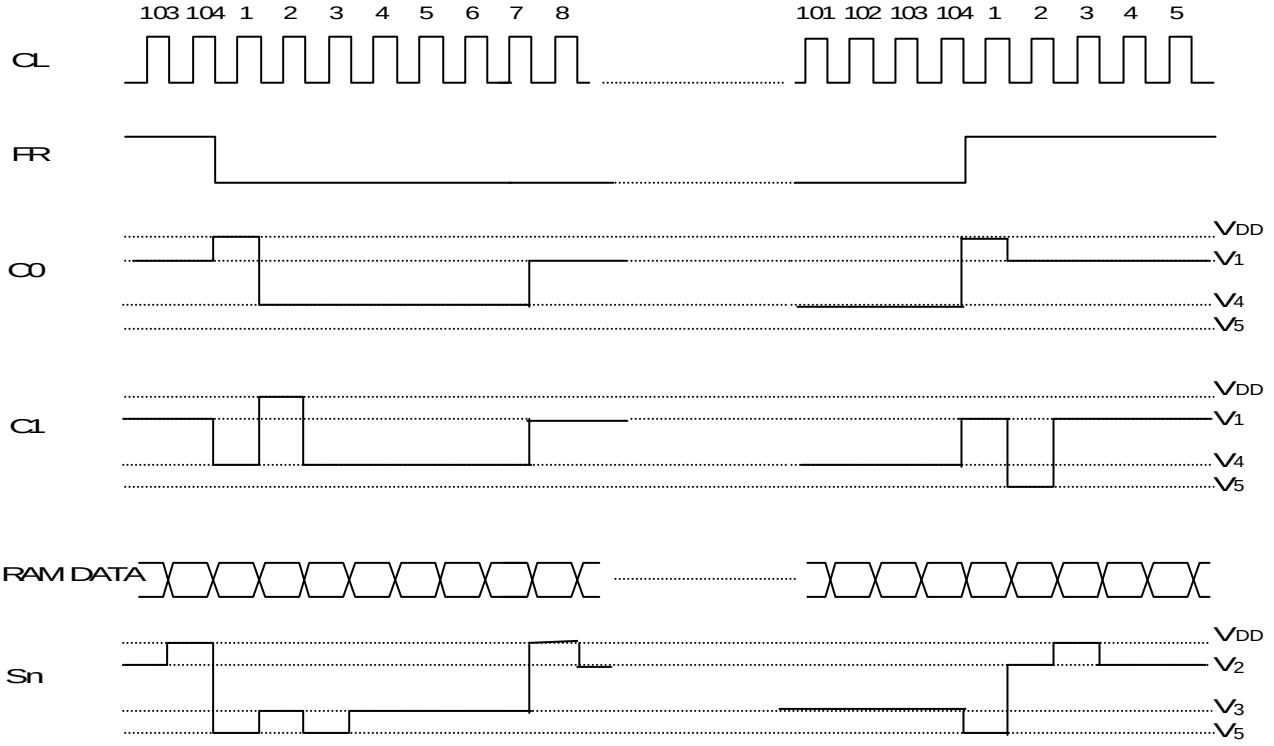


Fig.3

(f) Oscillation Circuit

The Oscillation Circuit is a low power type CR oscillator using an internal resistor and capacitor. The oscillator output is using for the display timing clock and for the voltage booster circuit. And the display clock(CL) is generated from this oscillator output frequency by dividing.

-The relation between duty and divide

Table 2

Duty	1/8	1/16	1/24	1/32	1/40	1/48,56	1/64,72	1/80,88	1/96,104
Divide	1/50	1/25	1/16	1/12	1/10	1/8	1/6	1/5	1/4

(g) Power Supply Circuit

The internal power supply circuit generates the voltage for driving LCD. It consists of voltage booster circuits (from 2 times to 5 times), voltage regulator circuits, and voltage followers.

The operation of internal Power Supply Circuits is controlled by the Internal Power Supply On/Off Instruction. When the Internal Power Supply Off Instruction is executed, all of the voltage booster circuits, regulator circuits, voltage follower circuits are turned off. In this time, the bias voltage of V_1, V_2, V_3, V_4,V_5 and V_{OUT} for the LCD should be supplied from outside, terminals $C1^+$, $C1^-$, $C2^+$, $C2^-$, $C3^+$, $C3^-$, $C4^+$, $C4^-$, and VR should be open. The status of internal power supply is selected by T_1 and T_2 terminal. Furthermore the external power supply operates with some of internal power supply function.

Table 3

T_1	T_2	Voltage Booster	Voltage Adj.	Buffer(V/F)	Ext.Pow Supply	C_{1+},C_{1-} to C_{4+},C_{4-}	VR Term.
L	L/H	ON	ON	ON	-		
H	L	OFF	ON	ON	V_{OUT}	Open	
H	H	OFF	OFF	ON	V_5,V_{OUT}	Open	Open

When (T_1, T_2)=(H, L), $C1^+$, $C1^-$, $C2^+$, $C2^-$,$C3^+$, $C3^-$, $C4^+$, $C4^-$ terminals for voltage booster circuits are open because the voltage booster circuits doesn't operate. Therefore LCD driving voltage to the V_{OUT} terminal should be supplied from outside.

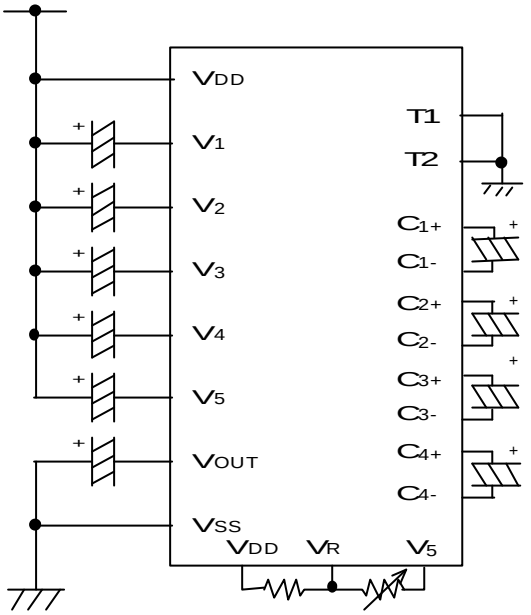
When (T_1, T_2)=(H, H), terminals for voltage booster circuits and VR are open, because the voltage booster circuits and Voltage adjust circuits do not operate.

The internal power supply Circuits is designed specially for a small-size LCD like as normal cellular phone size LCD panel. When **NJU6678V** apply to the large size LCD panel application (large capacitive load), external power supply is required to keep good display condition..

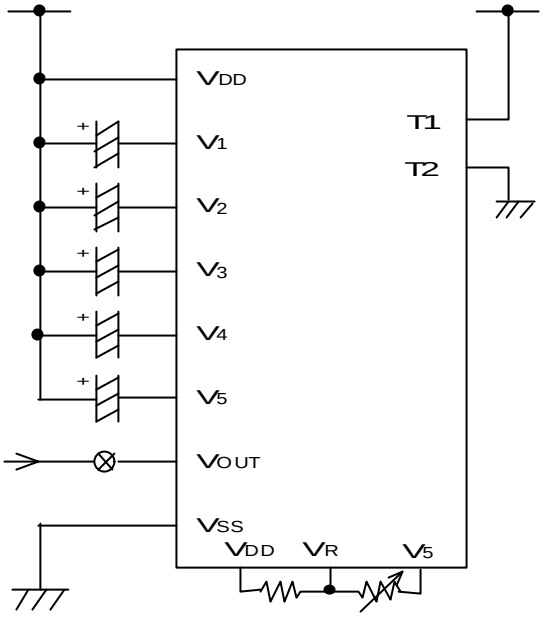
To keep good display condition, external component of the capacitors connecting to the V1 to V5 terminals and voltage booster circuits and the feedback resistors for the V5 operational amplifier must fix each optimized constant after checking various display patterns on LCD panel actually in the application.

○Power Supply applications

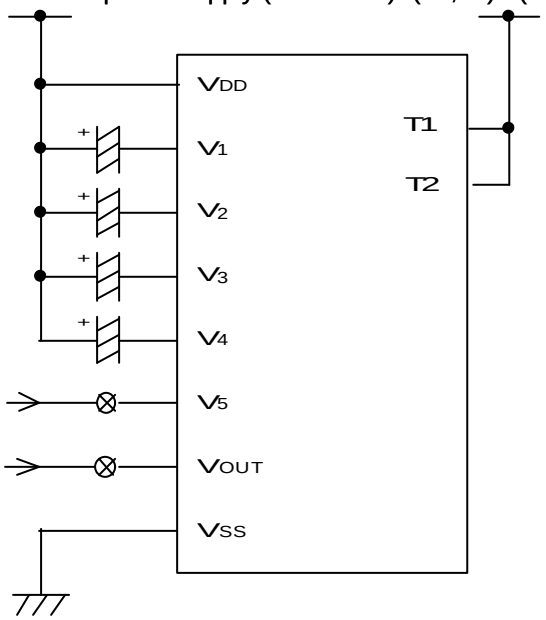
(1) Internal Power Supply Example.
All of the Internal Booster, Voltage Regulator, Voltage Follower using.
Internal power supply ON (instruction) (T1,T2)=(L,L)



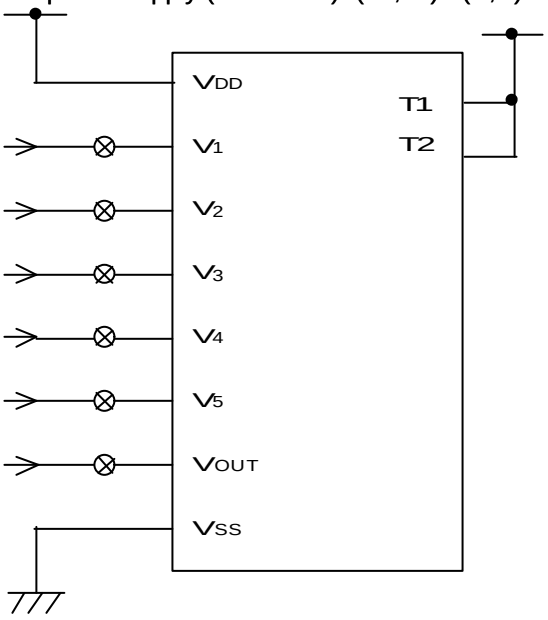
(2) Only VOUT Supply from outside Example.
Internal Voltage Regulator, Voltage Follower using
Internal power supply ON (Instruction) (T1,T2) = (H,L)



(3) VOUT and V5 supply from outside Example.
Internal Voltage Follower using.
Internal power supply (Instruction) (T1,T2) =(H,H)



(4) External Power Supply Example
All of V1 to V5 and VOUT supply from outside
Internal power supply (Instruction) (T1,T2) =(H,H)



⊗ : These switches should be open during the power save mode.

(2) Instruction

The **NJU6678V** distinguishes the data on the data bus D0 to D7 as an instruction by combination of A0, $\overline{RD}$, and $\overline{WR}$(R/W) signals. The decoding of the instruction and exection performes with only high speed internal timing without relation to the external clock. Therefore, no busy flag check required normally. In case of the serial interface, the data input as MSB(D7) first serially. Table.4 shows the instruction codes of the **NJU6678V**.

Table 4. Instruction Code (*:Don't Care)

Instruction		Code											Description
		A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(a)	Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0/1	LCD Display ON/OFF 0:OFF 1:ON
(b)	Display Start Line Set High Order 4bits	0	1	0	0	1	0	1	High Order Address				Determine the Display Line of RAM to the COM0. (Set the Higher order 4bits)
	Display Start Line Set Lower Order 4bits	0	1	0	0	1	1	0	Lower Order Address				Determine the Display Line of RAM to the COM0. (Set the Lower order 4bits)
(c)	Page Address Set High Order 1bits	0	1	0	0	1	0	0	*	*	*	Hi.	Set the Higher order 1bit page of DD RAM to the Page Address Register
	Page Address Set Lower Order 4bits	0	1	0	1	1	0	0	Lower Order Page Address				Set the Lower order 4 bit page of DD RAM to the Page Address Register
(d)	Column Address Set High Order 4bits	0	1	0	0	0	0	1	High Order Column Add.				Set the Higher order 4 bits Column Address to the Reg.
	Column Address Set Lower Order 4bits	0	1	0	0	0	0	0	Lower Order Column Add.				Set the Lower order 4 bits Column Address to the Reg.
(e)	Status Read	0	0	1	Status				0	0	0	0	Read out the internal Status
(f)	Write Display Data	1	1	0	Write Data								Write the data into the Display Data RAM
(g)	Read Display Data	1	0	1	Read Data								Read the data from the Display Data RAM
(h)	Normal or Inverse ON/OFF Set	0	1	0	1	0	1	0	0	1	1	0/1	Inverse the ON and OFF Display 0:Normal 1:Inverse
(i)	Static Drive ON /Normal Display	0	1	0	1	0	1	0	0	1	0	0/1	Whole Display Turns ON 0:Normal 1:Whole Disp. ON
(j)	Sub instruction table mode	0	1	0	0	1	1	1	0	0	0	0	Set the Sub instruction table.
Sub Inst.	(k)Partial Display												
	1st Block, Set Start display unit	0	1	0	0	0	0	0	Start display unit				Set the Start display unit of 1st Block.
	1st Block, Set The number of display units	0	1	0	0	0	0	1	number of display units				Set the number of display units of 1st Block.
	2nd Block, Set Start display unit	0	1	0	0	0	1	0	Start display unit				Set the Start display unit of 2nd Block.
	2nd Block, Set The number of display units	0	1	0	0	0	1	1	number of display units				Set the number of display units of 2nd Block.
	Partial display on	0	1	0	0	1	0	0	0	0	0	0	It comes off the mode to set and a display is executed.
	(l)n-line Inverse Drive Set												
	Register Set Higher order 2 bits	0	1	0	0	1	0	1	*	*	higher order		Set the number of inverse drive line.
	Register Set Lower order 4 bits	0	1	0	0	1	1	0	Lower order				Set the number of inverse drive line.
	n-line Inverse Drive Set is executed.	0	1	0	0	1	1	1	0	0	0	0	The execution of the line inverse drive.
	(m)EVR Register Set												
	EVR Register Set Higher order 4 bits	0	1	0	1	0	0	0	EVR Data Higher order				Set the V_5 output level to the EVR register. (Higher order 4 bits)
	EVR Register Set Lower order 4 bits	0	1	0	1	0	0	1	EVR Data Lower order				Set the V_5 output level to the EVR register. (Lower order 4 bits)
	EVR Register Set is executed.	0	1	0	1	0	1	0	0	0	0	0	The execution of the EVR.
(n)	End of sub instruction table mode	0	1	0	0	1	1	1	0	0	0	1	It ends the setting of sub instruction table.

(*:Don't Care)

Instruction		Code											Description
		A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(o)	Bias Select	0	1	0	1	0	1	1	*	Bias			Select the bias (8 Patterns)
(p)	Boost Level Select	0	1	0	0	0	1	1	0	0	Boost Multiple		Set the Booster circuits
(q)	Read Modify Write /End	0	1	0	1	1	1	0	0	0	0	0/1	Read Modify Write mode D0=0:On D0=1:End
(r)	Reset	0	1	0	1	1	1	0	0	0	1	0	Initialize the internal Circuits
(s)	Internal Power Supply ON/OFF	0	1	0	0	0	1	0	0	0	0	0/1	0:Int. Power Supply OFF 1:Int. Power Supply ON
(t)	Driver Outputs ON/OFF	0	1	0	0	0	1	0	0	0	1	0/1	D0=0: LCD Driver Outouts OFF D0=1: LCD Driver Outputs ON
(u)	Power Save (Complex Command)	0	1	0	1	0	1	0	1	1	1	0	Set the Power Save Mode (LCD Display OFF +Static Drive ON)
		0	1	0	1	0	1	0	0	1	0	1	
(v)	ADC Select	0	1	0	1	0	1	0	0	0	0	0/1	Set the DD RAM vs Segment D0=0:Normal D0=1:Inverse

(2-1) Explanation of Instruction Code

(a) Display On/Off

It executes the ON/OFF control of the whole display without relation to the DD RAM or any internal conditions.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

D 0:Display Off
1:Display On

(b) Display Start Line

It sets the DD RAM line address corresponding to the COM0 terminal (normally assigned to the top display line). In this instruction execution, the display area is automatically set by the lines that correspond to the display duty ratio to the upward direction of the line address. Changing the line address by this instruction performs smooth scrolling to a vertical direction. In this time, the DD RAM data are unchanged.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	0	1	A7	A6	A5	A4
0	1	0	0	1	1	0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Line Address(HEX)
0	0	0	0	0	0	0	0	00
0	0	0	0	0	0	0	1	01
				:				:
				:				:
1	0	0	1	1	1	1	1	9F

(c) Page Address Set

When MPU access to the DD RAM, a page address is set by page Address Set instruction before writing the data. (Note: the change of page address is not affected to the display.)

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	0	0	*	*	*	A4
0	1	0	1	1	0	0	A3	A2	A1	A0

(*:Don't Care)

A4	A3	A2	A1	A0	Page
0	0	0	0	0	0
0	0	0	0	1	1
		:			:
		:			:
1	0	0	1	1	19

(d) Column Address

When MPU accesses to the DD RAM , the row address set by Page Address Set instruction is required with the column address before writing the data. The column address set requires twice address set which are higher order 4 bits address set and lower order 4 bits.

When the MPU access to the DD RAM continuously, the column address increments automatically from the set address after each data access. Therefore, the MPU can transmit only the Data continuously without setting the column address at every transmission time. The increment of column address is stopped at the maximum column address plus 1 limited by each display mode. When the column address count up is stopped, the row address is not changed.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	0	0	1	A7	A6	A5	A4	Higher Order
0	1	0	0	0	0	0	A3	A2	A1	A0	Lower Order

A7	A6	A5	A4	A3	A2	A1	A0	Column Address(HEX)
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
				:				:
				:				:
1	0	0	0	0	0	1	1	83

(e) Status Read

This instruction reads out the internal status of "BUSY", “ADC", "ON/OFF" and "RESET" described as follows.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY : BUSY=1 indicate the operating or the Reset cycle.
All instructions can be input after the BUSY status change to "0".

ADC : Indicate the output correspondence of column (segment) address and segment driver.
0 :Counterclockwise Output (Inverse)
1 :Clockwise Output (Normal)
(Note) The data "0=Inverse" and "1=Normal" of ADC status is inverted with the ADC select Instruction of "1=Inverse" and "0=Normal".

ON/OFF : Indicate the whole display On/Off status.
0 : Whole Display "On
1 : Whole Display "Off"
(Note) The data "0=On" and "1=Off" of Display On/Off status is inverted with the Display On/Off instruction data of "1=On" and "0=Off".

RESET : Indicate the initializing by $\overline{RES}$ terminal signal or reset instruction.
0 : Not Reset status
1 : In the Reset status

(f) Write Display Data

It writes the data on the data bus into the DD RAM. column address increments automatically after data writing, therefore, the MPU can write the data into the DD RAM continuously without the address setting at every writing time once the starting address is set.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	WRITE DATA							

(g) Read Display Data

This instruction reads out the 8-bit data from DD RAM addressed by the column and the page address. The column address automatically increments after the 8-bit data read out, therefore, the MPU can read the data from the DD RAM continuously without the address setting at every reading time once the starting address is set. Note that the dummy read is required just after setting the column address (see “(4-4) Access to the DD RAM and the Internal Register”).

In the serial interface mode, the display data is unable to read out.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	READ DATA							

(h) Normal or Inverse On/Off Set

It changes the display condition of normal or reverse for entire display area. The execution of this instruction does not change the display data in the DD RAM.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	D

D 0 : Normal RAM data "1" correspond to "On"

1 : Inverse RAM data "0" correspond to "On"

(i) Static Drive

This instruction turns all the pixels ON regardless the data stored in the DD RAM. In this time, the data in DD RAM are remained and unchanged. This instruction is executed prior to the "Normal or Inverse On/Off Set" Instruction.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

D 0 : Normal Display

1 : Whole Display turns On

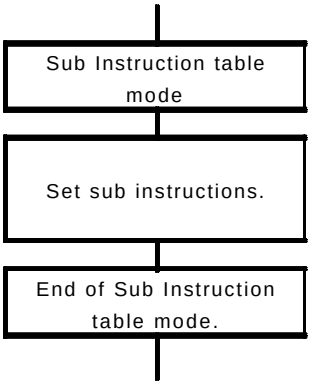
When the “Static Drive ON” instruction is executed at Display OFF status, the **NJU6678V** operates in Power Save Mode. (Refer “ Power Save Mode “)

(j) Sub Instruction table mode

This instruction switches the instruction table from the main to the sub. The sub instruction table contains instructions of partial display, n-line inverse drive set and EVR register set as mentioned in (k), (l) and (m).
The instruction of sub instruction table mode must be executed before above 3 sub instructions execution. The instruction of end of sub instruction table mode (n) switches the instruction table from the sub to the main. If any main instructions are written in the sub instruction mode, the **NJU6678V** will malfunction.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	1	1	0	0	0	0

-Set sub Instruction table flow is shown below:



Switches to Sub instruction table mode.

Switches to Main instruction mode.

(k) Partial Display

It selects two active display areas on the LCD Panel partially. The display area is divided to 13 units with four commons each and selected two display blocks by setting Unit number and number of Unit required (not overlap, not over than 13 units) to display on the LCD panel. These two display blocks are assigned optionally on the LCD panel. Duty selects an adapted ratio number corresponding to the total number of two display blocks automatically.
Partial Display function adjusts the LCD driving voltage, Voltage boosting times and E.V.R level by the instruction to generate the optimum LCD driving voltage for display quality. As result, the operating current is reduced.

· Display Unit Structure

UNIT	0	(8 commons)
UNIT	1	
UNIT	2	
UNIT	3	
UNIT	4	
UNIT	5	
UNIT	6	
UNIT	7	
UNIT	8	
UNIT	9	
UNIT	10	
UNIT	11	
UNIT	12	(8 commons)

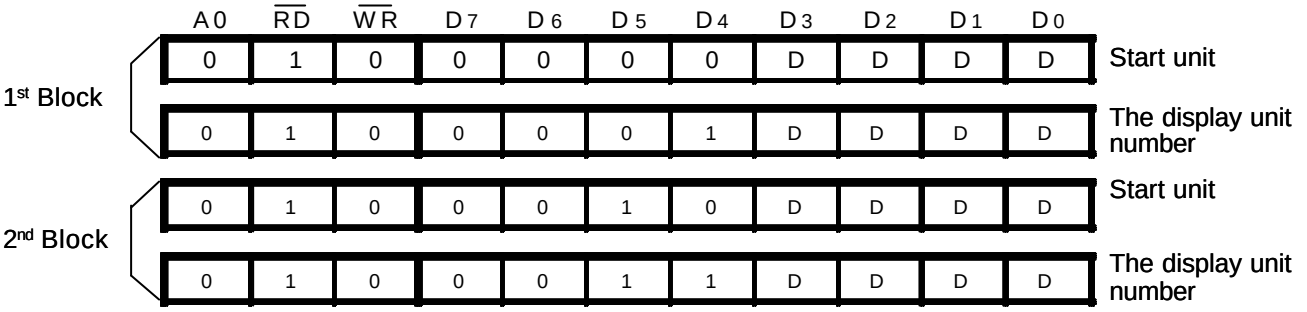
104-common

132-segment

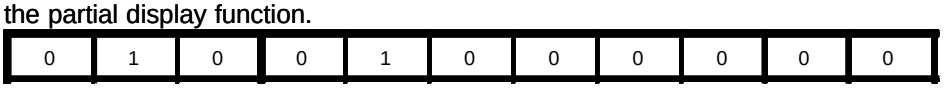
Partial display instruction

When Partial Display functions, both of Top Unit Number of display area (the Start Unit) and the number of the effective continuous unit (Display Unit) from the Start Unit for the first display block and the second. Attention that the first display block and the second definition must not be overlap of display area and not be over than 13 units in total.

In case of whole display (1/104 duty), the first display block defines Start Unit=0 (0,0,0,0) and Display Unit = 13 (1,1,0,1) for all of display area selection. In this time, the definition of the second display block is ignored.
In case of only the first block display, the second display block defines Start Unit=0 (0,0,0,0) and Display Unit = 0 (0,0,0,0) for no display area.



By input following instruction, the duty ratio is changed automatically and executes the partial display function.

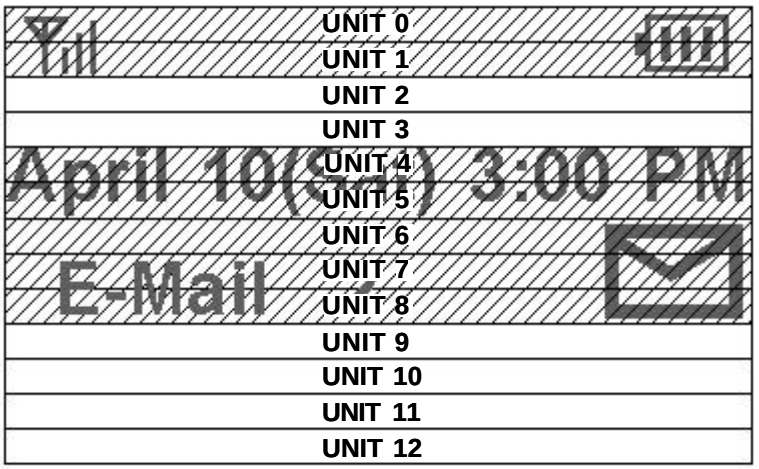


D :unit number (Hex.)

Notes) Attention followings due to prevent from mulfunction

- The input order of Partial Display instructions must follow above.
- Prohibits the overlap of the 1st partial display block and the 2nd.
- The Start Unit of the 1st partial display block must not be over 12.
- The total Display Unit Number (the sum of the 1st and 2nd partial display block Unit Num ber) must not be over 13.
- On the LCD panel, no active display area inserts between the 1st display block and the 2nd. However, the display data of the 1st display block and the 2nd must store continuously in the display data RAM.

Example of the Partial Display setting.



The above partial display condition is set as follows:

1)Set sub instruction mode

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	1	1	1	0	0	0	0	Set sub instruction mode.

2)Set partial display conditions

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	0	0	0	0	0	0	0	1st Block, Set start unit to "0"
0	1	0	0	0	0	1	0	0	1	0	1st Block, Set the display unit number to "2"
0	1	0	0	0	1	0	0	1	0	0	2nd Block, Set start unit to "4"
0	1	0	0	0	1	1	0	1	0	1	2nd Block, Set the display units number to "5"
0	1	0	0	1	0	0	0	0	0	0	Execute Partial display.

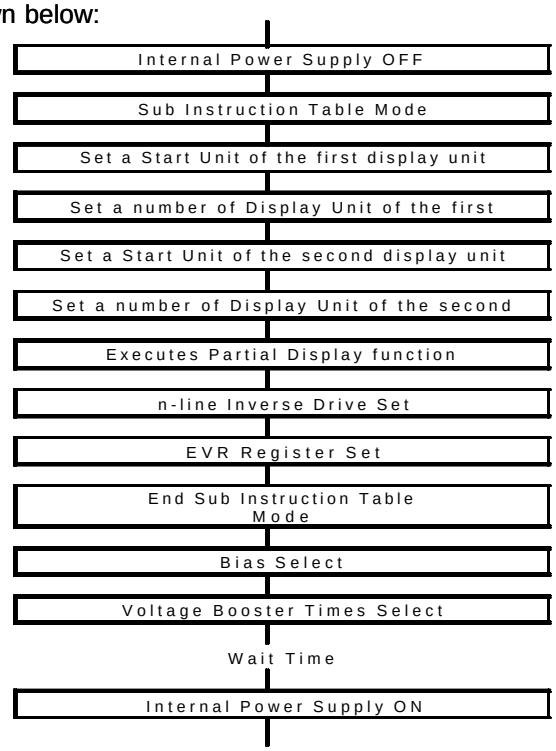
The Duty is changed to 1/56 automatically.

3)End sub instruction mode

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	1	1	1	0	0	0	1	End sub instruction mode. Back to main instruction mode.

Duty is changed automatically when Partial Display execution. But LCD Driving Voltage, Bias, Driving form like as 2-frame alternating driving or n-line inverse are not changed. Therefore, Display Off should operate before Partial Display execution for prevention of unexpected display, and Voltage Booster Select instruction, E.V.R Register Set, Bias Select and n-line Inverse Driving Set should set optimum conditions for good display in the mean time of Partial Display instruction execution. The optimum conditions should fix refering the result of actual display eveluation.

-Set Partial Display flow is shown below:



(l) n-line Inverse Drive Mode

n-Line Inverse Register Set (refer +Functional Description Fig.3 n-line Inverse alternative drive mode)
It sets a line number to inverse the polarity of common driver and segment.
The instructions must be input in order of followings. These instructions are sub instruction sets and must be set after (j)Sub instruction table mode.

1)Set sub instruction mode

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	1	1	1	0	0	0	0	Set sub instruction mode.

2)Set n-line Inverse number

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	1	0	1	*	*	A5	A4	Higher order
0	1	0	0	1	1	0	A3	A2	A1	A0	Low order

A5	A4	A3	A2	A1	A0	Inverse line
0	0	0	0	0	0	-(*)
0	0	0	0	0	1	2
			:			:
1	1	1	1	1	1	64

(*:2-frame alternating drive mode.)

3)Execute the n-line Inverse

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	1	1	0	0	0	0

4)End sub instruction mode

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	1	1	1	0	0	0	1	End sub instruction mode. Back to main instruction mode.

(m) EVR Register Set

It controls the voltage regulator circuit of the internal LCD power supply to adjust the LCD display contrast by changing the LCD driving voltage “V5”. By data setting into the EVR register, the LCD driving voltage “V5” selects out of 201 steps of regulated voltage. The voltage adjustable range of “V5” is fixed by the external resistors. For details, refer the section “(3-2) Voltage Adjust Circuits”.

1)Set sub instruction mode

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	1	1	1	0	0	0	0	Set sub instruction mode.

2)Set EVR Register

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	A7	A6	A5	A4
0	1	0	1	0	0	1	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	VLCD
0	0	1	1	0	1	1	1	Low
			:					:
			:					:
1	1	1	1	1	1	1	1	High

$V_{LCD}=V_{DD}-V5$

When EVR doesn't use, set the EVR register to (1,1,1,1,1,1,1,1).

3)Execute the EVR

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	0

4)End sub instruction mode

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	1	1	1	0	0	0	1	End sub instruction mode. Back to main instruction mode.

(n) End of Sub instruction table mode

"End of sub instruction table mode" instruction switches instruction table from sub to main.
(k)Partial display, (l)n-line inverse drive mode, and (m)EVR are sub instruction sets on the sub instruction table. The instruction of “END of sub instruction mode” must be set after these sub instruction sets. The **NJU6678V** may occur incorrect operation if any main instructions on the main instruction table are input in mode of sub instruction table.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	1	1	0	0	0	1

(o) Bias Select

This instruction sets the bias voltage.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	1	*	A2	A1	A0	(*:Don't Care)

A2	A1	A0	Bias
0	0	0	1/4
0	0	1	1/5
0	1	0	1/6
0	1	1	1/7
1	0	0	1/8
1	0	1	1/9
1	1	0	1/10
1	1	1	1/11

(p) Boost Level Select

This instruction sets the boost level (2 to 5 times). When “Partial Display Instruction” execution, the “Boost Level Select” also must be executed. If the external capasitors are connected as the lower than 5 times boost level, don’t set the boost level by the instruction over than the boost level by conecting capasitors. If set the boost level over than it, the device will make malfunction.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	1	0	0	A1	A0

Command		Booster Multiple			
A1	A0	5times external capacitors connections	4times external capacitors connections	3times external capacitors connections	2times external capacitors connections
0	0	2-time			
0	1	3-time	2-time		
1	0	4-time	3-time	2-time	
1	1	5-time	4-time	3-time	2-time

(q) Read Modify Write/End

This instruction sets the Read Modify Write controlling the page address increment. In this mode, the Column Address only increments when execute the display data “Write” instruction; but no change when the display data “Read” Instruction. This status is continued until the End instruction execution. When the End instruction is executed, the Column Adddress goes back to the start address before the execution of this “Read Modify Write” instruction. This function reduces the load of MPU for repeating display data change of the fixed area (ex. cursor blink).

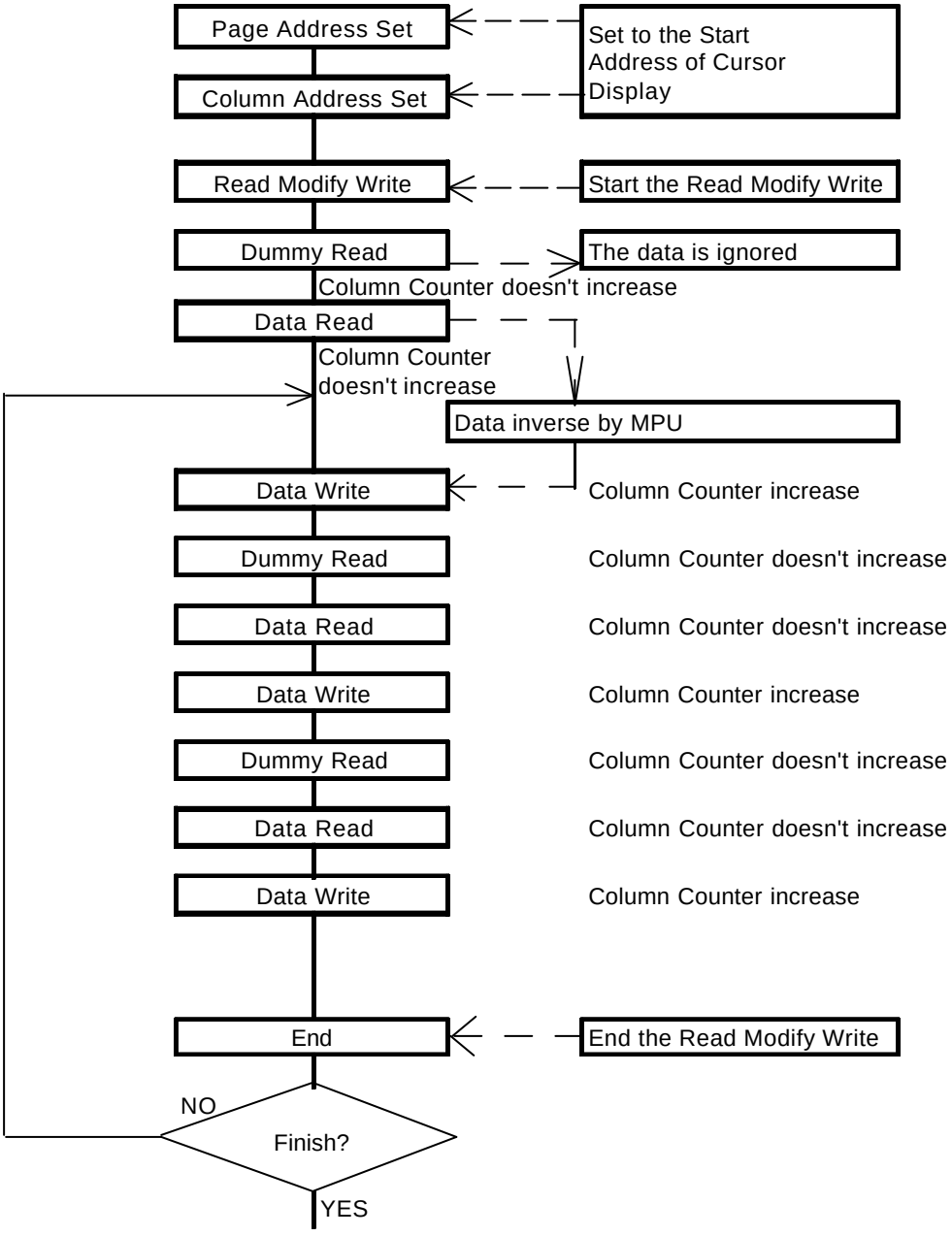
A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	D

D 0 : Read Modify Write On

1 : End

Note) In this “Read Modify Write” mode, out of display dara “Read”/”Write”, any instructions except “Column Address Set” can be executed.

- The Example of Read Modify Write Sequence



(r) Reset

This instruction executes the following initialization.
The reset by the reset signal input to the RES terminal (hardware reset) is required when power turns on. This reset instruction does not use instead of this hardware reset when power turns on.

Initialization

1 Set the Column Address Counter to 00H
2 Set the Display Start Line Register to 00H
3 Set the Page Address Register to page "0"
4 Set the EVR register to FFH
5 Set the Partial Display(1/104 duty)
6 Set the Bias select(1/11 Bias)
7 Set the Voltage Booster(5 times)
8 Set the n-line inverse register to 0H

The DD RAM is not affected by this initialization.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

(s) Internal Power Supply ON/OFF

This instruction control ON and OFF for the internal Voltage Converter, Voltage Regulator and Voltage Follower circuits. For the Booster circuits operation, the oscillation circuits must be in operation.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	0	0	D

D 0 : Internal Power Supply Off
1 : Internal Power Supply On

The internal Power Supply must be Off when external power supply using.

*1 The set up period of internal power supply On depends on the step up capacitors, voltage stabilizer capacitors, V_{DD} and V_{LCD}.
Therefore it requires the actual evaluation using the LCD module to get the correct time. (Refer to the (3-4) Fig.5)

(t) Driver Outputs ON/OFF

This instruction controlls ON/OFF of the LCD Driver Outputs.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	0	1	D

D 0 : LCD driving waveform output Off

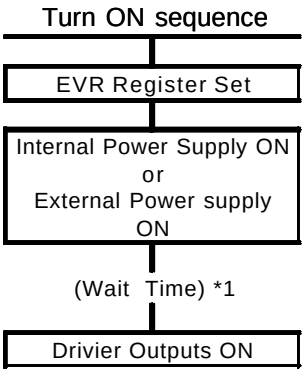
1 : LCD driving waveform output On

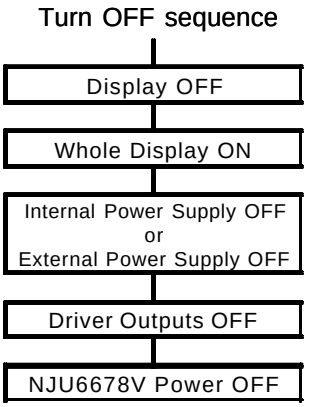
The **NJU6678V** implements low power LCD driving voltage generator circuit and requires the following Power Supply ON/OFF sequence.

- LCD Driving Power Supply ON/OFF Sequences

The sequences below are required when the power supply turns ON/OFF.

For the power supply turning on operation after the power-save mode, refer the ”power save release sequence” mentioned after.





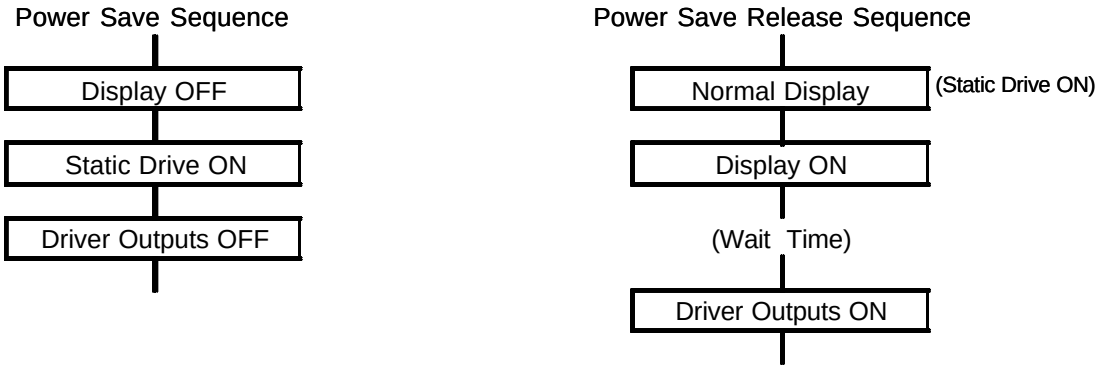
*1 The Internal Power Supply rise time is depending on the condition of the Supply Voltage, VLCD=VDD-V5, External Capacitor of Booster, and External Capacitor connected to V1 to V5. To know the rise time correctly, test by using the actual LCD module.

(u) Power Save (complex comand)

When Static Drive ON at the Display OFF status (inverse order also same), the internal circuits goes to the Power Save Mode and the operating current is dramatically reduced, almost same as the standby current.
The internal status in the Power Save Mode is shown as follows;

1: The Oscillation Circuits and the Internal Power Supply Circuits stop the operation.
2: LCD driving is stopped. Segment and Common drivers output V_{DD} level voltage.
3: The display data and the internal operating condition are remained and kept as just before enter the Power Save Mode.
4: All the LCD driving bias voltage (V1 to V5) is fixed to the V_{DD} level.

The power save and its release perform according to the following sequences.



The **NJU6678V** constantly spends the current without the execution of the Driver Outputs OFF instruction. The LCD drive waveform is not output until the Driver Outputs ON instruction is executed.

*1 In the Power Save sequence, the Power Save Mode starts after the Static Drive ON command is executed.
*2 In the Power Save Release sequence, the Power Save Mode releases just after the Static Drive OFF instruction execution. The Display ON instruction is allowed to execute at any time after the Static Drive OFF instruction is completed.
*3 The Internal Power Supply rise time is depending on the condition of the Supply Voltage, $V_{LCD}=V_{DD}-V5$, External Capacitor of Booster, and External Capacitor connected to V1 to V5. To know the rise time cor rectly, test by using the actual LCD module.
*4 LCD driving waveform is output after the exection of the Driver Outputs ON instruction execution.
*5 In case of the external power supply operation, the external power supply should be turned off before the Power Save Mode and connected to the V_{DD} for fixing the voltage. In this time, V_{OUT} terminal also should be made codition like as disconection or connection to V_{SS}.

(v) ADC Select

This instruction determines the correspondence of Column in the DD RAM with the Segment Driver Outputs. Segment Driver Output order is inversed when this instruction executes, therefore, the placement the **NJU6678V** against the LCD panel becomes easy.

A0	$\overline{RD}$	R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	D

D 0 : Clockwise Output (Normal) Segment Driver S_0 to S_{131}
1 : Counterclockwise Output (Inverse) Segment Driver S_{131} to S_0

(3) Internal Power Supply

(3-1) 5-time voltage booster circuits

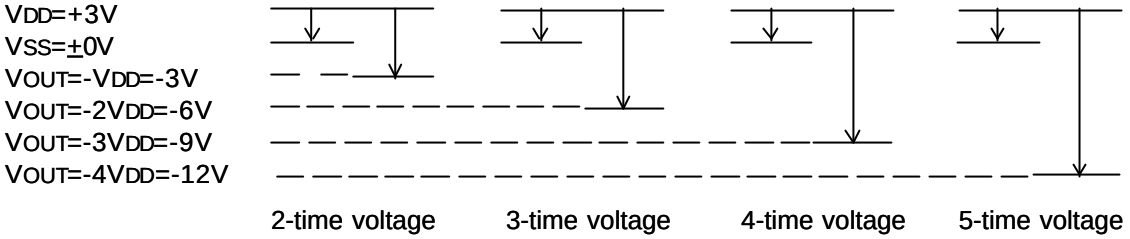
The 5-time voltage booster circuit outputs the negative Voltage(V_{DD} Common) boosted 5 times of V_{DD}-V_{SS} from the V_{OUT} terminal with connecting the five capacitors between C_1^+ and C_1^-, C_2^+ and C_2^-, C_3^+ and C_3^-, C_4^+ and C_4^-, and V_{SS} and V_{OUT}. The boosting time is selected out of 2 times to 5 by the combination of changing the external capacitors connection and "Booster Level Select" instruction. (refer (2-1)Instruction (p)Voltage Boost time select)

Voltage Booster circuits requires the clock signals from internal oscillation circuit or the external clock signal, therefore, the internal oscillation circuits or the external clock supplier must be operating when the voltage booster is in operation.

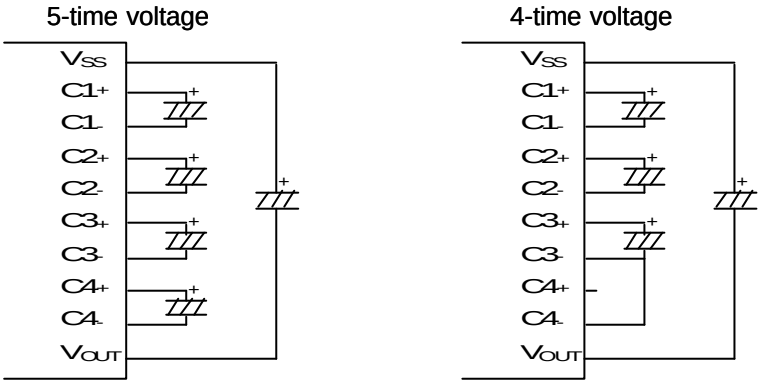
The boosted voltage of V_{DD}-V_{OUT} must be 17V or less.

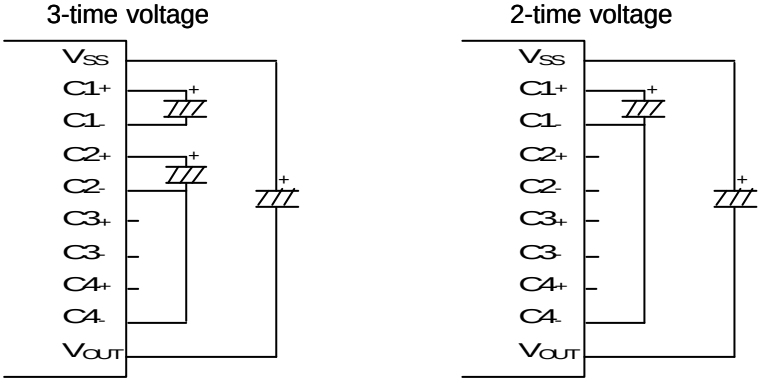
The boost voltage and the capacitor connection are shown below.

● The boosted voltage and V_{DD},V_{SS}



● Example of the external capacitor connection to the voltage booster circuits





(3-2)Voltage Adjust Circuits

The boosted voltage of V_{OUT} outputs V5 for LCD driving through the voltage adjust circuits. The output voltage of V5 is adjusted by Ra and Rb within the range of $|V5| < |V_{OUT}|$.
The output is calculated by the following formula(1).

$$V_{LCD} = V_{DD}-V_5 = (1+Rb/Ra)V_{REG} \quad (1)$$

The V_{REG} voltage is a reference voltage generated by the built-in bleeder registance. V_{REG} is adjustable by EVR functions (see section 3-3).
For minor adjustment of V5, it is recommended that the Ra and Rb is composed of R2 as variable resistor and R1 and R3 as fixed resistors, constant should be connected to V_{DD} terminal,VR and V5 ,as shown below.

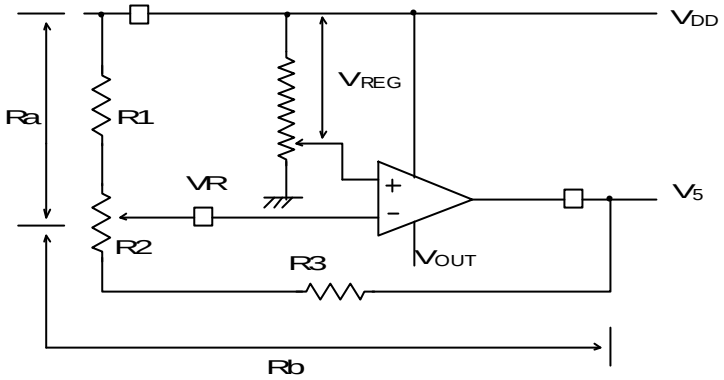


Fig. 4

< Design example for R1, R2 and R3 /Reference >

- R1+R2+R3=6MΩ
  (Determind by the current between V_{DD}-V5)
- Variable voltage range by the R2. -7V to -11V ($V_{LCD}=V_{DD}$-V5 : 10V to 12V)
  (Determind by the LCD electrical characteristics)
- VREG=3V
  (In case of V_{DD}=3V and EVR=FFh)

R1,R2 and R3 are calculated by above conditions and the fomula of (1) to below;

R1=1.5MΩ
R2=0.3MΩ
R3=4.2MΩ

Note) V5 voltage is generated referencing with VREG voltage beased on the supply voltage (V_{DD} and V_{SS}) as shown in above figure. Therefore, V_{LCD} (V_{DD}-V5) is affected including the gain (Rb/Ra) by the fluctuation of V_{REG} voltage based on the supply voltage. The power supply voltage should be stabilized for V5 stable operation.

(3-3) Contrast Adjustment by the EVR function

The EVR selects the V_{REG} voltage out of the following 201 conditions by setting 8-bit data into the EVR register. With the EVR function, V_{REG} is controlled, and the LCD display contrast is adjusted. The EVR controls the voltage of V_{REG} by instruction and changes the voltage of V5.
A step with EVR is set like table shown below.
37H to 4FH available for use. If keeping 3% precision, sets EVR over 4FH.

EVR register		V_{REG}[V]	V_{LCD}
3FH	(0,0,1,1,0,1,1,1)	(100/300) x (V_{DD}-V_{SS})	Low
:	:	:	:
4FH	(0,1,0,0,1,1,1,1)	(124/300) x (V_{DD}-V_{SS})	:
:	:	:	:
:	:	:	:
FDH	(1,1,1,1,1,1,0,1)	(298/300) x (V_{DD}-V_{SS})	:
FEH	(1,1,1,1,1,1,1,0)	(299/300) x (V_{DD}-V_{SS})	:
FFH	(1,1,1,1,1,1,1,1)	(300/300) x (V_{DD}-V_{SS})	High

In use of the EVR function, the voltage adjustment circuit must turn on by the power supply instruction.

● Adjustable range of the LCD driving voltage by EVR function

The adjustable range is decided by the power supply voltage V_{DD} and the ratio of external resistors Ra and Rb.

[Design example for the adjustable range / Reference]

- Condition V_{DD}=3.0V, V_{SS}=0V
  Ra=1MΩ, Rb=4MΩ (Ra:Rb=1:4)

The adjustable range and the step voltage are calculated as follows in the above condition.

In case of setting 4FH in the EVR register,

V_{LCD} = ((Ra+Rb)/Ra)V_{REG}
= (5/1) x [(124/300) x 3.0]
= 6.2V

In case of setting FFH in the EVR register,

V_{LCD} = ((Ra+Rb)/Ra)V_{REG}
= (5/1) x [(300/300) x 3.0]
= 15.0V

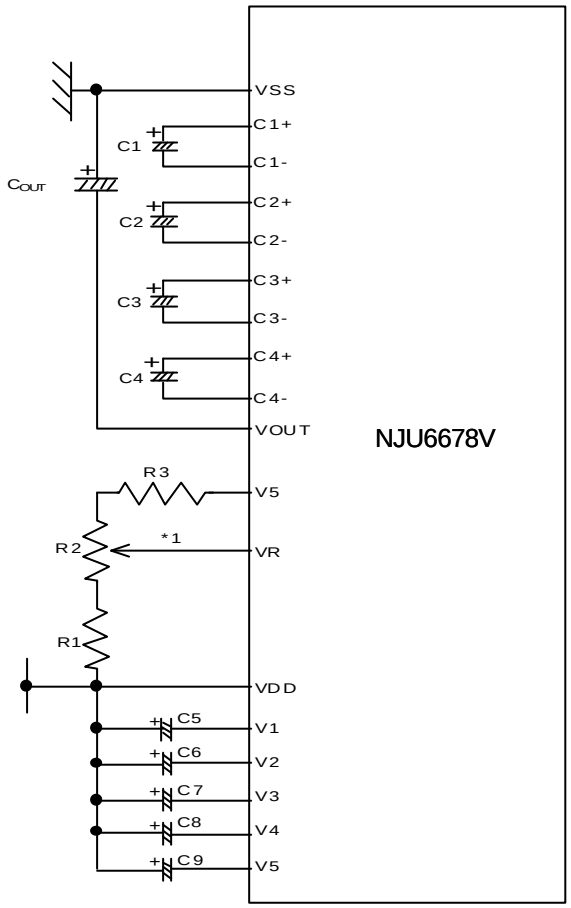
	Min.4FH		Max.FFH
Adjustable Range	6.2	- - - - - - - - - - - - - - - - - -	15.0 [V]
Step Voltagre	50		[mV]

* In case of V_{DD}=3V

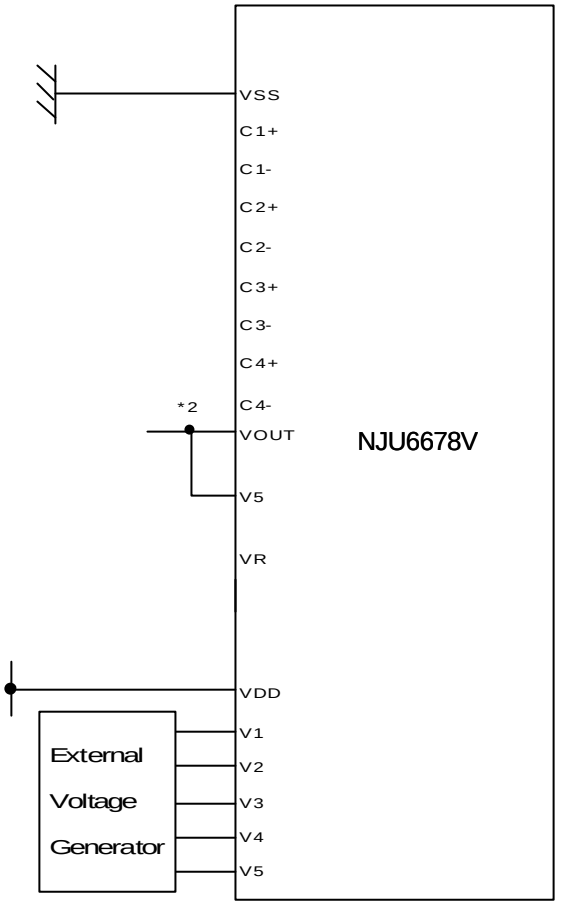
(3-4) LCD Driving Voltage Generation Circuits

The LCD driving bias voltage of V_1,V_2,V_3,V_4 are generated by dividing the V_5 voltage with the internal bleeder resistance and is supplied to the LCD driving circuits after the impedence conversion by the voltage follower.
As shown in Figure 5, five external capacitors are required to connect to each LCD driving voltage terminal for voltage stabilization. The value of capacitors (C_5 to C_9) should be determined after the actual LCD panel display evaluation.

Using the internal Power Supply



Using the external Power Supply



Reference set up value $V_{LCD}=V_{DD}-V5$ = 10 to 12V

C_{OUT}	to 1uF
C1 to C4, C9	to 1uF
C5 to C8	0.1 to 0.47uF
R1	1.5MΩ
R2	0.3MΩ
R3	4.2MΩ

Fig.5

*1 Short wiring or sealed wiring to the VR terminal is required due to the high impedance of VR terminal.
*2 Following connection of V_{OUT} is required when external power supply using.
When $V_{SS} > V5$ --- $V_{OUT}=V5$
When $V_{SS} \leq V5$ --- $V_{OUT}=V_{SS}$

(4) MPU Interface

(4-1) Interface type selection

Two MPU interface types are available in the **NJU6678V**: by 1) 8-bit bi-directional data bus (D7 to D0), 2) serial data input (SI:D7). The interface type (the 8 bit parallel or serial interface) is determined by the condition of the P/S terminals connecting to "H" or "L" level as shown in Table 5. In case of the serial interface, neither the status read-out nor the RAM data read-out operation is allowed.

Table 5

P/S	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	SEL68	D_7	D_6	D_0 to D_5
H	Parallel	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	SEL68	D_7	D_6	D_0 to D_5
L	Serial	$\overline{CS}$	A0	-	-	-	SI	SCL	Hi-Z

Parallel Interface

The **NJU6678V** interfaces the 68- or 80-type MPU directly if the parallel interface (P/S="H") is selected.
The 68-type or 80-type MPU is selected by connecting the SEL68 terminal to "H" or "L" as shown in table 6.

Table 6

SEL68	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7
H	68 type MPU	$\overline{CS}$	A0	E	R/W	D0 to D7
L	80 type MPU	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7

(4-2) Discrimination of Data Bus Signal

The **NJU6678V** discriminates the mean of signal on the data bus by the combination of A0, E, R/W, and ($\overline{RD}$,$\overline{WR}$) signals as shown in Table 7.

Table 7

Common	68 type	80 type		Function
A0	R/W	$\overline{RD}$	$\overline{WR}$	
H	H	L	H	Read Display Data
H	L	H	L	Write Display Data
L	H	L	H	Status Read
L	L	H	L	Write into the Register(Instruction)

(4-3) Serial Interface.(P/S="L")

The serial interface of the **NJU6678V** consists of the 8-bit shift register and 3-bit counter. In case the chip is selected ($\overline{CS}$=L), the input to D7(SI) and D6(SCL) becomes available, and in case that the chip isn't selected, the shift register and the counter are reset to the initial condition.
The data input from the terminal(SI) is MSB first like as the order of D7, D6, ●●●D0 by a serial interface, it is entered into with rise edge of serial clock(SCL). The data converted into parallel data of 8-bit with the rise edge of 8th serial clock and processed.
It discriminates display data or instructions by A0 input terminal. A0 is read with rise edge of (8 X n)th of serial clock (SCL), it is recognized display data by A0=H" and instruction by A0="L". A0 input is read in the rise edge of (8 X n)th of serial clock (SCL) after chip select and distinguished.
However,in case of RES="H" to "L" or $\overline{CS}$="L" to "H" with trasfered data does not fill 8 bit, attention is necessary because it will processed as there was command input. Always, input the data of (8 X n) style.
The SCL signal must be careful of the termination reflection by the wiring length and the external noise and confirmation by the actual machine is recommended by it.

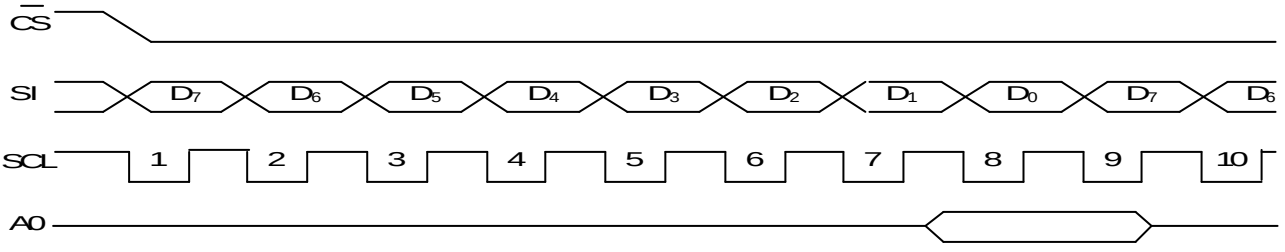


Fig. 6

(4-4) Access to the Display Data RAM and Internal Register.

The **NJU6678V** transfers data to the CPU through the bus holder with the internal data bus.

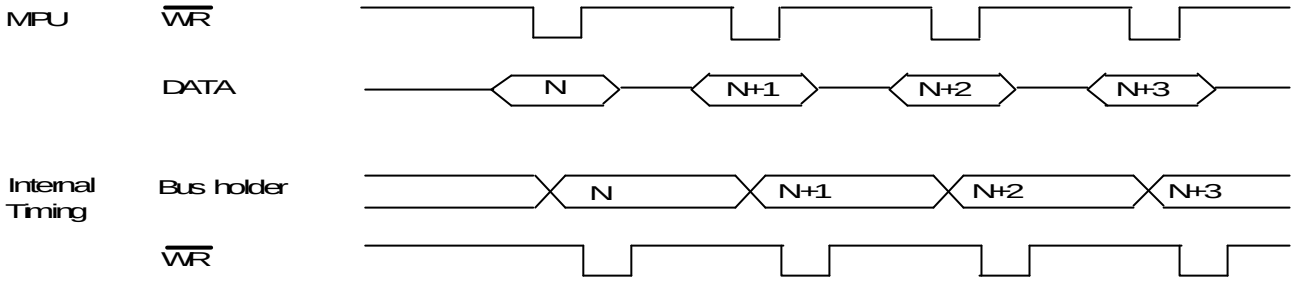
In case of reading out the display data contents in the DD RAM, the data which was read in the first data read cycle (= the dummy read) is memorized in the bus holder. Then the data is read out to the system bus from the bus holder in the next data read cycle. Also, In case that the MPU writes into DD RAM, the data is temporarily stored in the bus holder and is then written into DD RAM by the next data write cycle.

Therefore, the limitation of the access to **NJU6678V** from MPU side is not access time (t_{ACC},t_{DS}) of Display Data RAM and the cycle time becomes dominant. With this, speed-up of the data transfer with the MPU becomes possible. In case of cycle time isn't met, the MPU inserts NOP operation only and becomes an equivalent to an execution of wait operation on the sutisfy condition in MPU.

When setting an address, the data of the specified address isn't output immediately by the read operation after setting an address, and the data of the specified address is output at the the 2nd data read operation. Therefore, the dummy read is always necessary once after the address set and the write cycle. (See Fig. 7)

The exsample of Read Modify Write operaion is mentioned in (2-1)Instruction –(q)The sequence of Inverse Display.

● Write Operation



● Read Operation

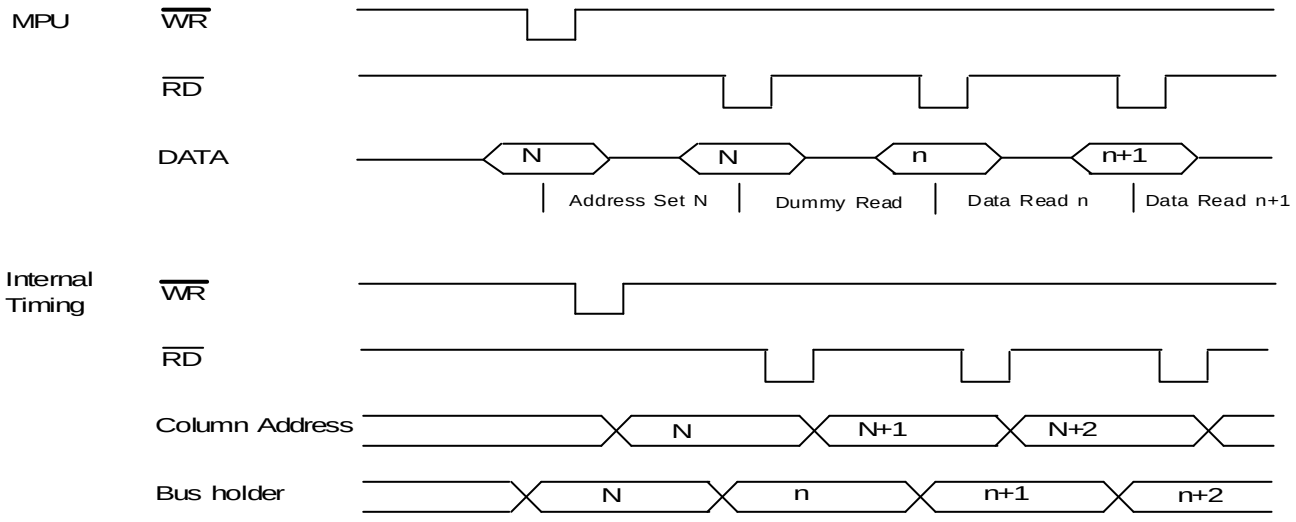


Fig.7

(4-6) Chip Select

$\overline{CS}$ is the Chip Select terminal. In case of $\overline{CS}$="L", the interface with MPU is available.

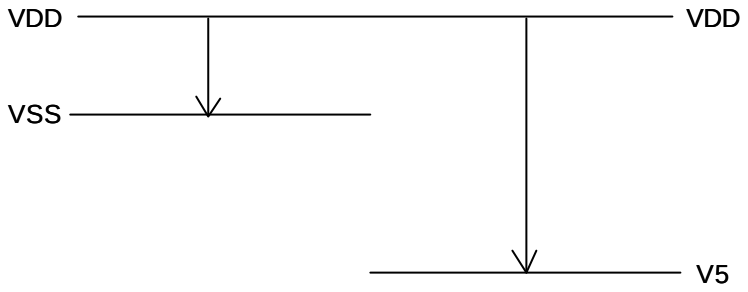
In case of $\overline{CS}$="H" (Chip is not selected), the terminals of D_0 to D_7 are high impedance and A0, $\overline{RD}$, $\overline{WR}$, D_7(SI) and D_6(SCL) inputs are ignored. If the serial interface is selected when $\overline{CS}$="H", the shift register and the counter for the serial interface are reset.

However, the reset signal is always input and executed in any conditions of $\overline{CS}$.

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (1)	V_{DD}	-0.3 to +5.0	V
Supply Voltage (2)	V_5	V_{DD}-17.0 to V_{DD}+0.3	V
Supply Voltage (3)	V_1 to V_4	V_5 to V_{DD}+0.3	V
Input Voltage	V_{IN}	-0.3 to V_{DD}+0.3	V
Operating Temperature	T_{opr}	-30 to +80	°C
Storage Temperature	T_{stg}	-55 to +125 (Chip)	°C
		-55 to +100 (TCP)	



Note 1) All voltage values are specified as V_{SS}=0V.

Note 2) The relation of $V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5 > VOUT; V_{DD} > V_{SS} \geq V_{OUT}$ must be maintained.
In case of inputting external LCD driving voltage , the LCD drive voltage should start supplying to **NJU6678V** at the mean time of turning on V_{DD} power supply or after turned on V_{DD} .
In use of the voltage boost circuit, the condition that the supply voltage: $17.0V \geq V_{DD}-V_{OUT}$ is necessary.

Note 3) If the LSI are used on condition beyond the absolute maximum rating, the LSI may be destroyed.
Using LSI within electrical characteristics is strongly recommended for normal operation.
Use beyond the erectric characteristics conditions will cause malfunction and poor reliability.

Note 4) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the voltage converter.

■ ELECTRICAL CHARACTERISTICS (1) (VDD=2.5V to 3.3V, VSS=0V, Ta=-30 to +80°C)

PARAMETE		SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	Note
Operating Voltage(1)		V_{DD}			2.5		3.3	V	5
Operating Voltage(2)		V_5			V_{DD}-17.0		V_{DD}-6.0	V	6
		V_1,V_2	V_{LCD}= V_{DD}-V_5		VDD-0.5VLCD		V_{DD}		
		V_3,V_4			V_5		VDD-0.5VLCD		
Input Voltage	High Level	V_{IHC1}	D0...D7,A0, CS,RES,RD,WR,SEL68, P/S Terminals		0.8V_{DD}		V_{DD}	V	
	Low Level	V_{ILC1}			V_{SS}		0.2V_{DD}	V	
Output Voltage	High Level	V_{OHC11}	D0...D7 Terminals	I_{OH}=-0.5mA	0.8V_{DD}		V_{DD}	V	
	Low Level	V_{OLC11}		I_{OL}= 0.5mA	V_{SS}		0.2V_{DD}	V	
Input Leakage Current		I_{LIO}	All Input terminals		- 1.0		1.0	uA	
Driver On-resistance		R_{ON1}	Ta=25°C	V_{LCD}=15.0V		2.0	3.0	kΩ	7
		R_{ON2}		V_{LCD}=8.0V		3.0	4.5		
Stand-by Current		I_{DDQ}	during Power save Mode			0.05	5	uA	8
Operating Current		I_{DD12}	Display V_{LCD}=12.0V			15	40	uA	
		I_{DD21}	Accessing f_{CYC}=200kHz			600	800		9
Input Terminal Capacitance		C_{IN}	A0,$\overline{CS}$,$\overline{RES}$,$\overline{RD}$,$\overline{WR}$,SEL68, P/S,T1,T2,D0...D7 Ta=25°C			10		pF	10
Oscillation Frequency		f_{OSC}	Ta=25°C		26	32	38	kHz	

Reset time	t_R	$\overline{RES}$ Terminal	1.0			us	11
Reset "L" Level Pulse Width	t_{RW}	$\overline{RES}$ Terminal	10			us	12

Voltage Booster	Output Volt.	V_{OUT1}	V_{SS}-Vout, 5-time voltage booster, V_{DD}=3V	V_{DD}-15.0V		V_{DD}-14.5V	V	
	On-resistance	R_{TRI}	V_{DD}=3V;C_{OUT}=1.0uF 5-time voltage booster		4000	6000	Ω	
	Adjustment range of LCD Driving Volt.	V_{OUT2}	Voltage Booster Circuit "OFF"	V_{DD}-17.0V		V_{DD}-6.0V	V	13
	Voltage Follower	V_5	Voltage Adjustment Circuit "OFF"	V_{DD}-17.0V		V_{DD}-6.0V	V	
	Operating Current	I_{OUT1}	V_{DD}=3V, V_{LCD}=12V COM/SEG Terminals Open No Access Display Checkered pattern		160	320	uA	14
		I_{OUT2}			35	70		
		I_{OUT3}			25	50		
	Voltage Reg.	$V_{REG\%}$	V_{DD}=3V,Ta=25°C, V_{REG}=4F to FFH			3	%	

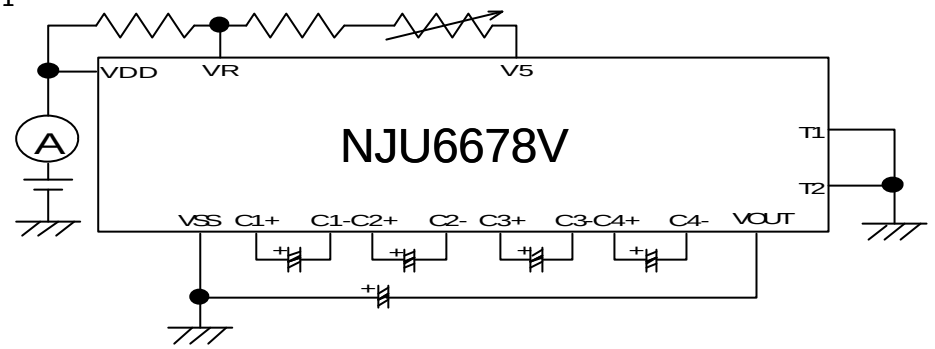
Note 5) Although the **NJU6678V** can operate in wide range of the operating voltage, it shall not be guaranteed in a sudden voltage fluctuation during the access with MPU.
Note 6) The operating voltage when using external power supply.
Note 7) R_{ON} is the resistance values in supplying 0.1V voltage-difference beteen power supply terminals (V1,V2,V3,V4) and each output terminals (common/ segment). This is specified within the range of Operating Voltage(2).
Note 8,9) The value of after Driver Output On instruction execution.
Note 8,9) Refers to the current consumption of the IC itself; external power supply is used for the LCD driving. In case of not use internal power supply circuit,meaning current of IC's. LCD driving power supply are external power supply.
Note 8) Applicable in case of not accessing to the MPU.
Note 9) The operating current when writing a vertical stripe pattern on the tcyc. Current consumption during the access is approximately proportional to the access frequency. When not accessed, it consumpts only I_{DD01}
Note 10) Apply to A0, D_0-D_7, $\overline{RD}$,$\overline{WR}$,$\overline{CS}$,$\overline{RES}$,SEL68,P/S,T_1,T_2 terminals.

Note 11) t_R (Reset Time) refers to the reset completion time of the internal circuits from the rise edge of the $\overline{RES}$ signal.
Note 12) Apply minimum pulse width of the $\overline{RES}$ signal. To reset, the "L" pulse over t_{RW} shall be input. .
Note 13) The voltage adjustment circuit controls V5 within the range of the voltage follower operating voltage.
Note 14) Each operating current shall be defined as being measured in the following condition.

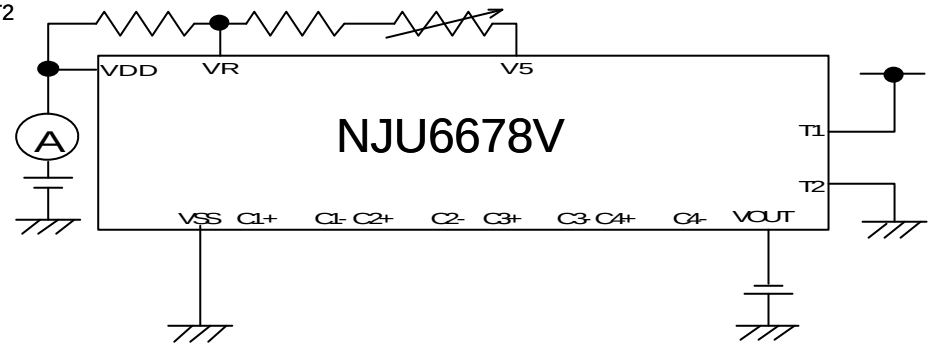
SYMBOL	Status		Operating Condition				External Voltage Supply (Input Terminal)
	T_1	T_2	Internal Oscillator	Voltage Booster	Voltage Adjustment	Voltage Follower	
I_{OUT1}	L	L/H	Validity	Validity	Validity	Validity	Unuse
I_{OUT2}	H	L	Validity	Invalidity	Validity	Validity	Use(V_{OUT})
I_{OUT3}	H	H	Validity	Invalidity	Invalidity	Validity	Use(V_{OUT},V_5)

MEASUREMENT BLOCK DIAGRAM

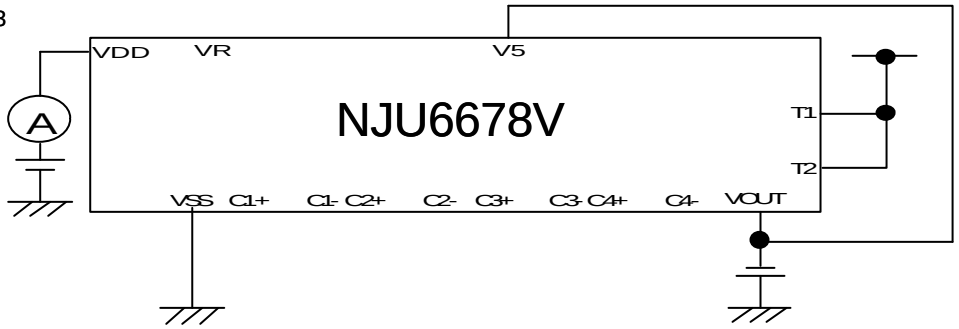
:I_{OUT1}



:I_{OUT2}

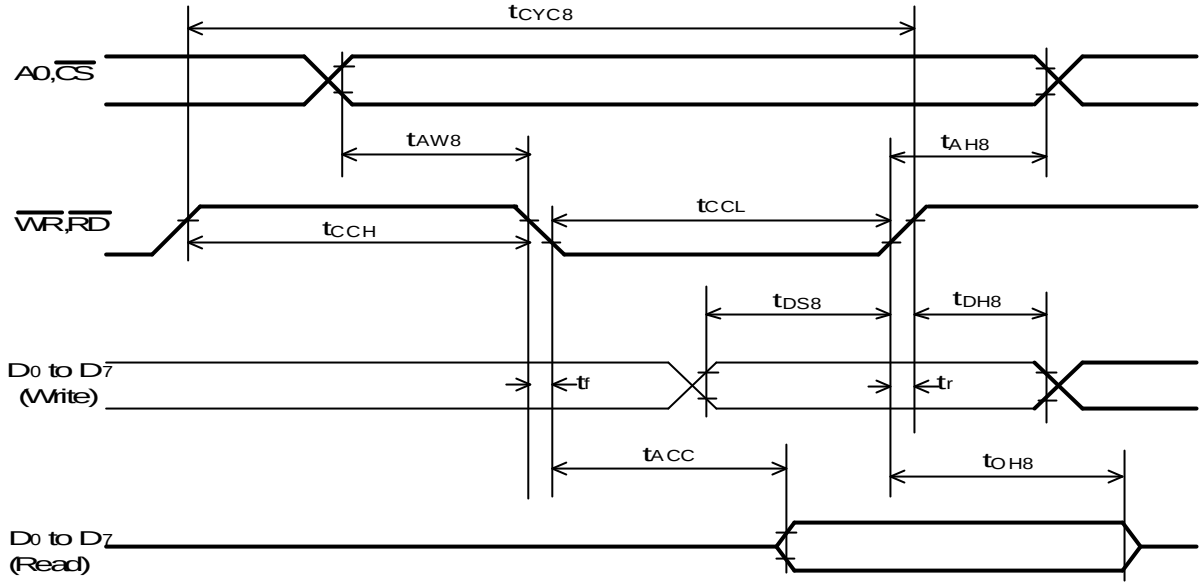


:I_{OUT3}



■ BUS TIMING CHARACTERISTICS

- Read/Write operation sequence (80 Type MPU)

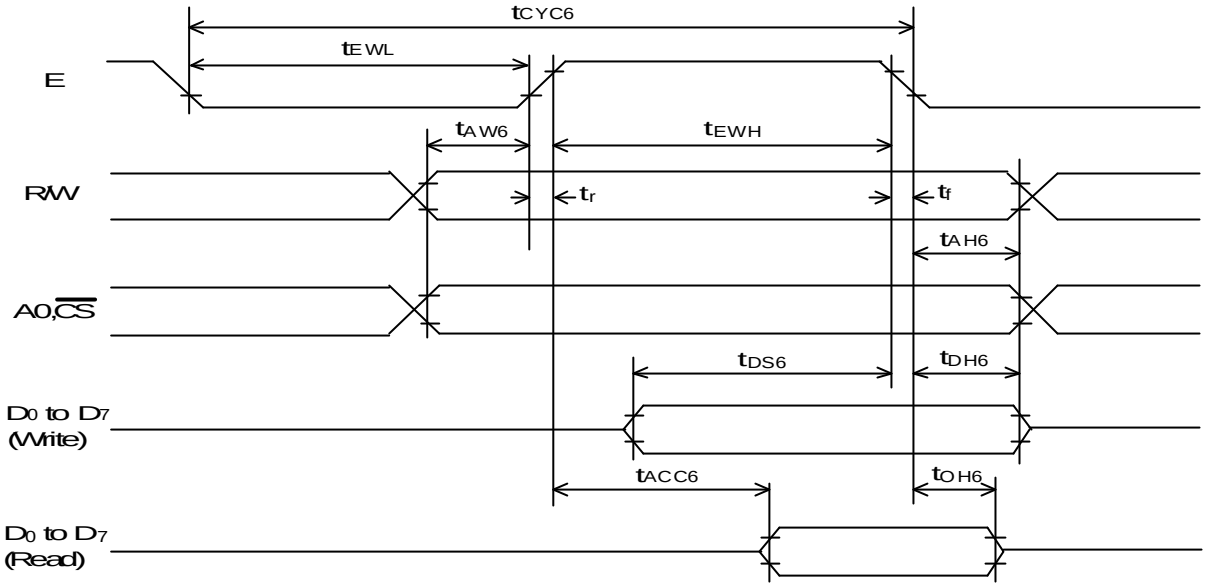


(VDD=2.5V to 3.3V,Ta=-30 to +80°C)

PARAMETER			SYMBOL	MIN.	TYP.	MAX.	CONDITION	UNIT
Address Hold Time		A0,CS Terminals	tAH8	10				ns
Address Set Up Time			tAW8	0				ns
System Cycle Time	WR	WR,RD Terminals	tCYC8 (W)	270	220			ns
	RD		tCYC8 (R)	350				ns
Control Pulse Width	WR,"L"		tCCL(W)	50				ns
	RD,"L"		tCCL(R)	200				ns
	WR,"H"		tCCH(W)	220	160			ns
	RD,"H"		tCCH(R)	150				ns
Data Set Up Time		D0 to D7 Terminals	tDS8	35				ns
Data Hold Time			tDH8	15				ns
RD Access Time			tACC8			120	CL=100pF	ns
Output Disable Time			tOH8	0		50		ns
Rise Time, Fall Time		CS, WR, RD, A0, D0 to D7 Terminals	tr,tf			15		ns

Note 15) All timing based on 20% and 80% of VDD voltage level.

- Read/Write operation sequence (68 Type MPU)



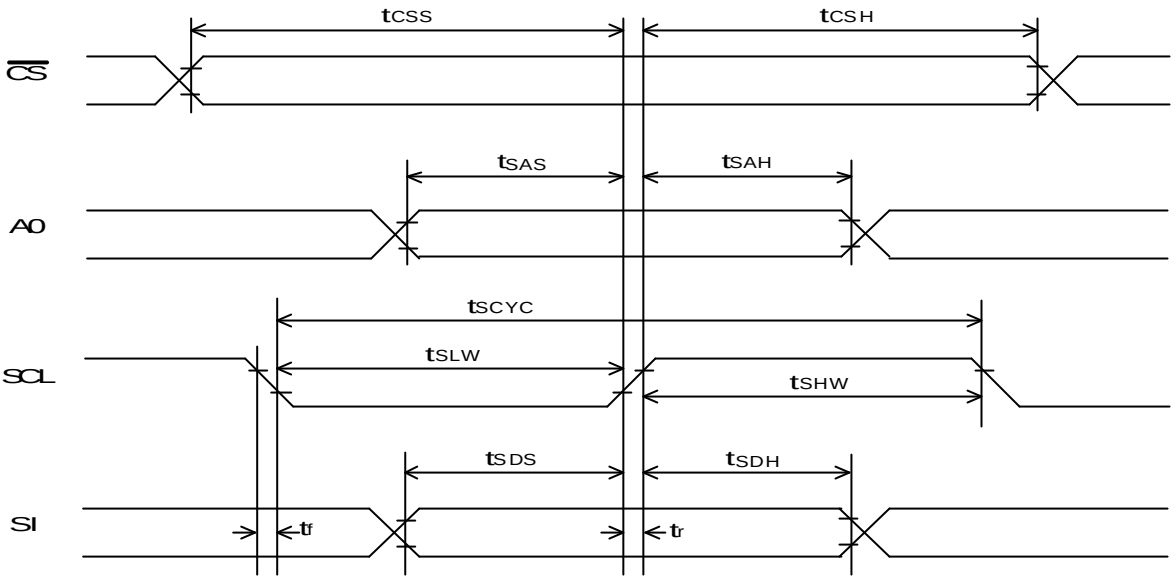
(VDD=2.5V to 3.3V,Ta=-30 to +80°C)

PARAMETER			SYMBOL	MIN.	TYP.	MAX.	CONDITION	UNIT
Address Hold Time		A0,CS,R/W Terminals	tAH6	10				ns
Address Set Up Time			tAW6	0				ns
System Cycle Time(W)			tCYC6(W)	270	220			ns
System Cycle Time(R)			tCYC6(R)	350				ns
Enable Pulse Width	Read"H"	E Terminal	tEWH	200				ns
	Write"H"			50				ns
	Read"L"		tEWL	220	160			ns
	Write"L"			150				ns
Data Set Up Time		D0 to D7 Terminals	tDS6	35				ns
Data Hold Time			tDH6	15				ns
Access Time			tACC6			200	CL=100pF	ns
Output Disable Time			tOH6	0		50		ns
Rise Time, Fall Time		A0, CS, R/W, E, D0 to D7 Terminals	tr,tf			15		ns

Note 16) All timing are based on 20% and 80% of VDD voltage level.

Note 17) tCYC6 shows the cycle of the E signal in active CS.

- Write operation sequence (Serial Interface)

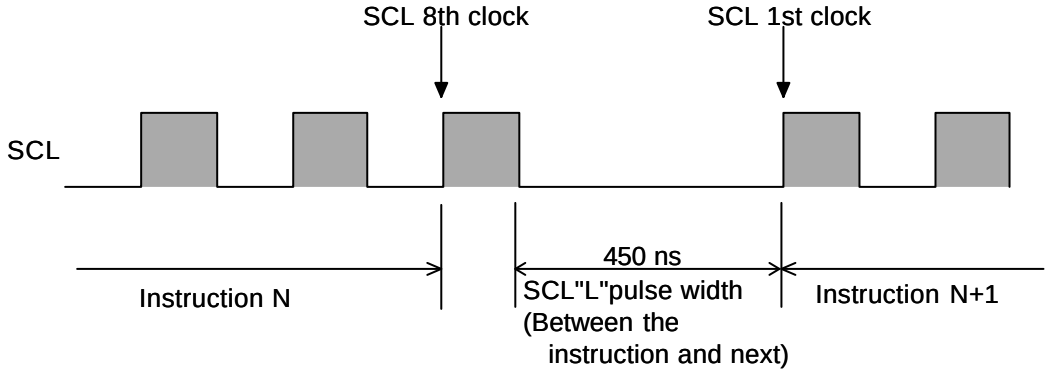


(VDD=2.5V to 3.3V,Ta=-30 to +80°C)

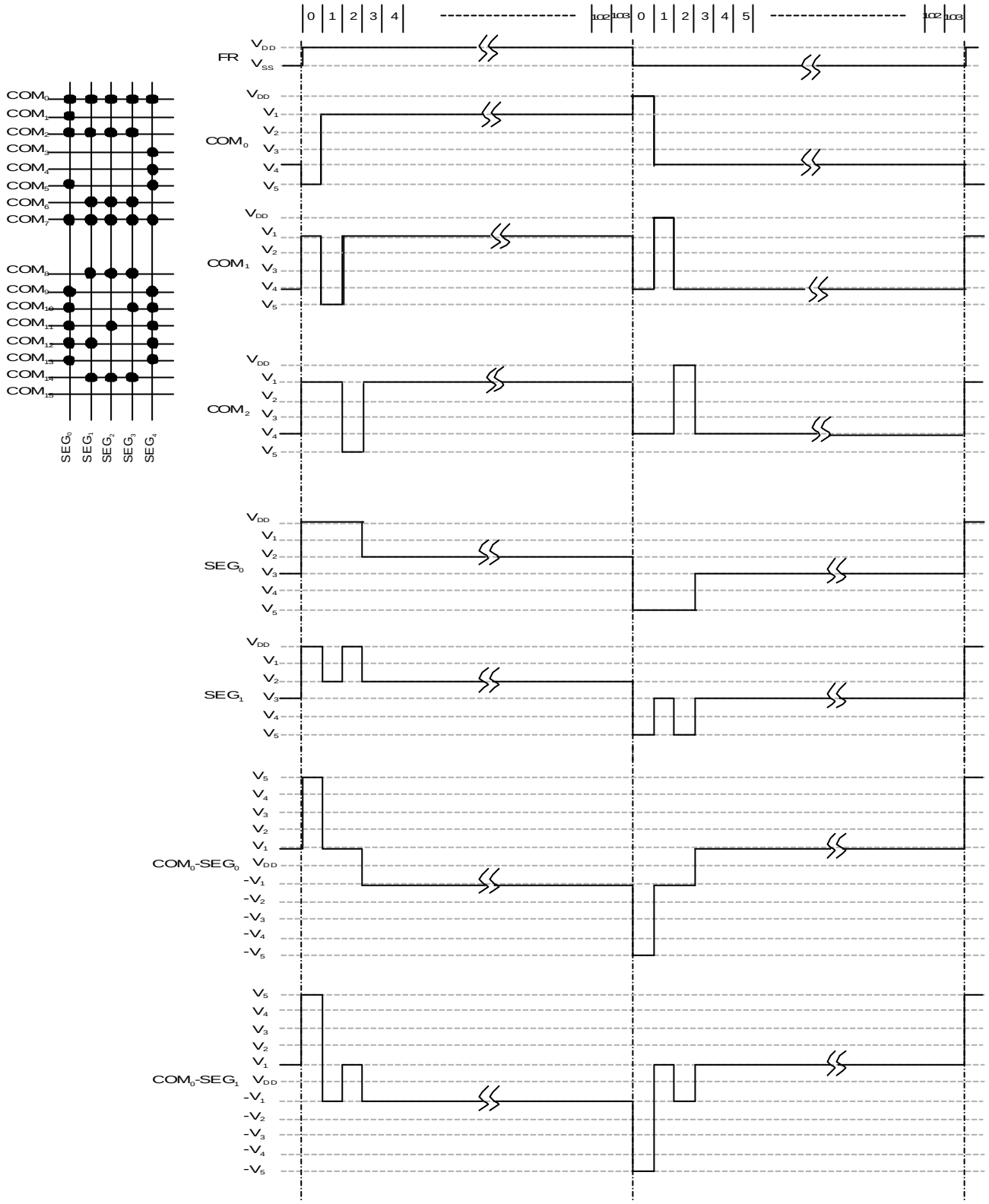
PARAMETER		SYMBOL	MIN.	TYP.	MAX.	CONDITION	UNIT
Serial Clock cycle	SCL Terminal	tSCYC	120				ns
SCL "H" pulse width		tSHW	40				ns
SCL "L" pulse width		tSLW	80				ns
Address Set Up Time	A0 Terminal	tSAS	0				ns
Address Hold Time		tSAH	150				ns
Data Set Up Time	SI Terminal	tSDS	25				ns
Data Hold Time		tSDH	10				ns
$\overline{CS}$-SCL Time	$\overline{CS}$ Terminal	tCSS	10				ns
		tCSH	300				ns
Rise Time, Fall Time	SCL, A0, CS, SI Terminals	tr,tf			15		ns

Note 18) All timing are based on 20% and 80% of VDD voltage level.

Note 19) When inputting an instruction continuously, keep 450nS as the cycle of SCL between the instructions as follows



■ LCD DRIVING WAVEFORM



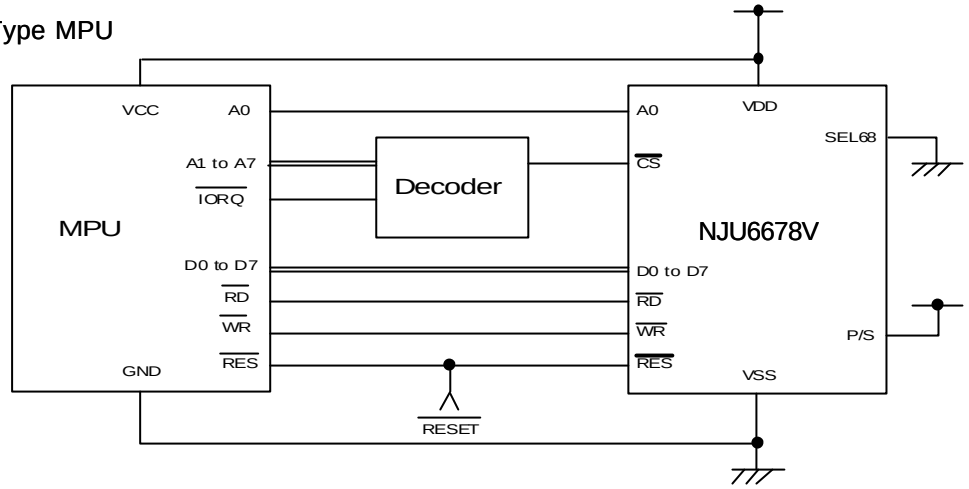
■ APPLICATION CIRCUIT

MPU Interface (examples)

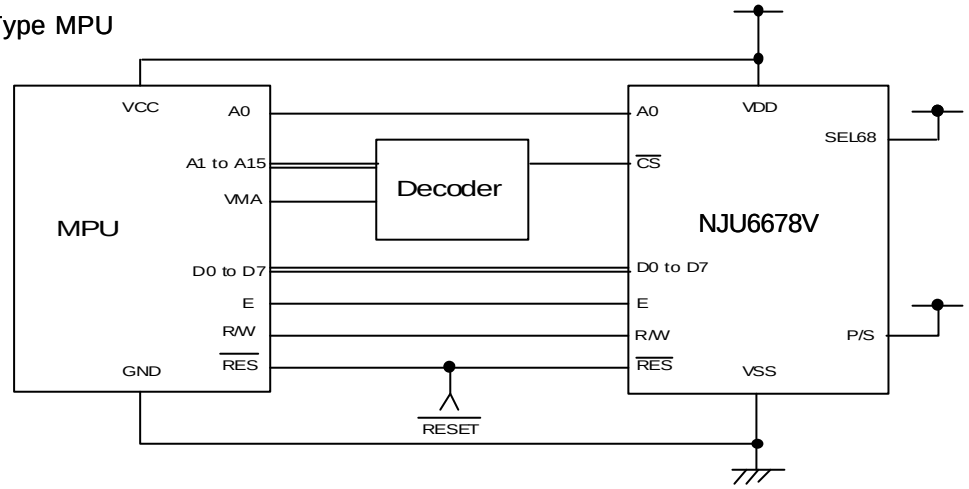
The **NJU6678V** is connectable to 80-type MPU or 68-type. In use of Serial Interface, it is possible to be controlled by the signal line with the more small being.

*:SEL68 terminal shall be connected to V_{DD} or V_{SS}.

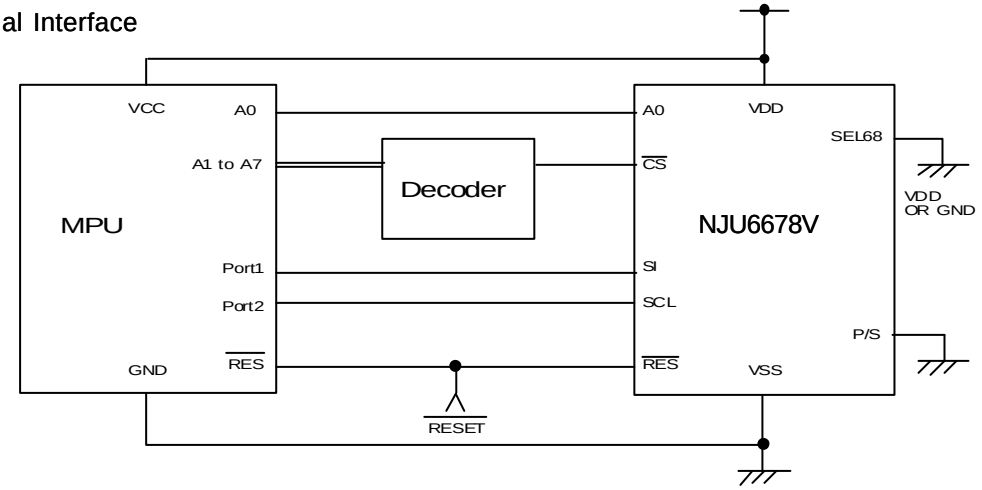
- 80 Type MPU



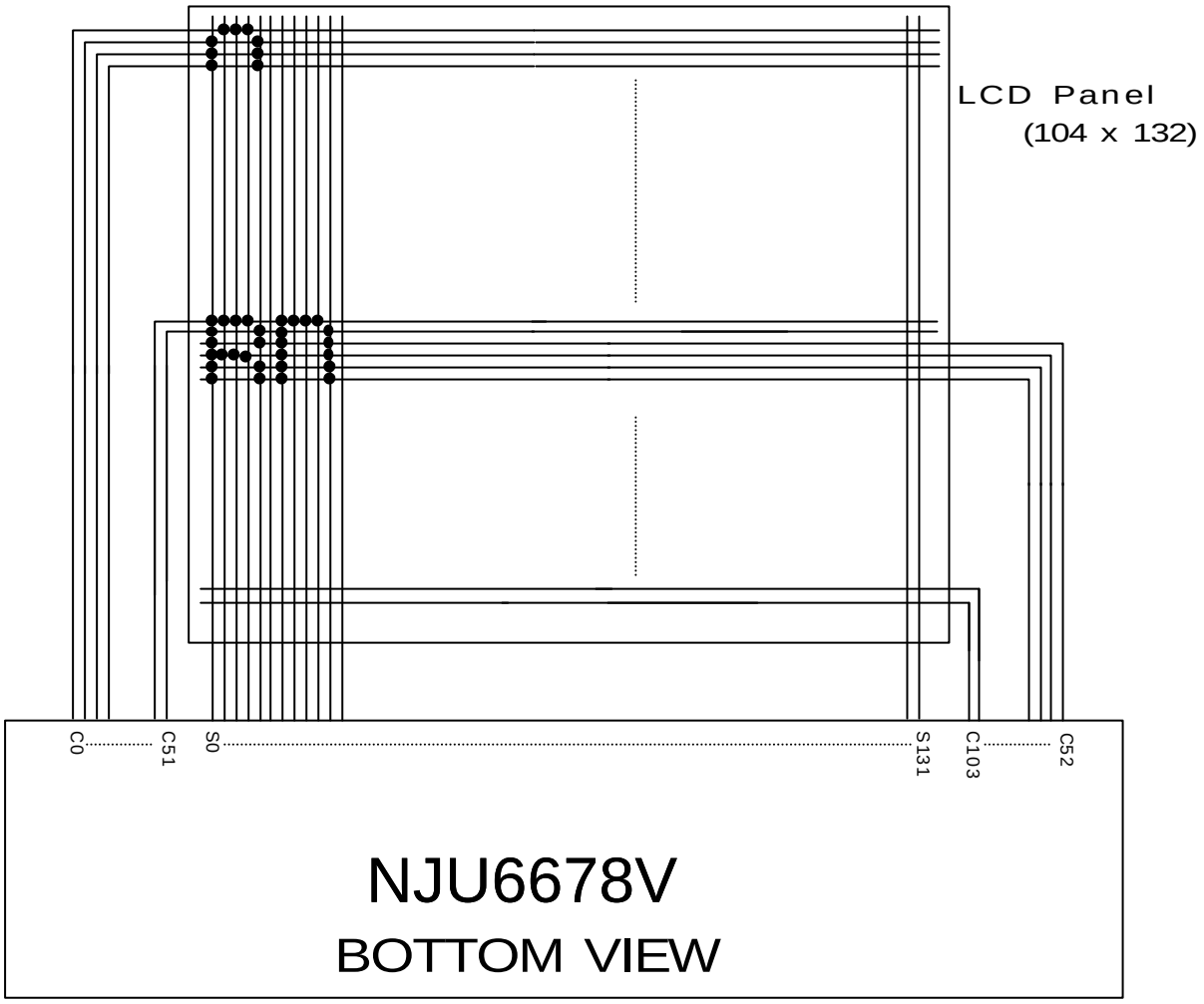
- 68 Type MPU



- Serial Interface



■ LCD Panel Interface Example



■ CAUTION

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