

# Two Channel Distributed System Interface (DSI) Physical Interface Device

The 33790 is a dual channel physical layer interface IC for the Distributed System Interface (DSI) bus. It is designed to meet automotive requirements. It can also be used in non automotive applications. It supports bidirectional communication between slave and master ICs. Some slave devices derive a regulated 5.0 V from the bus, which can be used to power sensors, thereby eliminating the need for additional circuitry and wiring. This device is powered by SMARTMOS technology.

### Features

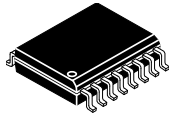
- Two independent DSI compatible buses
- Wave-shaped bus output voltage
- Independent thermal shutdown and current limit
- Return signalling current detection
- Internal logic input pull-ups and pull-downs
- On-board charge pump
- 2.0 kV ESD capability
- Communications rate up to 150 kbps

33790

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DISTRIBUTED SYSTEM INTERFACE (DSI)

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EG SUFFIX (PB-FREE)  
98ASB42567B  
16-PIN SOICW

### Applications

- Simple bus for remote control and sensing
- Automotive, aircraft, marine, industrial controls, and safety systems
- Heating and air-conditioning

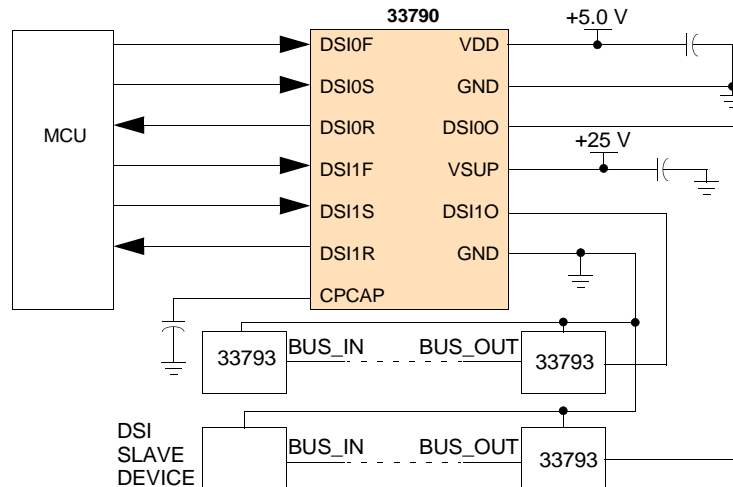


Figure 1. 33790 Simplified Application Diagram

## ORDERABLE PARTS

**Table 1. Orderable Part Variations**

Part Number	Temperature ( $T_A$ )	Package
MC33790HEG/R2	-40 to 85 °C	16 SOICW

## INTERNAL BLOCK DIAGRAM

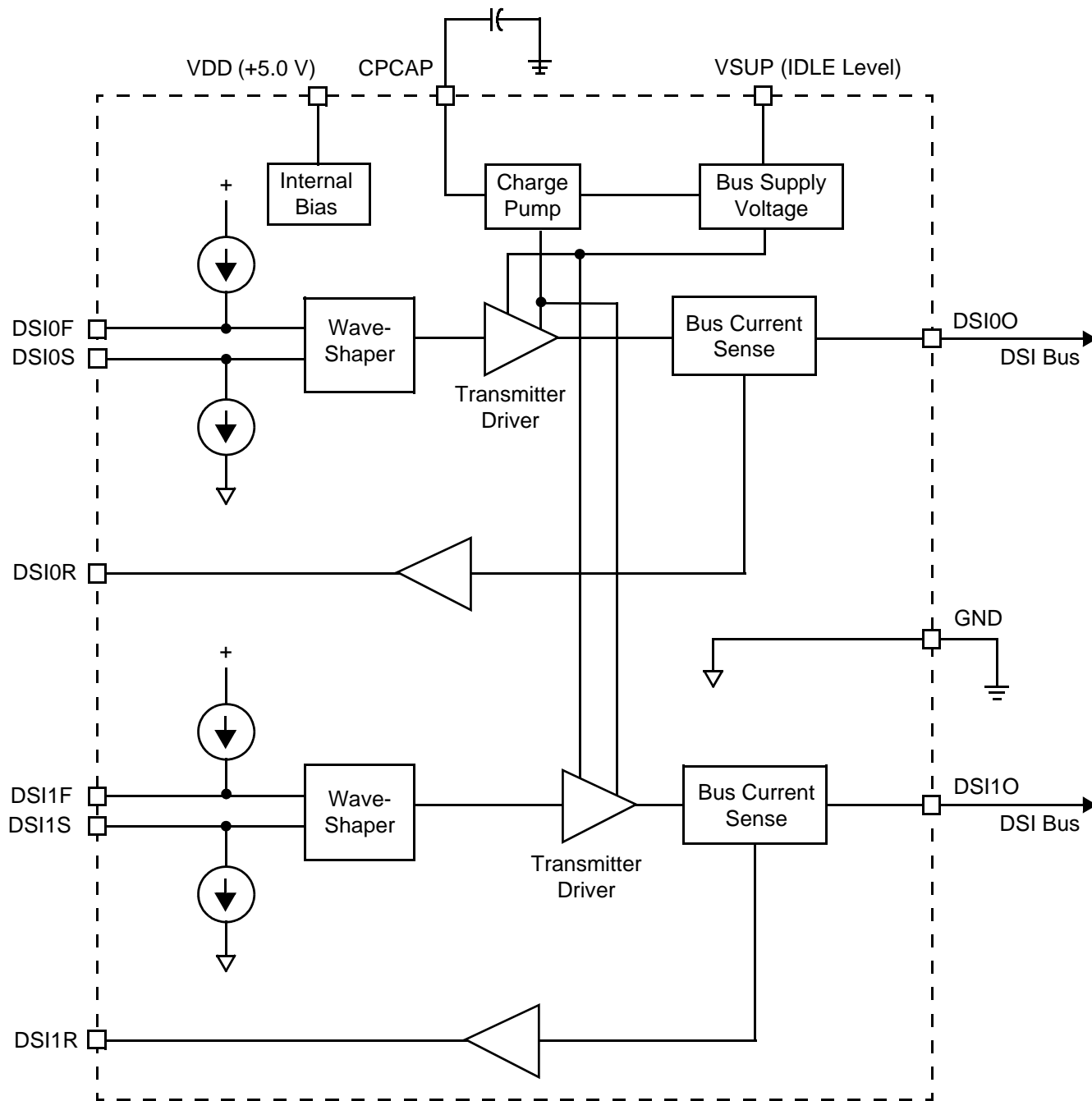
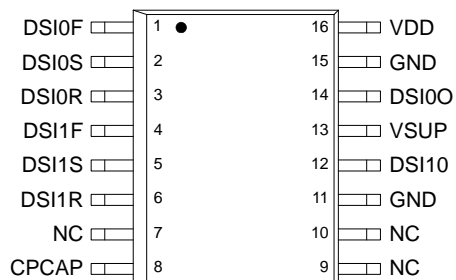


Figure 2. 33790 Simplified Internal Block Diagram

## PIN CONNECTIONS



**Figure 3. 33790 Pin Connections**

**Table 2. 33790 Pin Definitions**

A functional description of each pin can be found in the Functional Pin Description section beginning on [page 9](#).

Pin Number	Pin Name	Definition
1	DSI0F	This logic input controls the frame output for DSI channel 0 in accordance with <a href="#">Table 6</a> , page <a href="#">9</a> .
2	DSI0S	This logic input controls the signalling output for DSI channel 0 in accordance with <a href="#">Table 6</a> , page <a href="#">9</a> .
3	DSI0R	This logic output provides the return data for DSI channel 0 in accordance with <a href="#">Table 6</a> , page <a href="#">9</a> .
4	DSI1F	This logic input controls the frame output for DSI channel 1 in accordance with <a href="#">Table 6</a> , page <a href="#">9</a> .
5	DSI1S	This logic input controls the signalling output for DSI channel 1 in accordance with <a href="#">Table 6</a> , page <a href="#">9</a> .
6	DSI1R	This logic output provides the return data for DSI channel 1 in accordance with <a href="#">Table 6</a> , page <a href="#">9</a> .
7	NC	Unused.
8	CPCAP	Used to store and filter charge pump output.
9	NC	Unused.
10	NC	Unused.
11	GND	Circuit and bus ground return.
12	DSI10	DSI bus 1 input/output.
13	VSUP	Idle level supply input. The voltage supplied to this pin sets the idle level on the DSI bus.
14	DSI00	DSI bus 0 input/output.
15	GND	Circuit and bus ground return.
16	VDD	5.0 V logic supply input.

## ELECTRICAL CHARACTERISTICS

### MAXIMUM RATINGS

**Table 3. Maximum Ratings**

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
<b>ELECTRICAL RATINGS</b>			
Supply Voltage	$V_{SUP}$	-0.5 to 25	V
Continuous			
Load Dump - $t < 300$ ms	$V_{SUP(t)}$	40	
Maximum Voltage on Input/Output Pins	$V_{DD}$ DSIxS, DSIxF (1) DSIxO (1)	-0.3 to 5.5 -0.3 to $V_{DD}+0.3$ -0.3 to $V_{SUP}+0.3$	V
Storage Temperature	$T_{STG}$	-55 to 150	°C
Operating Ambient Temperature	$T_A$	-40 to 85	°C
Operating Junction Temperature	$T_J$	-40 to 150	°C
Peak Package Reflow Temperature During Reflow (2), (3)	$T_{PPRT}$	Note 3	°C
Continuous Current per Pin	$V_{DD}$ DSIxR $V_{SUP}$	0 to 10 -2.5 to 5.0 500	mA
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	45	°C/W
Thermal Shutdown	$T_{SD}$	155 to 190	°C
ESD Voltage (All Pins) (4)			V
Human Body Model	$V_{ESD1}$	±2000	
Machine Model	$V_{ESD2}$	±200	

**Notes**

- $R = 0 \Omega$ .
- Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
- Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to [www.freescale.com](http://www.freescale.com), search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.
- ESD1 performed in accordance with the Human Body Model ( $C_{ZAP}=100$  pF,  $R_{ZAP}=1500 \Omega$ ), ESD2 performed in accordance with the Machine Model ( $C_{ZAP}=200$  pF,  $R_{ZAP}=0 \Omega$ ).

### STATIC ELECTRICAL CHARACTERISTICS

**Table 4. Static Electrical Characteristics**

Characteristics noted under conditions  $4.75\text{ V} \leq V_{DD} \leq 5.25\text{ V}$ ,  $8.0\text{ V} \leq V_{SUP} \leq 25.0\text{ V}$ ,  $-40\text{ }^\circ\text{C} \leq T_J \leq 150\text{ }^\circ\text{C}$ , unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>SUPPLY</b>					
$I_{SUP}$ Supply Current/Channel (Not Including $I_{OUT}$ )					mA
DSIx0 = Idle Voltage, $-100\text{ mA} \leq I_{OUT} \leq 0\text{ mA}$	$I_{SUPI}$	–	1.35	3.25	
DSIx0 = Output High Voltage, $I_{OUT} = 12\text{ mA}$	$I_{SUPH}$	–	5.0	9.00	
$I_{DD}$ Supply Current/Channel	$I_{DD}$	–	0.5	1.0	mA
<b>BUS TRANSMITTER</b>					
$V_{SUP}$ to DSIxO ON Resistance (During Idle)	$R_{DS(ON)}$	–	–	10	$\Omega$
$I_{OUT} = -100\text{ mA}$					
Output High Voltage	$DSIV_{OH}$	4.175	4.5	4.825	V
DSIx0 ( $-15\text{ mA} \leq I_{OUT} \leq 1.0\text{ mA}$ )					
Output Low Voltage	$DSIV_{OL}$	1.325	1.5	1.675	V
DSIx0 ( $-15\text{ mA} \leq I_{OUT} \leq 1.0\text{ mA}$ )					
Output High Side Current Limit <sup>(5)</sup>	$I_{CLH}$	-100	–	-200	mA
Output Low Side Current Limit <sup>(5)</sup>	$I_{CLL}$	110	–	220	mA
Input Leakage	$DSI_{IB}$	-200	–	50	$\mu\text{A}$
DSIxO When DSIxF Is High and DSIxS Is Low ( $0\text{ V} \leq DSIxO \leq \text{Min}$ ( $V_{SUP} = 16.5\text{ V}$ ))					
<b>BUS RECEIVER</b>					
Return Current Threshold	$I_{RH}$	-5.0	-6.0	-7.0	mA
<b>MICROCONTROLLER INTERFACE</b>					
Logic Input Thresholds DSIxS, DSIxF	$V_{IN(TH)}$	1.10	–	2.20	V
Output High Voltage	$V_{OH}$	$0.8 V_{DD}$	–	$V_{DD}$	V
DSIxR Pin = -0.5 mA					
Output Low Voltage	$V_{OL}$	0.0	–	$0.2 V_{DD}$	V
DSIxR Pin = 1.0 mA					
Internal Pull-up for DSIxF	$I_{IL}$	-100	–	-10	$\mu\text{A}$
Internal Pull-down for DSIxS	$I_{IH}$	10	–	100	$\mu\text{A}$

Notes

- After 10  $\mu\text{s}$  settling time (assured by design).

## DYNAMIC ELECTRICAL CHARACTERISTICS

**Table 5. Dynamic Electrical Characteristics**

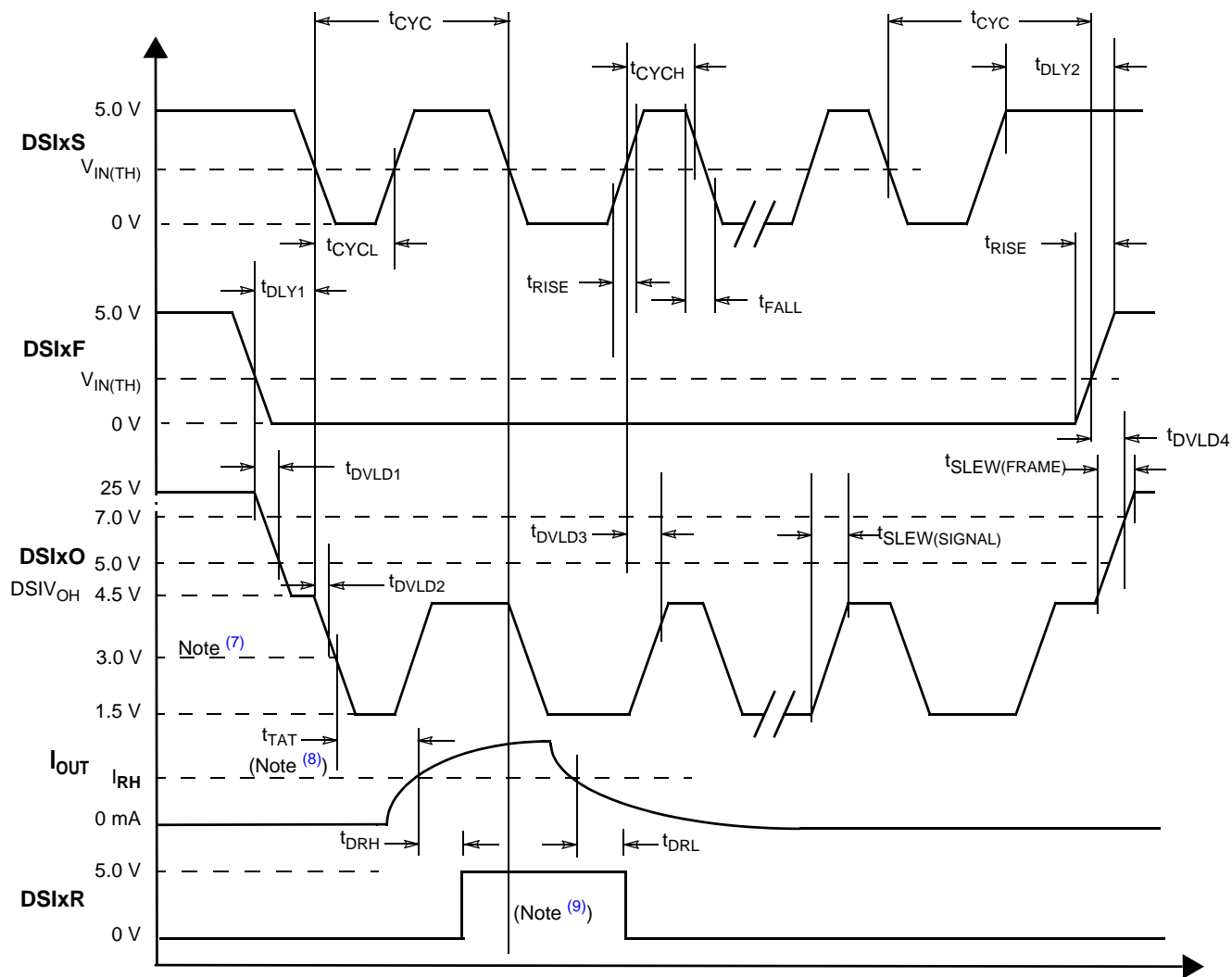
Characteristics noted under conditions  $4.75\text{ V} \leq V_{DD} \leq 5.25\text{ V}$ ,  $8.0\text{ V} \leq V_{SUP} \leq 25.0\text{ V}$ ,  $-40\text{ }^\circ\text{C} \leq T_J \leq 150\text{ }^\circ\text{C}$ , unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>MICROCONTROLLER INTERFACE</b>					
Microcontroller Signal Cycle Time	$t_{CYC}$	6.6	–	1000	$\mu\text{s}$
Microcontroller Signal Low Time	$t_{CYCL}$	2.0	–	667	$\mu\text{s}$
Microcontroller Signal High Time	$t_{CYCH}$	2.0	–	667	$\mu\text{s}$
Microcontroller Signal Duty Cycle for Logic Zero	$DC_{LO}$	30	33	36	%
Microcontroller Signal Duty Cycle for Logic One	$DC_{HI}$	60.0	66.7	72.0	%
Microcontroller Signal Slew Time <sup>(6)</sup>	$t_{SLEW}$	–	–	500	ns
Frame Start to Signal Delay Time	$t_{DLY1}$	$t_{cyc}-0.1$	$t_{cyc}$	$t_{cyc}+0.1$	$\mu\text{s}$
Signal End to Frame End Delay Time	$t_{DLY2}$	1.0	–	–	$\mu\text{s}$
Rise Time <sup>(6)</sup>	$t_{RISE}$	0	–	100	ns
Fall Time <sup>(6)</sup>	$t_{FALL}$	0	–	100	ns
<b>BUS TRANSMITTER</b>					
Idle to Frame and Frame to Idle Slew Rate $C \leq 5.0\text{ nF}$	$t_{SLEW(FRAME)}$	3.0	6.0	10.0	$\text{V}/\mu\text{s}$
Signal High to Low and Signal Low to High Slew Rate $C \leq 5.0\text{ nF}$	$t_{SLEW(SIGNAL)}$	3.0	4.5	8.0	$\text{V}/\mu\text{s}$
Data Valid ( $V_{SUPx} = 25\text{ V}$ , $C_L \leq 5.0\text{ nF}$ )					$\mu\text{s}$
DSIxF, $V_{IN(TH)}$ to DSIXO = 5.3 V	$t_{DVLD1}$	2.44	–	6.56	
DSIXS, $V_{IN(TH)}$ to DSIXO = 2.6 V	$t_{DVLD2}$	0.25	–	1.3	
DSIXS, $V_{IN(TH)}$ to DSIXO = 3.4 V	$t_{DVLD3}$	0.25	–	1.3	
DSIXF, $V_{IN(TH)}$ to DSIXO = 7.0 V	$t_{DVLD4}$	0.25	–	1.3	
<b>BUS RECEIVER</b>					
Receiver Delay Time					ns
$t_{DRH}$ : $I = I_{RH}$ to DSIXR = 2.5 V	$t_{DRH}$	–	400	750	
$t_{DRL}$ : $I = I_{RH}$ to DSIXR = 2.5 V	$t_{DRL}$	–	400	750	

**Notes**

6. Slew times and rise and fall times between 10% and 90% of output high and low levels.

**TIMING CHARACTERISTICS**



**Figure 4. Timing Characteristics**

Notes

7. Typical BUSIN/BUSOUT logic thresholds ( $V_{THL}$ ) from MC33793 datasheet.
8.  $t_{TAT}$  (Turnaround Time) is dependent upon wire length, bus loads, and slave response characteristics.
9. DS1xR stable on falling edge of DS1xS or rising edge of DS1xF.



## FUNCTIONAL DESCRIPTION

### INTRODUCTION

The 33790 is designed to provide the interface between logic and the DSI bus. It accepts signals with a typical 0 V to 5.0 V logic level to control the state of the bus output (Idle Level, Logic High Level, Logic Low Level, and High Impedance). It detects the current drawn from the bus output during signaling and outputs a 0 V to 5.0 V logic level corresponding

to the bus current being above (Logic [1] out) the bus return logic [1] current or below (Logic [0] out). The 33790 contains current limiting of the bus outputs as required by the DSI Bus specification and thermal shutdown to protect itself from damage. Two independent DSI bus outputs are provided by the IC.

### FUNCTIONAL TERMINAL DESCRIPTION

#### Bus Driver and Receiver

The Wave-Shaper converts the 0 to 5.0 V logic inputs from DSIXF (frame) and DSIXS (signal) to a wave-shaped signal on the DSIXO output, as shown in the timing diagrams in [Figure 2](#), page 3, and the truth table in [Table 6](#). The Bus Current Sense detects the current being drawn by the device(s) on the bus during signalling (DSIXF=0). If the current is above a set level, DSIXR will be high; otherwise, it is low. Due to the variations in the turnaround time ( $t_{TAT}$ ) from slave devices and bus delays, DSIXR should be sampled on the falling edge of DSIXS and on the rising edge of DSIXF (for the last return bit).

**Table 6. DSI Bus Truth Table**

DSIXF	DSIXS	TX <sub>LIM</sub>	DSIXR	DSIXO
0	0	0	Not Defined	Low (1.5 V)
0	1	0	Not Defined	High (4.5 V)
0	↓	0	Return Data	Unchanged
↑	X	0	Return Data	Unchanged
1	0	0	0	High Impedance
1	1	0	0	Idle $\geq V_{SUP} - 0.5$ V
X	X	1	1	High Impedance

The current for the idle state is from the supply connected to  $V_{SUP}$  and this supply should not be current limited below

250 mA per channel. During idle state, the voltage on the DSI bus will be very close to the  $V_{SUP}$  voltage.

Internal thermal shutdown circuitry and current limit individually protect the DSIXO outputs from shorts to battery and ground.

Typically, the thermal shutdown occurs between 160 °C and 170 °C. If the junction temperature rises above this temperature, the internal TX<sub>LIM</sub> bit is asserted, and the output drivers for DSIXO are disabled by the thermal shutdown circuitry. The output drivers remain off until the junction temperature decreases below approximately 155 °C, at which time the thermal shutdown circuitry turns off and the outputs are re-enabled. Each DSIXO output has a unique thermal sense and shutdown circuit, so a short on one channel does not affect the other channel.

#### Charge Pump

The charge pump uses on-board capacitors to step the input voltage up to the voltage needed to drive the on-board transmitter FETs. A filter/storage capacitor is connected to CPCAP to hold the stepped-up voltage.

#### Input Pull-ups and Pull-downs

Internal current pull-ups are used on the DSIXF pins and pulldowns on the DSIXS pins. If these pins are left unconnected, their associated DSI bus will go to the unused (high-impedance) state.

## TYPICAL APPLICATIONS

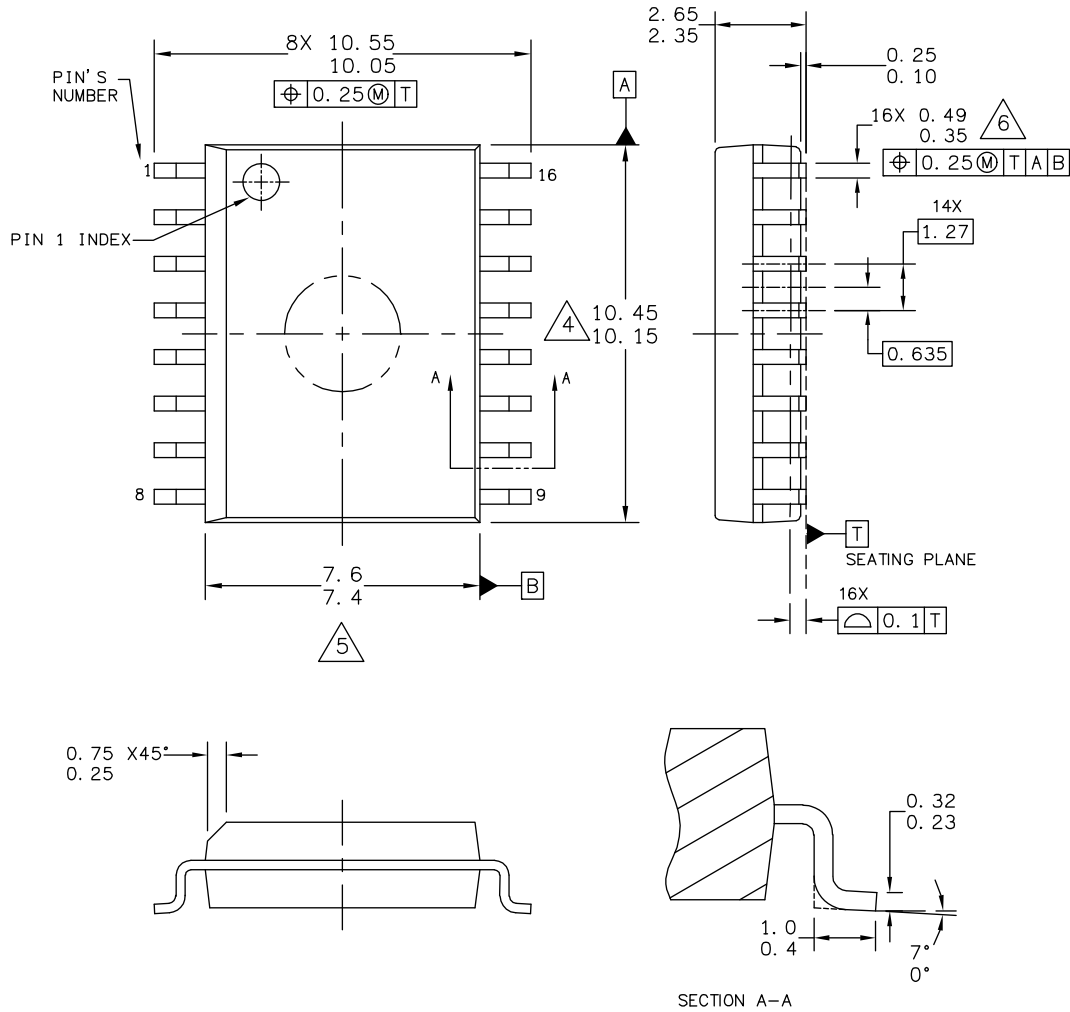
The 33790 is intended for use in a DSI system. This device supplies the interface between standard logic levels and the voltage and current required for the DSI bus. Two independent DSI busses are supported by this part. The 33790 does not form the timing for the DSI bus. This is done by logic embedded in a microcontroller which interfaces to the 33790 through the MCU's 5 V I/O pins.

A capacitor attached to CPCAP serves as a charge reservoir for the gate drive charge pump. This circuit creates a voltage that is higher than the source of the N-channel output transistor. This allows turning on of the transistor enough to prevent any significant voltage drop across it. The rest of charge pump electronics are completely self-contained on the IC.

# PACKAGING

## PACKAGE DIMENSIONS

For the most current package revision, visit [www.freescale.com](http://www.freescale.com) and perform a keyword search using the "98A" listed below.



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TITLE: 16LD SOIC W/B, 1.27 PITCH CASE-OUTLINE	DOCUMENT NO: 98ASB42567B	REV: F	
	CASE NUMBER: 751G-04	02 JUN 2005	
	STANDARD: JEDEC MS-013AA		

**EG SUFFIX (PB-FREE)**  
**98ASB42567B**  
**16-PIN SOICW**

## REVISION HISTORY

Revision	Date	Description of Changes
7.0	5/2006	<ul style="list-style-type: none"> <li>• Implemented Revision History page</li> <li>• Converted to Freescale format</li> </ul>
8.0	11/2006	<ul style="list-style-type: none"> <li>• Updated data sheet format</li> <li>• Removed Peak Package Reflow Temperature During Reflow (solder reflow) parameter from <a href="#">Maximum Ratings on page 5</a>. Added note with instructions to obtain this information from <a href="http://www.freescale.com">www.freescale.com</a>.</li> </ul>
9.0	11/2006	<ul style="list-style-type: none"> <li>• Minor correction changes to Figure 1 and ordering information</li> </ul>
10.0	12/2006	<ul style="list-style-type: none"> <li>• Restated note <a href="#">Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C</a>. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to <a href="http://www.freescale.com">www.freescale.com</a>, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics. on page 5</li> </ul>
11.0	3/2008	<ul style="list-style-type: none"> <li>• Removed watermark from page 1.</li> </ul>
12.0	12/2011	<ul style="list-style-type: none"> <li>• Removed part numbers MCZ33790EG/R2, MC33790DW/R2 and added part number MC33790HEG/R2.</li> <li>• Deleted references to MC68HC55.</li> <li>• Updated Freescale form and style.</li> </ul>
13.0	2/2014	<ul style="list-style-type: none"> <li>• No technical changes. Revised back page. Updated document properties. Added SMARTMOS sentence to last paragraph on page 1.</li> </ul>

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