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November 2013

# FDB035N10A

# N-Channel PowerTrench<sup>®</sup> MOSFET 100 V, 214 A, 3.5 m $\Omega$

#### **Features**

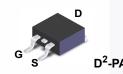
- $R_{DS(on)}$  = 3.0  $m\Omega$  ( Typ.) @  $V_{GS}$  = 10 V,  $I_D$  = 75 A
- · Fast Switching Speed
- Low Gate Charge, Q<sub>G</sub> = 89 nC (Typ.)
- High Performance Trench Technology for Extremely Low  $R_{DS(on)}$
- · High Power and Current Handling Capability
- · RoHS Compliant

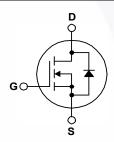
#### Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advance PowerTrench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

### **Applications**

- · Synchronous Rectification for ATX / Server / Telecom PSU
- · Battery Protection Circuit
- · Motor drives and Uninterruptible Power Supplies
- · Micro Solar Inverter





#### MOSFET Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted.

Symbol		Parameter		FDB035N10A	Unit
V <sub>DSS</sub>	Drain to Source Voltage			100	V
V <sub>GSS</sub>	Gate to Source Voltage	Source Voltage			V
		- Continuous (T <sub>C</sub> = 25°C, Silicon I	_imited)	214*	
I <sub>D</sub>	Drain Current	- Continuous (T <sub>C</sub> = 100°C, Silicon	Limited)	151*	Α
		e Limited)	120		
I <sub>DM</sub>	Drain Current	- Pulsed	(Note 1)	856	Α
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)			658	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	6.0	V/ns
D	Davies Dissination	(T <sub>C</sub> = 25°C)		333	W
$P_{D}$	Power Dissipation	- Derate Above 25°C		2.22	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range			-55 to +175	οС
T <sub>L</sub>	Maximum Lead Temperatur	e for Soldering, 1/8" from Case for 5 Sec	onds	300	οС

<sup>\*</sup>Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 120A.

#### Thermal Characteristics

Symbol	Parameter	FDB035N10A	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.45	
D	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	62.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (1 in <sup>2</sup> Pad of 2-oz Copper), Max.	40	

# **Package Marking and Ordering Information**

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDB035N10A	FDB035N10A	D <sup>2</sup> -PAK	Tape and Reel	330 mm	24 mm	800 units

# **Electrical Characteristics** $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	cteristics					
$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V, T_C = 25^{\circ}C$	100	-	-	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 μA, Referenced to 25°C	-	0.07	-	V/°C
1	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V	-	-	1	
IDSS	Zeio Gate voltage Dialii Cuilent	$V_{DS} = 80 \text{ V}, T_{C} = 150^{\circ}\text{C}$	-	-	500	μΑ
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V	-	-	±100	nA

#### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu\text{A}$	2.0	-	4.0	V
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 75 A	-	3.0	3.5	mΩ
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 75 A	-	167	-	S

#### **Dynamic Characteristics**

-							
C <sub>iss</sub>	Input Capacitance	V 05.V.V 0.V		-	5485	7295	pF
Coss	Output Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1 MHz		-	2430	3230	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 1 1/11 12		-\	210	-	pF
Q <sub>g(tot)</sub>	Total Gate Charge at 10V	V <sub>DS</sub> = 80 V, I <sub>D</sub> = 75 A,		- \	89	116	nC
$Q_{gs}$	Gate to Source Gate Charge	V <sub>GS</sub> = 10 V		- \	24	-	nC
Q <sub>gs2</sub>	Gate Charge Threshold to Plateau			-	8	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		(Note 4)	-	25	-	nC

#### **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 50 V, I <sub>D</sub> = 75 A,		-	22	54	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{GS} = 10 \text{ V}, R_{G} = 4.7 \Omega$		- /	54	118	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			- /	37	84	ns
t <sub>f</sub>	Turn-Off Fall Time		(Note 4)	-/	11	32	ns
ESR	Equivalent Series Resistance (G-S)	f = 1 MHz		-	1.2	-	Ω

#### **Drain-Source Diode Characteristics**

I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current		-	-	214*	Α
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current		-	-	856	Α
$V_{SD}$	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 75 A	-	-	1.25	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 75 A, V <sub>DD</sub> = 80 V,	-	72	-	ns
$Q_{rr}$	Reverse Recovery Charge	$dI_F/dt = 100 A/\mu s$	-	129	-	nC

#### Notes:

- 1. Repetitive rating: pulse-width limited by maximum junction temperature.
- 2. Starting  $T_J$  = 25°C, L = 1 mH,  $I_{\mbox{\scriptsize AS}}$  = 36.3 A.
- 3. I  $_{SD} \leq$  75 A, di/dt  $\leq$  200 A/µs, V  $_{DD} \leq$  BV  $_{DSS}$ , starting T  $_{J}$  = 25°C.
- 4. Essentially independent of operating temperature typical characteristics.

# **Typical Performance Characteristics**

Figure 1. On-Region Characteristics

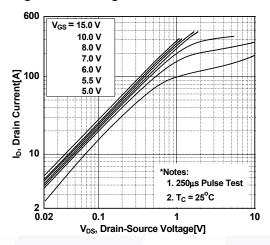


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

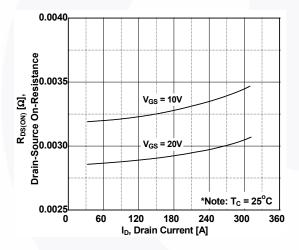


Figure 5. Capacitance Characteristics

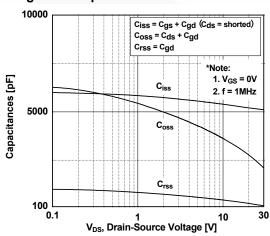


Figure 2. Transfer Characteristics

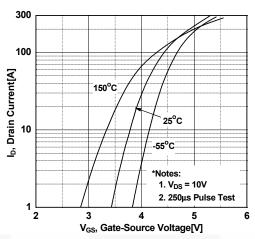


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

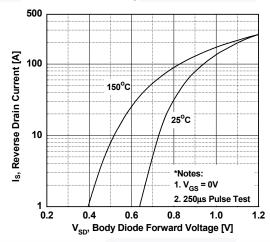
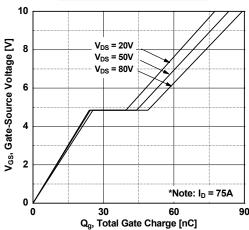


Figure 6. Gate Charge Characteristics



# **Typical Performance Characteristics**

Figure 7. Breakdown Voltage Variation vs. Temperature

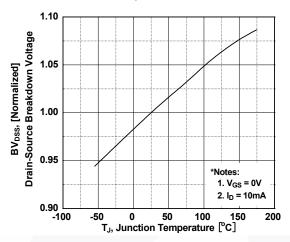


Figure 8. On-Resistance Variation vs. Temperature

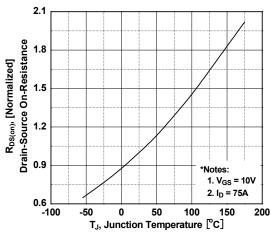


Figure 9. Maximum Safe Operating Area

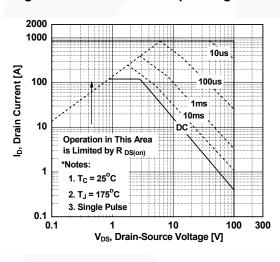


Figure 10. Maximum Drain Current vs. Case Temperature

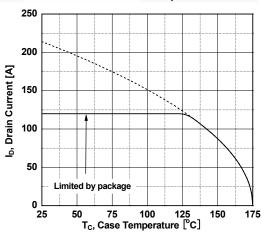
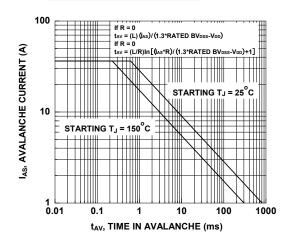
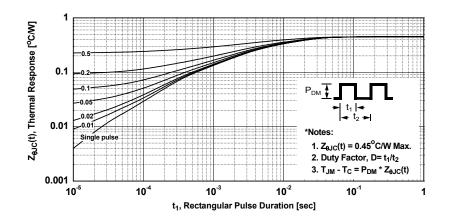


Figure 11. Unclamped Inductive Switching Capability



# **Typical Performance Characteristics**

**Figure 12. Transient Thermal Response Curve** 



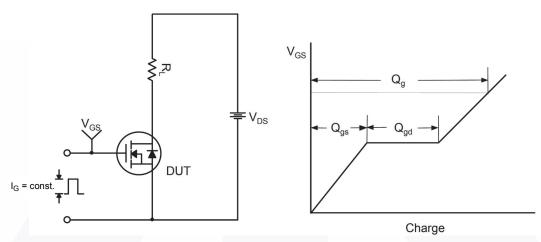


Figure 13. Gate Charge Test Circuit & Waveform

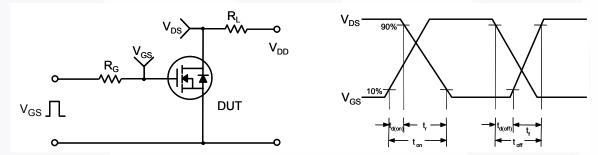


Figure 14. Resistive Switching Test Circuit & Waveforms

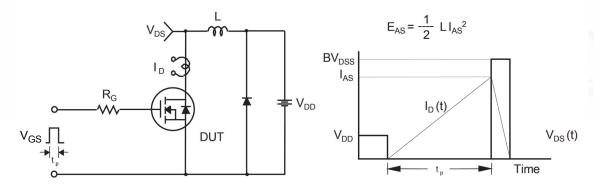


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

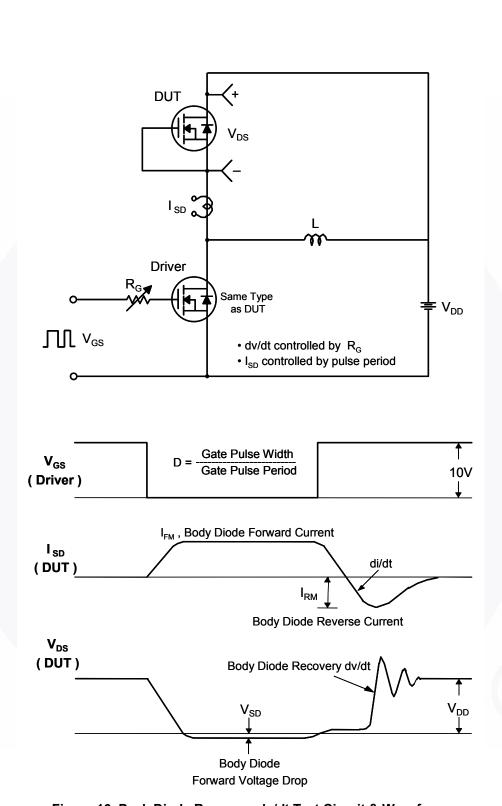


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

#### **Mechanical Dimensions**

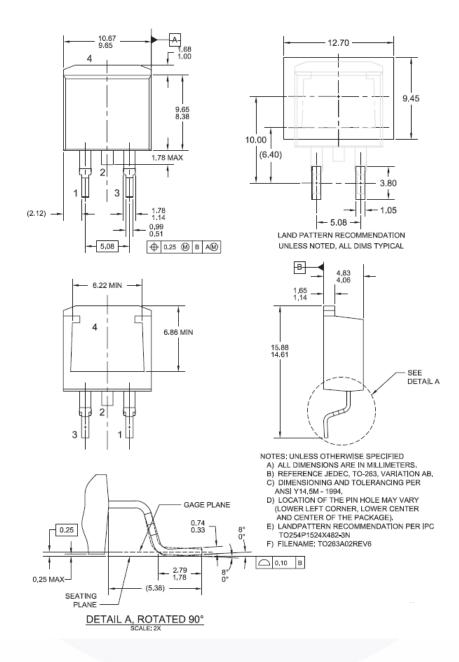


Figure 17. TO263 (D<sup>2</sup>PAK), Molded, 2-Lead, Surface Mount

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