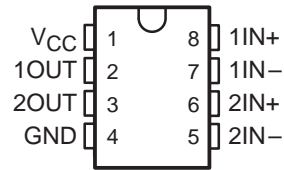


# uA9637AC DUAL DIFFERENTIAL LINE RECEIVER

SLLS111B – SEPTEMBER 1980 – REVISED MAY 1995

- Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-422-B and EIA/TIA-423-B and ITU Recommendations V.10 and V.11
- Operates From Single 5-V Power Supply
- Wide Common-Mode Voltage Range
- High Input Impedance
- TTL-Compatible Outputs
- High-Speed Schottky Circuitry
- 8-Pin Dual-in-Line and Small-Outline Packages
- Designed to Be Interchangeable With National DS9637A

uA9637AC . . . D OR P PACKAGE  
(TOP VIEW)

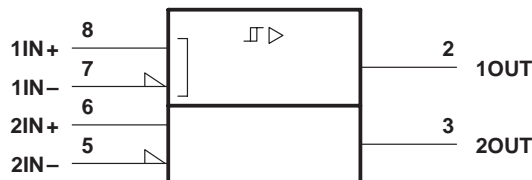


## description

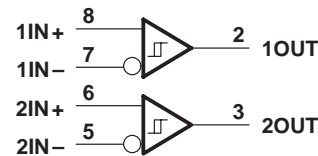
The uA9637AC is a dual differential line receiver designed to meet ANSI Standards EIA/TIA-422-B and EIA/TIA-423-B and ITU Recommendations V.10 and V.11. The line receiver utilizes Schottky circuitry and has TTL-compatible outputs. The inputs are compatible with either a single-ended or a differential-line system. This device operates from a single 5-V power supply and is supplied in an 8-pin dual-in-line package or small-outline package.

The uA9637AC is characterized for operation from 0°C to 70°C.

## logic symbol†



## logic diagram



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

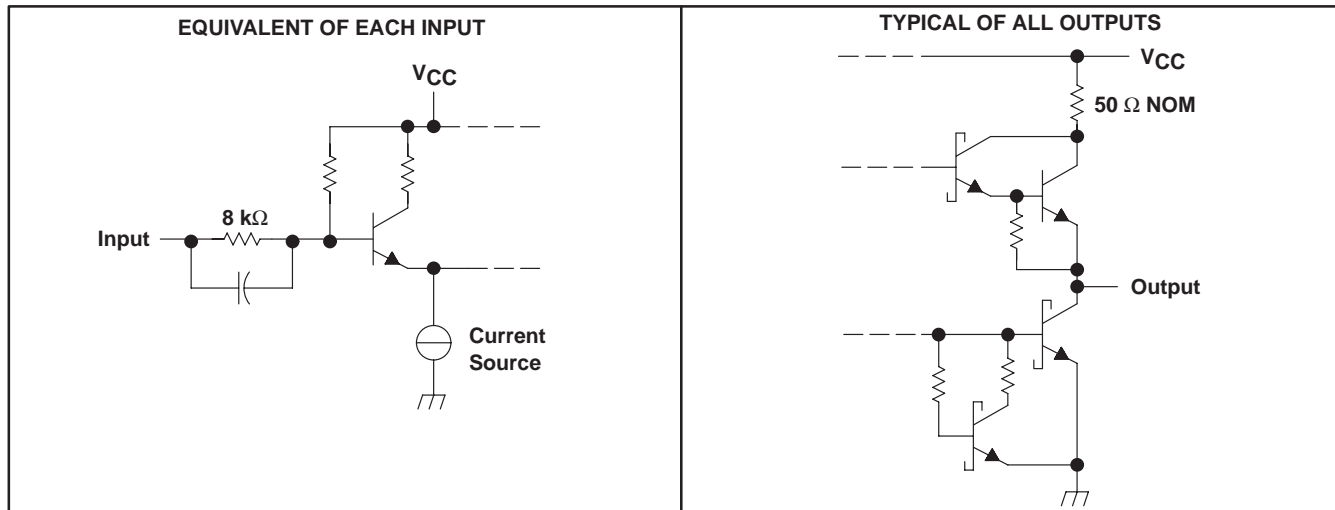
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# uA9637AC DUAL DIFFERENTIAL LINE RECEIVER

SLLS111B – SEPTEMBER 1980 – REVISED MAY 1995

## schematics of inputs and outputs



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ (see Note 1)	.....	-0.5 V to 7 V
Input voltage, $V_I$	.....	$\pm 15$ V
Differential input voltage, $V_{ID}$ (see Note 2)	.....	$\pm 15$ V
Output voltage range, $V_O$ (see Note 1)	.....	-0.5 V to 5.5 V
Low-level output current, $I_{OL}$	.....	50 mA
Continuous total dissipation	.....	See Dissipation Rating Table
Operating free-air temperature range, $T_A$	.....	0°C to 70°C
Storage temperature range, $T_{stg}$	.....	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	.....	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.  
 2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$	OPERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$	$T_A = 125^\circ\text{C}$
	POWER RATING		POWER RATING	POWER RATING
D	725 mW	5.8 mW/°C	464 mW	—
P	1000 mW	8.0 mW/°C	640 mW	—

**recommended operating conditions**

	MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$	4.75	5	5.25	V
Common-mode input voltage, $V_{IC}$			±7	V
Operating free-air temperature, $T_A$	0		70	°C

**electrical characteristics over recommended ranges of supply voltage, common-mode input voltage, and operating free-air temperature (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT	
$V_{IT+}$	Positive-going input threshold voltage	See Note 3			0.2 0.4	V	
$V_{IT-}$	Negative-going input threshold voltage	See Note 3	-0.2		-0.4‡	V	
$V_{hys}$	Hysteresis voltage ( $V_{IT+} - V_{IT-}$ )			70		mV	
$V_{OH}$	High-level output voltage	$V_{ID} = 0.2$ V, $I_O = -1$ mA	2.5	3.5		V	
$V_{OL}$	Low-level output voltage	$V_{ID} = -0.2$ V, $I_O = 20$ mA		0.35	0.5	V	
$I_I$	Input current	$V_{CC} = 0$ to 5.5 V, See Note 4		$V_I = 10$ V $V_I = -10$ V	1.1 -1.6	3.25 -3.25	mA
$I_{OS}$	Short-circuit output current§	$V_O = 0$ , $V_{ID} = 0.2$ V	-40	-75	-100	mA	
$I_{CC}$	Supply current	$V_{ID} = -0.5$ V, No load		35	50	mA	

† All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.

§ Only one output should be shorted at a time, and duration of the short circuit should not exceed one second.

NOTES: 3. The expanded threshold parameter is tested with a 500- $\Omega$  resistor in series with each input.

4. The input not under test is grounded.

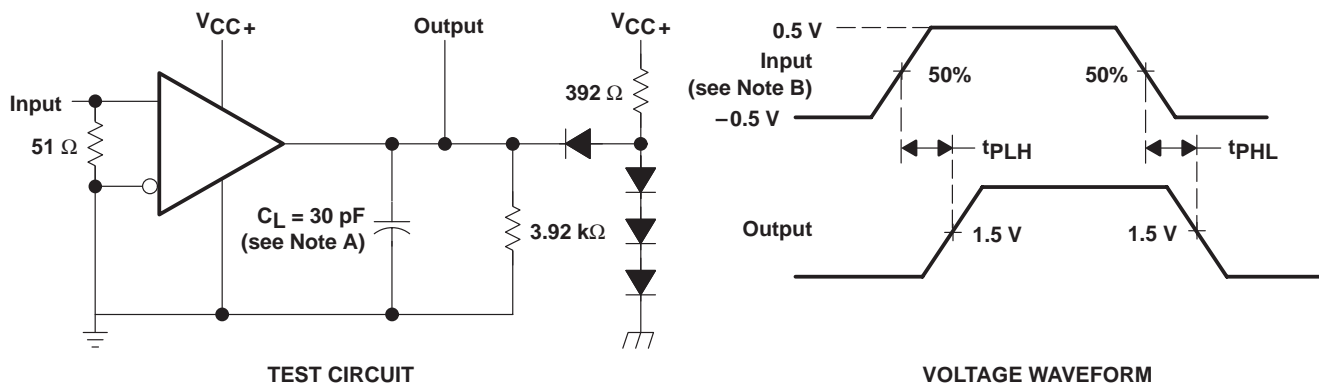
**switching characteristics,  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Propagation delay time, low- to high-level output	$C_L = 30$ pF, See Figure 1		15	25	ns
$t_{PHL}$	Propagation delay time, high- to low-level output			13	25	ns

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## PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The input pulse is supplied by a generator having the following characteristics:  $t_r \leq 5$  ns,  $t_f \leq 5$  ns,  $PRR \leq 5$  MHz, duty cycle = 50%.

Figure 1. Test Circuit and Voltage Waveform

## TYPICAL CHARACTERISTICS

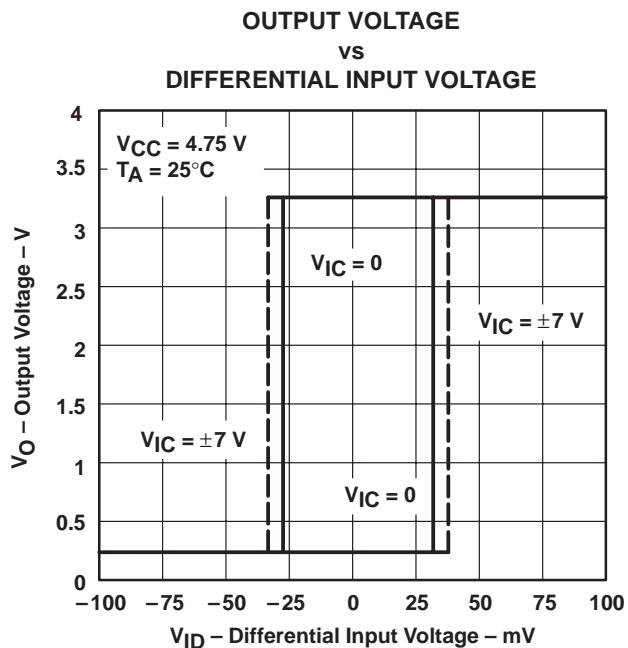


Figure 2

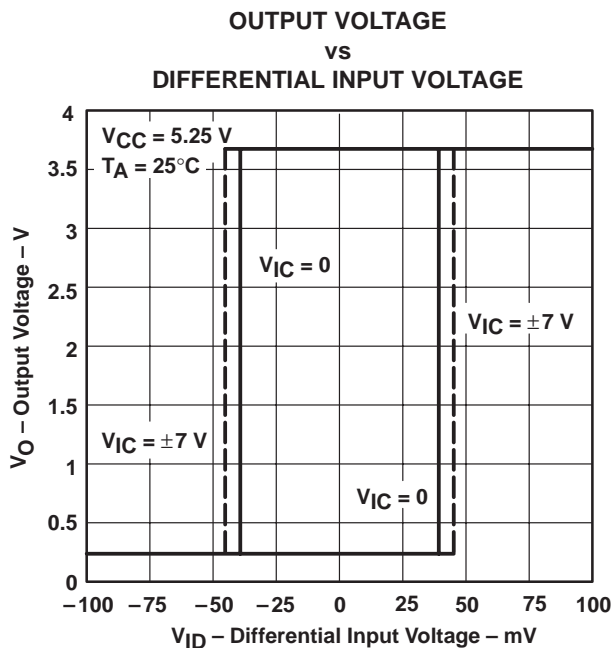


Figure 3

TYPICAL CHARACTERISTICS

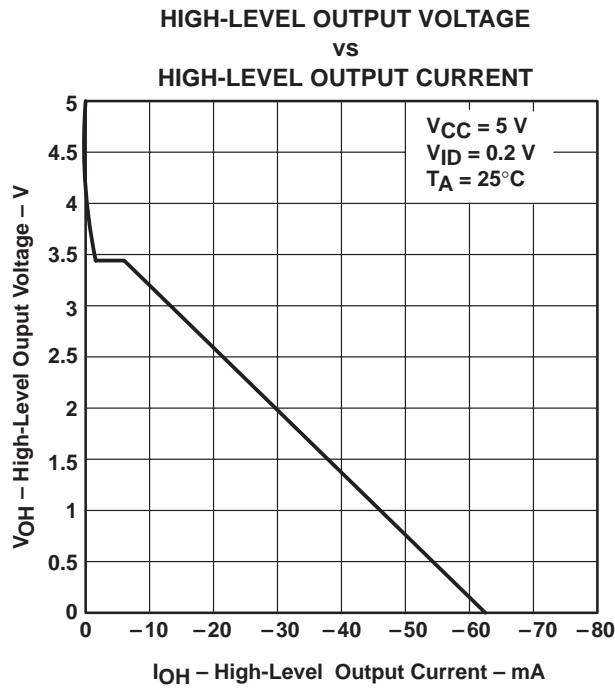


Figure 4

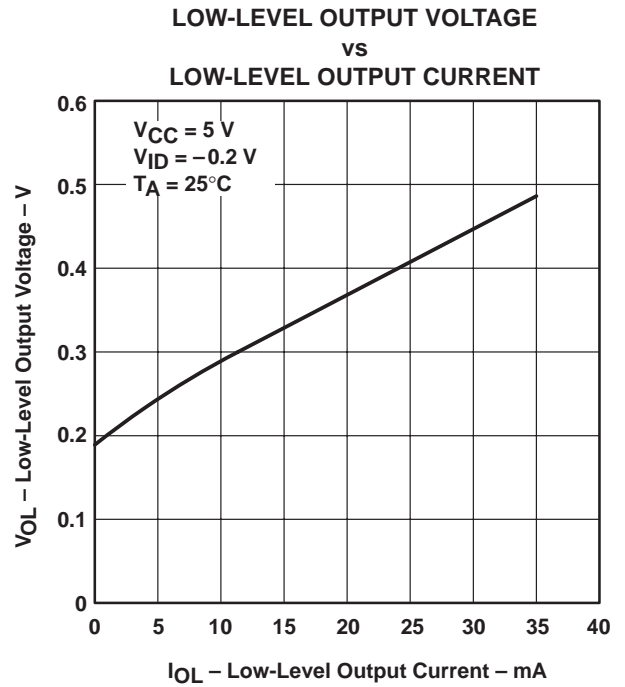


Figure 5

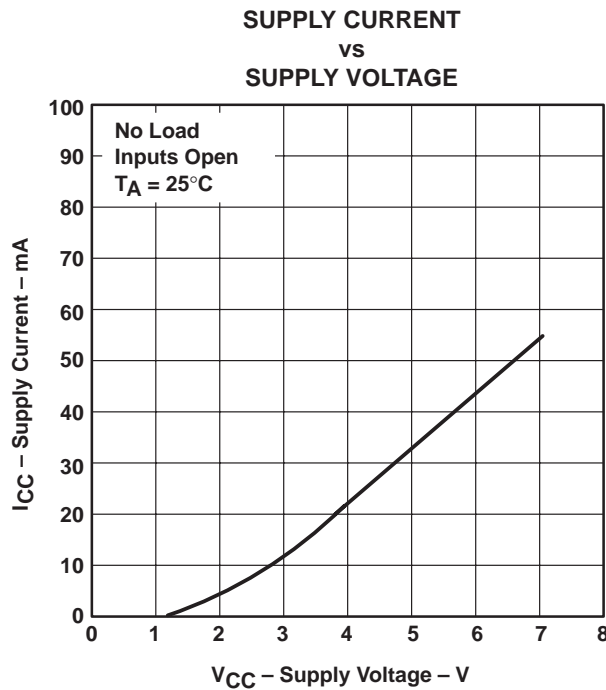


Figure 6

# uA9637AC DUAL DIFFERENTIAL LINE RECEIVER

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## APPLICATION INFORMATION

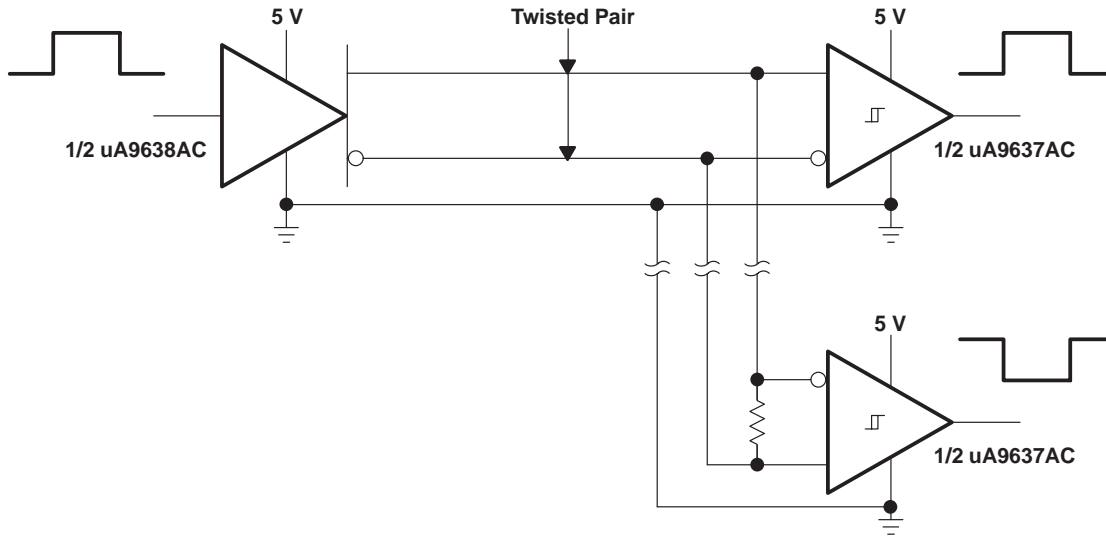


Figure 7. EIA/TIA-422-B System Applications

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UA9637ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	9637AC	<a href="#">Samples</a>
UA9637ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	9637AC	<a href="#">Samples</a>
UA9637ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	9637AC	<a href="#">Samples</a>
UA9637ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	9637AC	<a href="#">Samples</a>
UA9637ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 70	9637AC	<a href="#">Samples</a>
UA9637ACP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	UA9637ACP	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UA9637ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UA9637ACDR	SOIC	D	8	2500	340.5	338.1	20.6



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

### NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

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