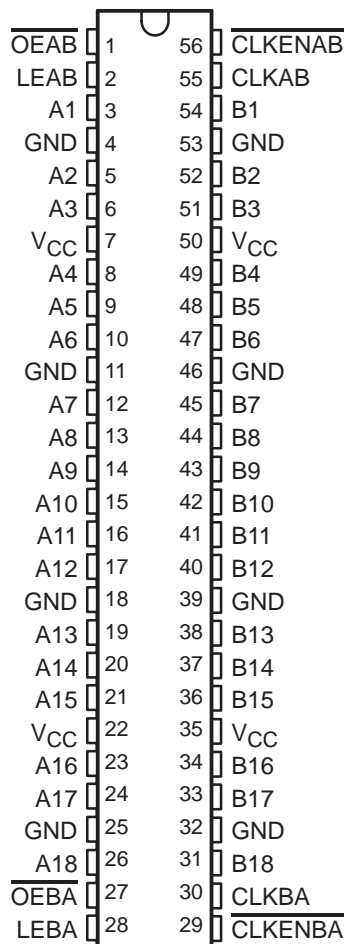


SN54ABT16601, SN74ABT16601 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS210C – JUNE 1992 – REVISED JANUARY 1997

- **Members of the Texas Instruments Widebus™ Family**
- **State-of-the-Art EPIC-II B™ BiCMOS Design Significantly Reduces Power Dissipation**
- **UBT™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 5 V$, $T_A = 25^\circ C$**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54ABT16601 . . . WD PACKAGE
SN74ABT16601 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, clocked, and clock-enabled modes.

Data flow in each direction is controlled by output-enable (\overline{OEAB} and \overline{OEBA}), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. Output enable \overline{OEAB} is active low. When \overline{OEAB} is low, the outputs are active. When \overline{OEAB} is high, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B, but uses \overline{OEBA} , LEBA, CLKBA, and $\overline{CLKENBA}$.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT16601 is characterized for operation over the full military temperature range of $-55^\circ C$ to $125^\circ C$. The SN74ABT16601 is characterized for operation from $-40^\circ C$ to $85^\circ C$.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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SN54ABT16601, SN74ABT16601
18-BIT UNIVERSAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

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FUNCTION TABLE†

INPUTS					OUTPUT B
CLKENAB	OEAB	LEAB	CLKAB	A	
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B ₀ ‡
H	L	L	X	X	B ₀ ‡
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B ₀ ‡
L	L	L	H	X	B ₀ §

† A-to-B data flow is shown; B-to-A flow is similar but uses OEBA, LEBA, CLKBA, and CLKENBA.

‡ Output level before the indicated steady-state input conditions were established

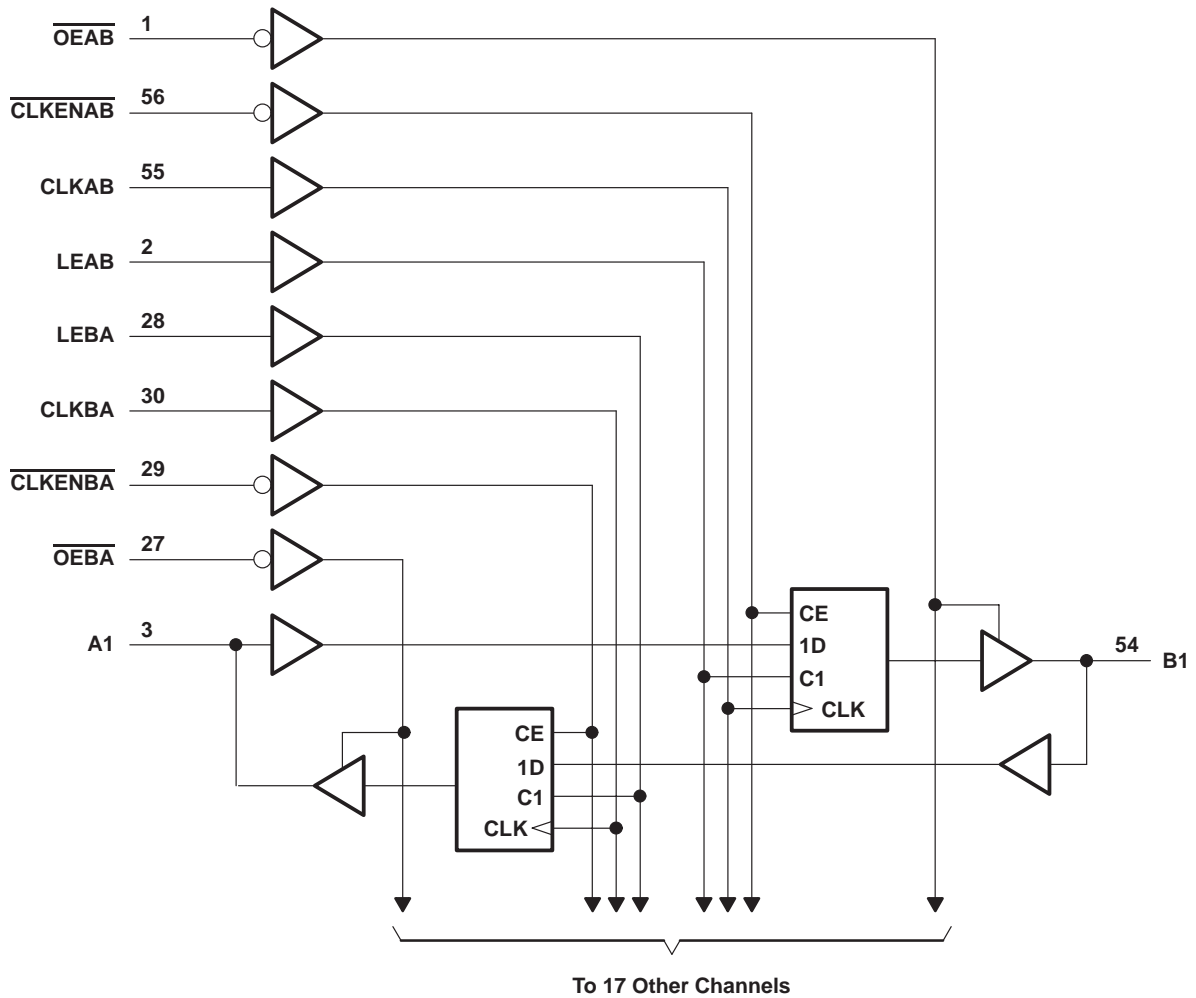
§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low



SN54ABT16601, SN74ABT16601
18-BIT UNIVERSAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	-0.5 V to 5.5 V
Current into any output in the low state, I_{OL} : SN54ABT16601	96 mA
SN74ABT16601	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	-18 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.



SN54ABT16601, SN74ABT16601 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 3)

		SN54ABT16601		SN74ABT16601		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		-24		-32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
T_A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			SN54ABT16601		SN74ABT16601		UNIT	
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX		
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			-1.2		-1.2		-1.2	V	
V_{OH}	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -3\text{ mA}$		2.5		2.5		2.5		V	
	$V_{CC} = 5\text{ V}$, $I_{OH} = -3\text{ mA}$		3		3		3			
	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -24\text{ mA}$		2		2				
							2			
V_{OL}	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 48\text{ mA}$		0.55		0.55			V	
		$I_{OL} = 64\text{ mA}$		0.55*			0.55			
V_{hys}			100						mV	
I_I	Control inputs	$V_{CC} = 5.5\text{ V}$, $V_I = V_{CC}\text{ or GND}$		± 1		± 1		± 1	μA	
	A or B ports			$\pm 20^{**}$		± 100		± 20		
I_{off}	$V_{CC} = 0$, $V_I\text{ or }V_O \leq 4.5\text{ V}$			± 100				± 100	μA	
I_{CEX}	$V_{CC} = 5.5\text{ V}$, $V_O = 5.5\text{ V}$	Outputs high		50		50		50	μA	
I_O^\ddagger	$V_{CC} = 5.5\text{ V}$, $V_O = 2.5\text{ V}$		-50	-100	-180	-50	-180	-50	-180	mA
I_{OZH}^\S	$V_{CC} = 5.5\text{ V}$, $V_O = 2.7\text{ V}$			10		10		10	μA	
I_{OZL}^\S	$V_{CC} = 5.5\text{ V}$, $V_O = 0.5\text{ V}$			-10		-10		-10	μA	
I_{CC}	A or B ports	$V_{CC} = 5.5\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$	Outputs high	1.9	3		2		3	mA
		Outputs low	28	36		35		36		
		Outputs disabled	1.6	3		2		3		
ΔI_{CC}^\P	$V_{CC} = 5.5\text{ V}$, One input at 3.4 V, Other inputs at V_{CC} or GND			50				50	μA	
						1.5			mA	
C_i	Control inputs	$V_I = 2.5\text{ V or }0.5\text{ V}$		3					pF	
C_{iO}	A or B ports	$V_O = 2.5\text{ V or }0.5\text{ V}$		9					pF	

* On products compliant to MIL-PRF-38535, this parameter does not apply.

** This limit applies only to the SN74ABT16601.

† All typical values are at $V_{CC} = 5\text{ V}$.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ The parameters I_{OZH} and I_{OZL} include the input leakage current.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



SN54ABT16601, SN74ABT16601 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN54ABT16601		SN74ABT16601		UNIT	
			MIN	MAX	MIN	MAX		
f_{clock}	Clock frequency		0	150	0	150	MHz	
t_w	Pulse duration	LEAB or LEBA high	2.5		2.5		ns	
		CLKAB or CLKBA high or low	3		3			
t_{su}	Setup time	A before CLKAB \uparrow or B before CLKBA \uparrow	4.6		4		ns	
		A before LEAB \downarrow or B before LEBA \downarrow	CLK high	2.5		2.5		
			CLK low	1.3		1		
		CLKEN before CLK \uparrow	2.9		2.5			
t_h	Hold time	A after CLKAB \uparrow or B after CLKBA \uparrow	0.4		0		ns	
		A after LEAB \downarrow or B after LEBA \downarrow	2.8		2			
		CLKEN after CLK \uparrow	0		0			

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT16601				UNIT	
			$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$			MIN		MAX
			MIN	TYP	MAX			
f_{max}			150	200		150	MHz	
t_{PLH}	A or B	B or A	1.5	2.5	4.1	1	4.6	ns
t_{PHL}			1.5	3.4	4.7	1	5.1	
t_{PLH}	LEAB or LEBA	B or A	2	3.4	4.7	1	5.6	ns
t_{PHL}			2	3.7	5	1	5.5	
t_{PLH}	CLKAB or CLKBA	B or A	1.5	3.2	4.5	1	5.2	ns
t_{PHL}			1.5	3.2	4.4	1	5	
t_{PZH}	$\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$	B or A	2	4	5	1	5.7	ns
t_{PZL}			2	4.2	5.6	1	6	
t_{PHZ}	$\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$	B or A	2	4.5	5.8	1	6.8	ns
t_{PLZ}			1.5	3.4	5.3	1	6.3	

SN54ABT16601, SN74ABT16601
18-BIT UNIVERSAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

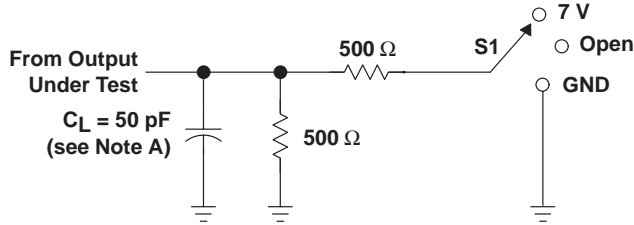
SCBS210C – JUNE 1992 – REVISED JANUARY 1997

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT16601				UNIT	
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN		MAX
			MIN	TYP	MAX			
f_{max}			150	200		150	MHz	
t_{PLH}	A or B	B or A	1.5	2.5	3.6	1.5	4	ns
t_{PHL}			1.5	3.4	4.7	1.5	4.9	
t_{PLH}	LEAB or LEBA	B or A	2	3.4	4.7	2	5	ns
t_{PHL}			2	3.7	5	2	5.2	
t_{PLH}	CLKAB or CLKBA	B or A	1.5	3.2	4.5	1.5	4.7	ns
t_{PHL}			1.5	3.2	4.4	1.5	4.6	
t_{PZH}	\overline{OEAB} or \overline{OEBA}	B or A	2	4	5	2	5.5	ns
t_{PZL}			2	4.2	5.6	2	5.8	
t_{PHZ}	\overline{OEAB} or \overline{OEBA}	B or A	2	4.5	5.4	2	6.2	ns
t_{PLZ}			1.5	3.4	4.7	1.5	5.4	

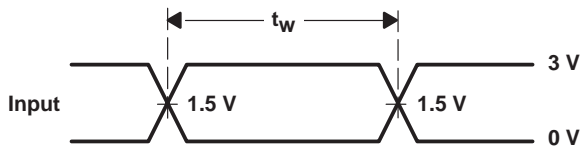


PARAMETER MEASUREMENT INFORMATION

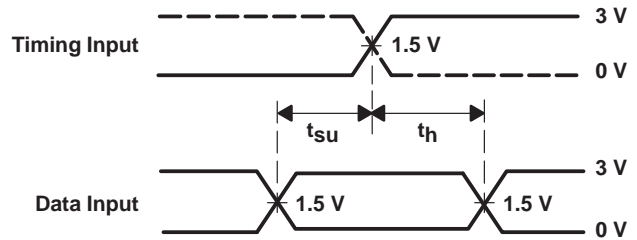


LOAD CIRCUIT

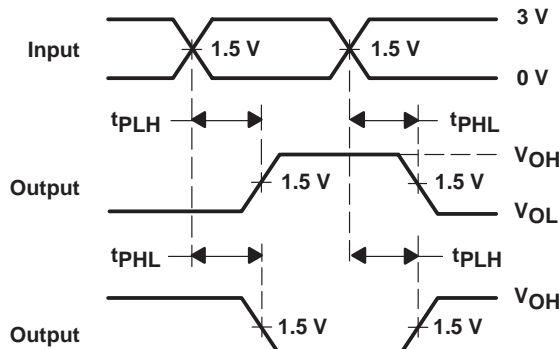
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



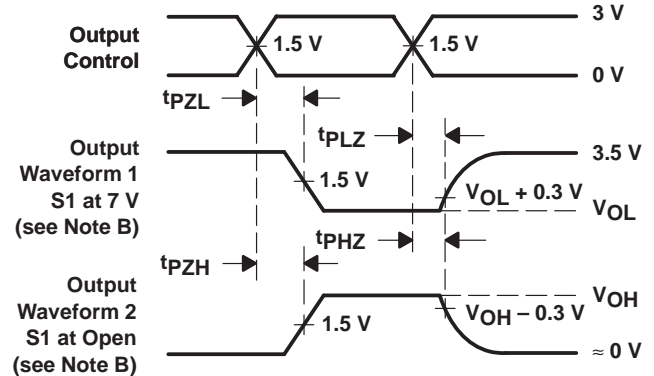
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ABT16601DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16601	Samples
SN74ABT16601DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16601	Samples
SN74ABT16601DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16601	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

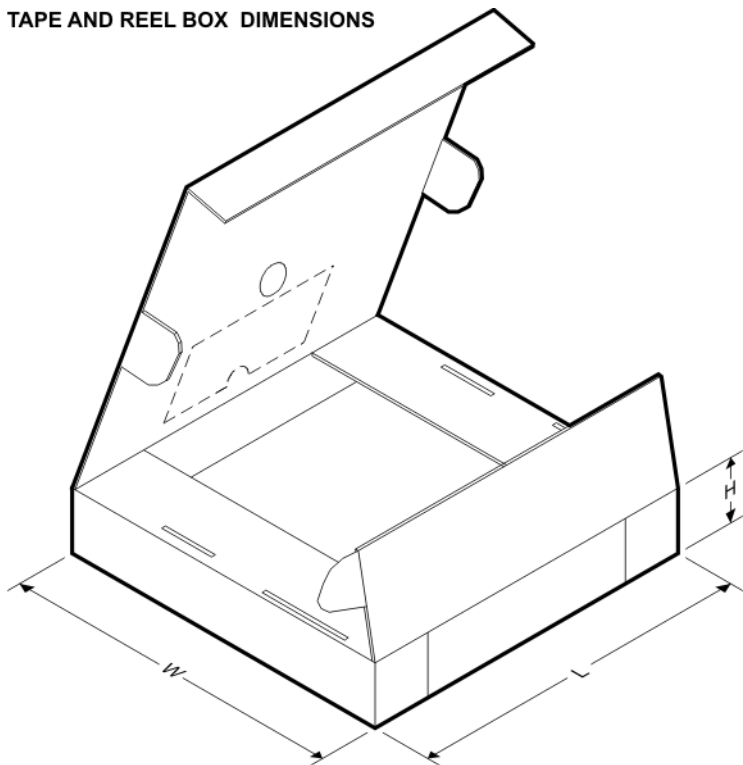
TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT16601DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74ABT16601DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS


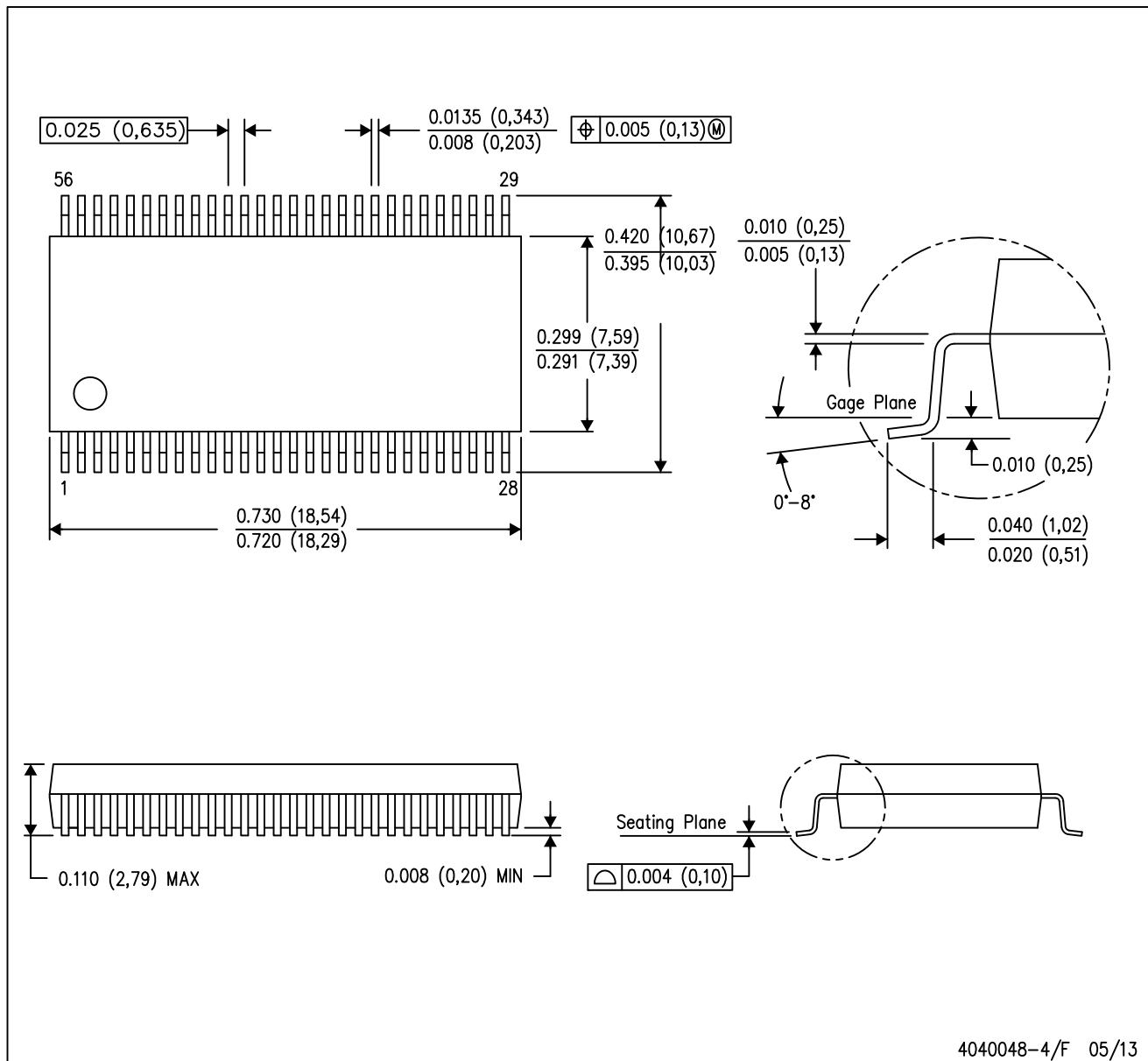
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT16601DGGR	TSSOP	DGG	56	2000	367.0	367.0	45.0
SN74ABT16601DLR	SSOP	DL	56	1000	367.0	367.0	55.0

MECHANICAL DATA

DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.

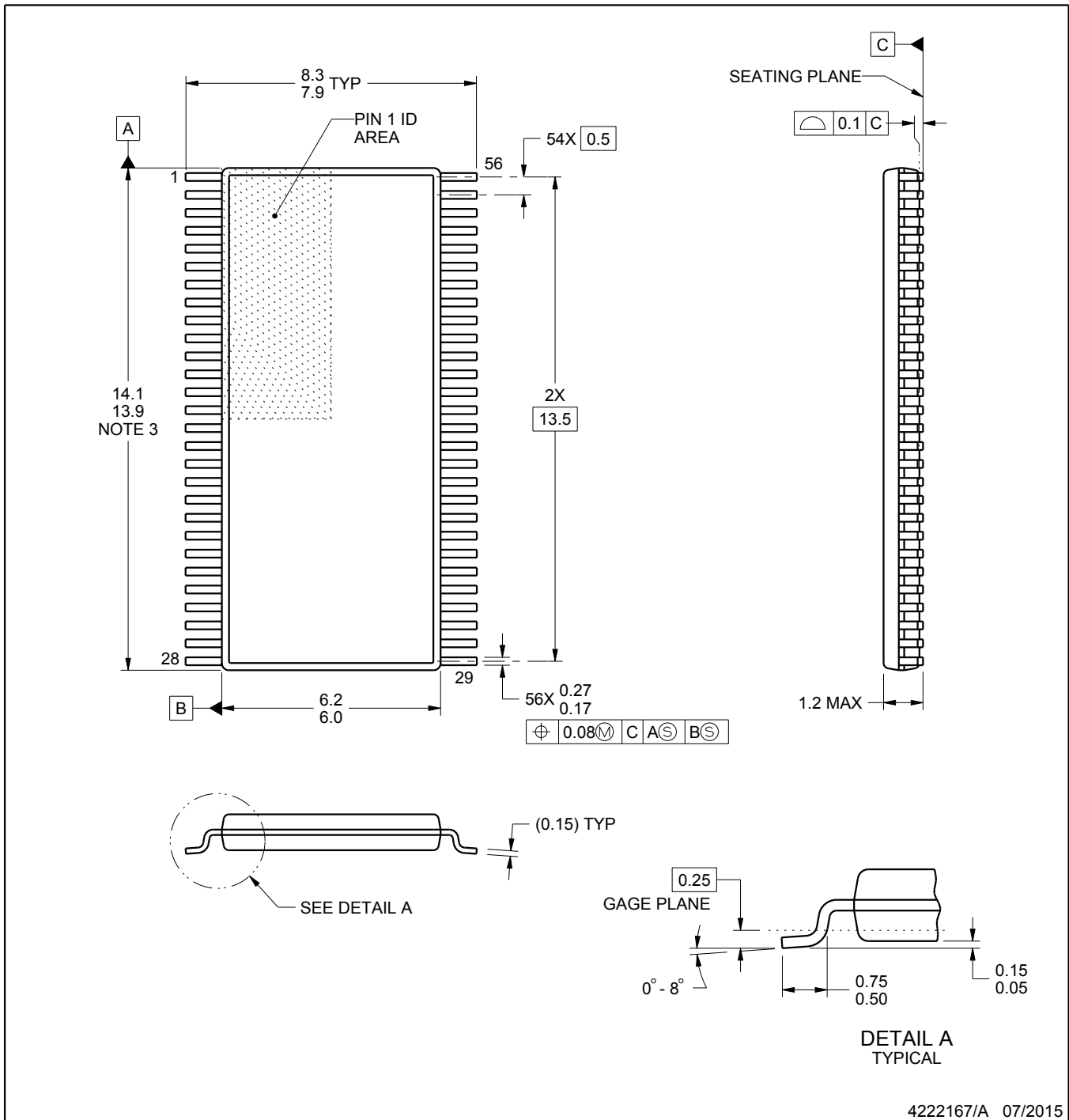
DGG0056A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



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NOTES:

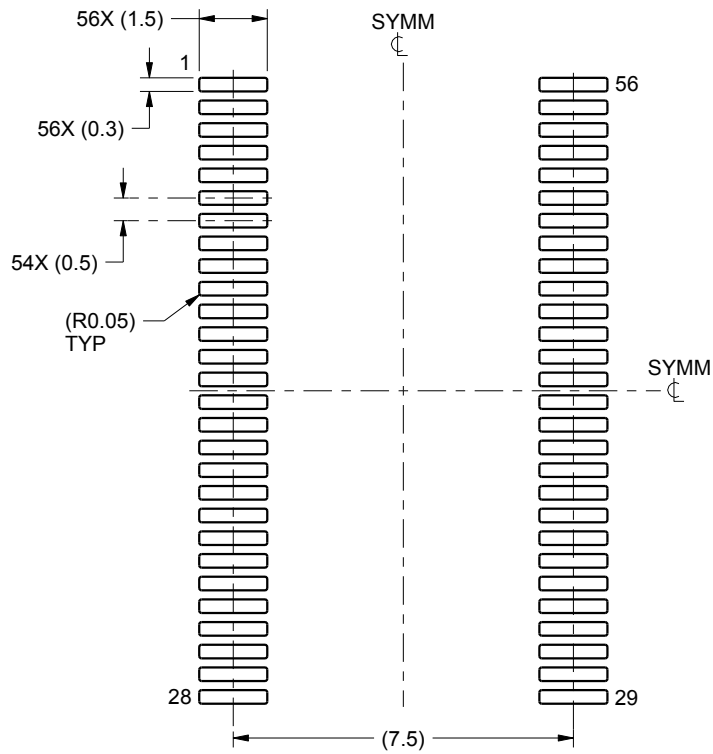
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

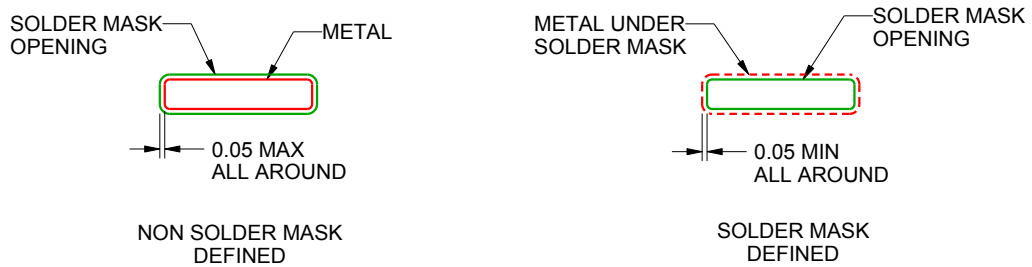
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

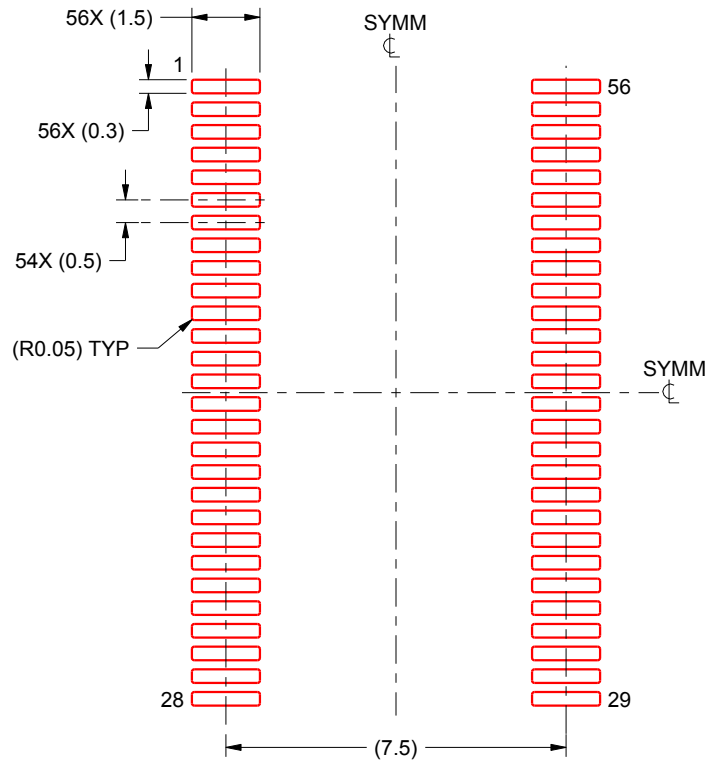
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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