Low Power 14-Bit, 400ksps Sampling ADC

FEATURES

- **Sample Rate: 400ksps**
- **Power Dissipation: 70mW**
- **Guaranteed ±1.5LSB DNL, ±2LSB INL (Max)**
- **80.5dB S/(N + D) and 93dB THD at 100kHz**
- **80dB S/(N + D) and 90dB THD at Nyquist**
- Nap and Sleep Shutdown Modes
- Operates with Internal or External Reference
- True Differential Inputs Reject Common Mode Noise
- 15MHz Full Power Bandwidth Sampling
- ±2.5V Bipolar Input Range
- 28-Pin SSOP Package

APPLICATIONS

- Telecommunications
- Digital Signal Processing
- Multiplexed Data Acquisition Systems
- High Speed Data Acquisition
- Spectrum Analysis
- Imaging Systems

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DESCRIPTION

The LTC®1416 is a 2.2μs, 400ksps, 14-bit sampling A/D converter that draws only 70mW from ±5V supplies. This easy-to-use device includes a high dynamic range sample-and-hold and a precision reference. Two digitally selectable power shutdown modes provide flexibility for low power systems.

The LTC1416's full-scale input range is ±2.5V. Maximum DC specifications include ±2LSB INL, ±1.5LSB DNL over temperature. Outstanding AC performance includes 80.5dB S/(N + D) and 93dB THD with a 100kHz input, and 80dB S/(N + D) and 90dB THD at the Nyquist input frequency of 200kHz.

The unique differential input sample-and-hold can acquire single-ended or differential input signals up to its 15MHz bandwidth. The 60dB common mode rejection allows users to eliminate ground loops and common mode noise by measuring signals differentially from the source.
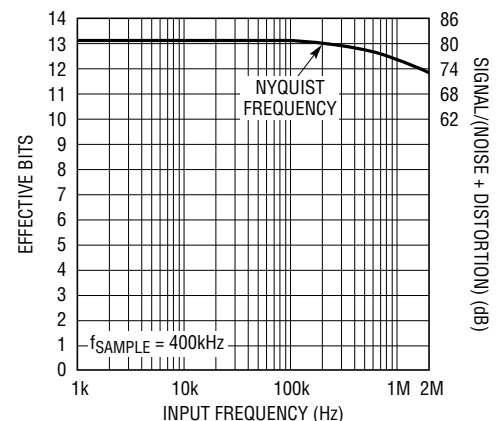
The ADC has a μP compatible, 14-bit parallel output port. There is no pipeline delay in the conversion results. A separate convert start input and a data ready signal ($\overline{BUSY}$) ease connections to FIFOs, DSPs and microprocessors.

TYPICAL APPLICATION

Complete, 70mW, 14-Bit ADC with 80.5dB S/(N + D)
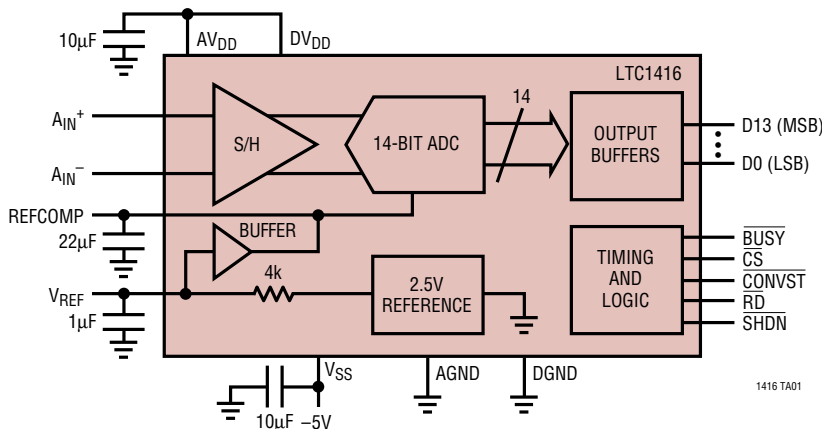
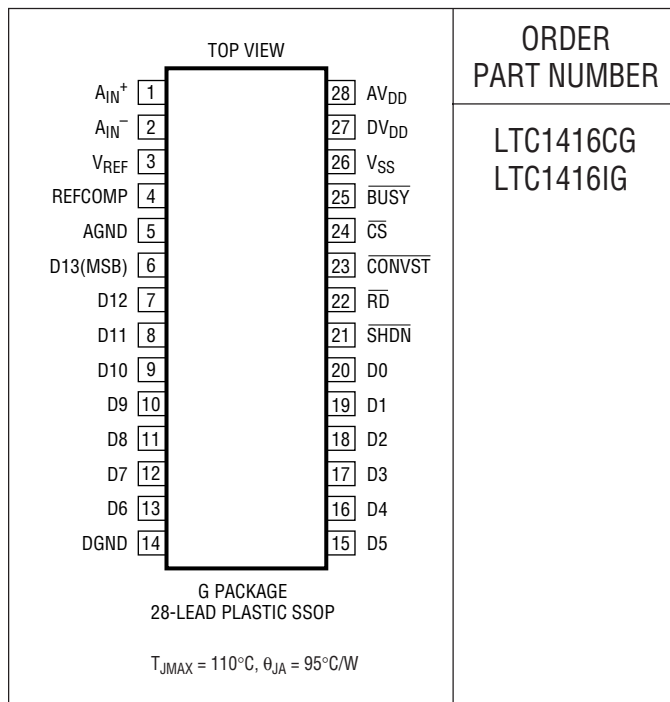Effective Bits and Signal-to-(Noise + Distortion) vs Input Frequency

ABSOLUTE MAXIMUM RATINGS

$AV_{DD} = DV_{DD} = V_{DD}$ (Notes 1, 2)

Supply Voltage (V_{DD}) 6V
Negative Supply Voltage (V_{SS}) .... −6V
Total Supply Voltage (V_{DD} to V_{SS}) 12V
Analog Input Voltage
  (Note 3) .... (V_{SS} − 0.3V) to (V_{DD} + 0.3V)
Digital Input Voltage (Note 4) .... (V_{SS} − 0.3V) to 10V
Digital Output Voltage .... (V_{SS} − 0.3V) to (V_{DD} + 0.3V)
Power Dissipation 500mW
Operating Temperature Range
  Commercial .... 0°C to 70°C
  Industrial .... −40°C to 85°C
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION

```
              TOP VIEW
        ┌──────────────────┐
 AIN⁺ [1]                  [28] AVDD
 AIN⁻ [2]                  [27] DVDD
 VREF [3]                  [26] VSS
REFCOMP [4]                [25] BUSY
 AGND [5]                  [24] CS
D13(MSB) [6]               [23] CONVST
  D12 [7]                  [22] RD
  D11 [8]                  [21] SHDN
  D10 [9]                  [20] D0
   D9 [10]                 [19] D1
   D8 [11]                 [18] D2
   D7 [12]                 [17] D3
   D6 [13]                 [16] D4
 DGND [14]                 [15] D5
        └──────────────────┘
          G PACKAGE
     28-LEAD PLASTIC SSOP

  TJMAX = 110°C, θJA = 95°C/W
```

ORDER PART NUMBER
LTC1416CG
LTC1416IG

Consult factory for Military grade parts and for A grade parts.

CONVERTER CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. With Internal Reference (Notes 5, 6)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	13			Bits
Integral Linearity Error	(Note 7)	●		±0.8	±2	LSB
Differential Linearity Error		●		±0.7	±1.5	LSB
Offset Error	(Note 8)	●		±5	±20	LSB
Full-Scale Error	Internal Reference External Reference = 2.5V			±20 ±10	±60 ±40	LSB LSB
Full-Scale Tempco	$I_{OUT(REF)} = 0$			±15		ppm/°C

ANALOG INPUT

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range (Note 9)	$4.75V \le V_{DD} \le 5.25V, -5.25V \le V_{SS} \le -4.75V$	●		±2.5		V
I_{IN}	Analog Input Leakage Current	$\overline{CS}$ = High	●			±1	µA
C_{IN}	Analog Input Capacitance	Between Conversions During Conversions			15 5		pF pF
t_{ACQ}	Sample-and-Hold Acquisition Time	(Note 9)	●		100	400	ns
t_{AP}	Sample-and-Hold Aperture Delay Time				−1.5		ns
t_{jitter}	Sample-and-Hold Aperture Delay Time Jitter				2		ps_{RMS}
CMRR	Analog Input Common Mode Rejection Ratio	$-2.5V < (A_{IN}^- = A_{IN}^+) < 2.5V$			60		dB

DYNAMIC ACCURACY
The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-(Noise + Distortion) Ratio	100kHz Input Signal 200kHz Input Signal	●	77	80.5 80		dB dB
THD	Total Harmonic Distortion	100kHz Input Signal, First 5 Harmonics 200kHz Input Signal, First 5 Harmonics	●		−93 −90	−86	dB dB
SFDR	Spurious-Free Dynamic Range	100kHz Input Signal	●		−95	−86	dB
IMD	Intermodulation Distortion	$f_{IN1} = 87.01172kHz$, $f_{IN2} = 113.18359kHz$			−90		dB
	Full Power Bandwidth				15		MHz
	Full Linear Bandwidth	S/(N + D) ≥ 77dB			0.8		MHz

INTERNAL REFERENCE CHARACTERISTICS
The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	$I_{OUT} = 0$		2.480	2.500	2.520	V
V_{REF} Output Tempco	$I_{OUT} = 0$			±15		ppm/°C
V_{REF} Line Regulation	$4.75V ≤ V_{DD} ≤ 5.25V$ $−5.25V ≤ V_{SS} ≤ −4.75V$			0.05 0.05		LSB/V LSB/V
V_{REF} Output Resistance	$−0.1mA ≤ |I_{OUT}| ≤ 0.1mA$			4		kΩ
COMP Output Voltage	$I_{OUT} = 0$			4.06		V

DIGITAL INPUTS AND DIGITAL OUTPUTS
The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	$V_{DD} = 5.25V$	●	2.4			V
V_{IL}	Low Level Input Voltage	$V_{DD} = 4.75V$	●			0.8	V
I_{IN}	Digital Input Current	$V_{IN} = 0V$ to V_{DD}	●			±10	μA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	$V_{DD} = 4.75V$ $I_{OUT} = −10μA$ $I_{OUT} = −200μA$	●	4.0	4.5		V V
V_{OL}	Low Level Output Voltage	$V_{DD} = 4.75V$ $I_{OUT} = 160μA$ $I_{OUT} = 1.6mA$	●		0.05 0.10	0.4	V V
I_{OZ}	Hi-Z Output Leakage D13 to D0	$V_{OUT} = 0V$ to V_{DD}, $\overline{CS}$ High	●			±10	μA
C_{OZ}	Hi-Z Output Capacitance D13 to D0	$\overline{CS}$ High (Note 9)	●			15	pF
I_{SOURCE}	Output Source Current	$V_{OUT} = 0V$			−10		mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{DD}$			10		mA

POWER REQUIREMENTS
The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Positive Supply Voltage	(Note 10)		4.75		5.25	V
V_{SS}	Negative Supply Voltage	(Note 10)		−4.75		−5.25	V
I_{DD}	Positive Supply Current Nap Mode Sleep Mode	 $\overline{SHDN} = 0V$, $\overline{CS} = 0V$ $\overline{SHDN} = 0V$, $\overline{CS} = 5V$	●		7 1 1	10 1.6	mA mA μA

POWER REQUIREMENTS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{SS}	Negative Supply Current		●		7	10	mA
	Nap Mode	$\overline{SHDN} = 0V$, $\overline{CS} = 0V$			20		µA
	Sleep Mode	$\overline{SHDN} = 0V$, $\overline{CS} = 5V$			15		µA
P_{DISS}	Power Dissipation		●		70	100	mW
	Power Dissipation, Nap Mode	$\overline{SHDN} = 0V$, $\overline{CS} = 0V$			4	6	mW
	Power Dissipation, Sleep Mode	$\overline{SHDN} = 0V$, $\overline{CS} = 5V$			0.1		mW

TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 5, see Figures 15 to 21)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$f_{SAMPLE(MAX)}$	Maximum Sampling Frequency		●	400			kHz
t_{CONV}	Conversion Time		●	1.5	1.9	2.2	µs
t_{ACQ}	Acquisition Time	(Note 9)	●		100	400	ns
$t_{ACQ+CONV}$	Acquisition + Conversion Time		●		2	2.5	µs
t_1	$\overline{CS}$ to $\overline{RD}$ Setup Time	(Notes 9, 10)	●	0			ns
t_2	$\overline{CS}\downarrow$ to $\overline{CONVST}\downarrow$ Setup Time	(Notes 9, 10)	●	10			ns
t_3	$\overline{CS}\downarrow$ to $\overline{SHDN}\downarrow$ Setup Time	(Notes 9, 10)	●	10			ns
t_4	$\overline{SHDN}\uparrow$ to $\overline{CONVST}\downarrow$ Wake-Up Time	$\overline{CS} = 0V$ (Note 10)			400		ns
t_5	$\overline{CONVST}$ Low Time	(Notes 10, 11)	●	40			ns
t_6	$\overline{CONVST}$ to $\overline{BUSY}$ Delay	$C_L = 25pF$			25		ns
			●			50	ns
t_7	Data Ready Before $\overline{BUSY}\uparrow$	(Note 9)		75	100		ns
			●	50			ns
t_8	Delay Between Conversions	(Note 10)	●	40			ns
t_9	Wait Time $\overline{RD}\downarrow$ After $\overline{BUSY}\uparrow$		●	−5			ns
t_{10}	Data Access Time After $\overline{RD}\downarrow$	$C_L = 25pF$			15	25	ns
			●			35	ns
		$C_L = 100pF$			20	35	ns
			●			50	ns
t_{11}	Bus Relinquish Time				8	20	ns
		$0°C \leq T_A \leq 70°C$	●			25	ns
		$-40°C \leq T_A \leq 85°C$	●			30	ns
t_{12}	$\overline{RD}$ Low Time		●	t_{10}			ns
t_{13}	$\overline{CONVST}$ High Time		●	40			ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND and AGND wired together unless otherwise noted.

Note 3: When these pin voltages are taken below V_{SS} or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents greater than 100mA below V_{SS} or above V_{DD} without latchup.

Note 4: When these pin voltages are taken below V_{SS}, they will be clamped by internal diodes. This product can handle input currents greater than 100mA below V_{SS} without latchup. These pins are not clamped to V_{DD}.

Note 5: $V_{DD} = 5V$, $V_{SS} = -5V$, $f_{SAMPLE} = 400kHz$, $t_r = t_f = 5ns$ unless otherwise specified.

Note 6: Linearity, offset and full-scale specifications apply for a single-ended A_{IN}^+ input with A_{IN}^- grounded.

Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 8: Bipolar offset is the offset voltage measured from −0.5LSB when the output code flickers between 0000 0000 0000 00 and 1111 1111 1111 11.

Note 9: Guaranteed by design, not subject to test.

Note 10: Recommended operating conditions.

Note 11: The falling $\overline{CONVST}$ edge starts a conversion. If $\overline{CONVST}$ returns high at a critical point during the conversion it can create small errors. For best results ensure that $\overline{CONVST}$ returns high either within 900ns after the start of the conversion or after $\overline{BUSY}$ rises.

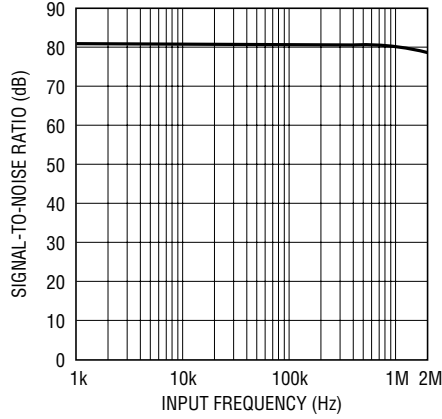# TYPICAL PERFORMANCE CHARACTERISTICS
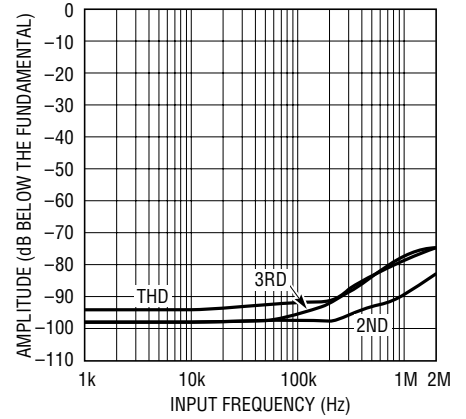
S/(N + D) vs Input Frequency and Amplitude
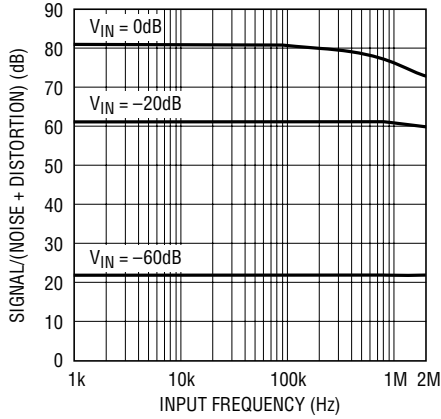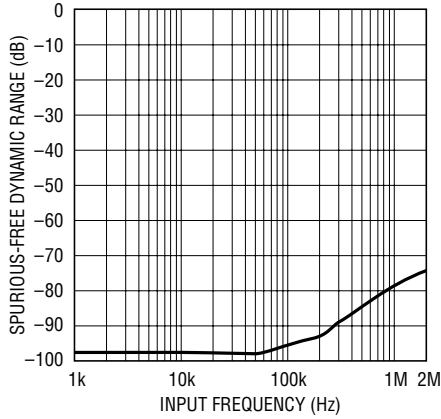
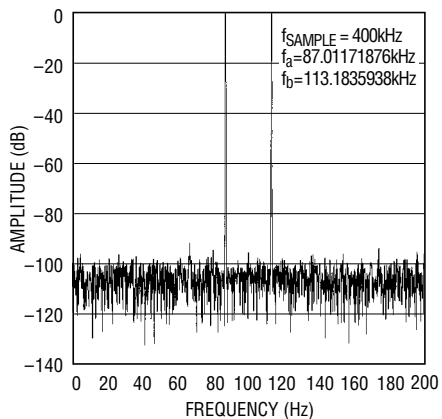### Signal-to-Noise Ratio vs Input Frequency

Distortion vs Input Frequency

Spurious-Free Dynamic Range vs Input Frequency

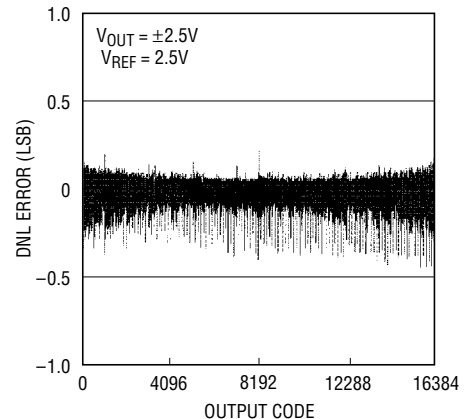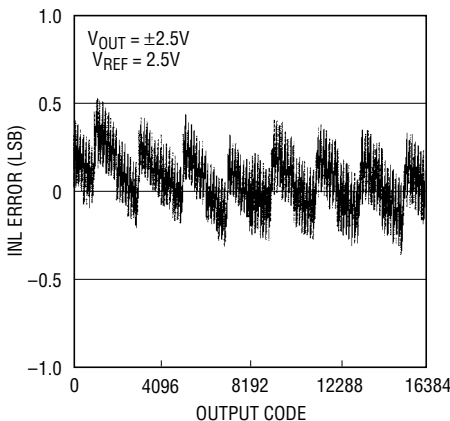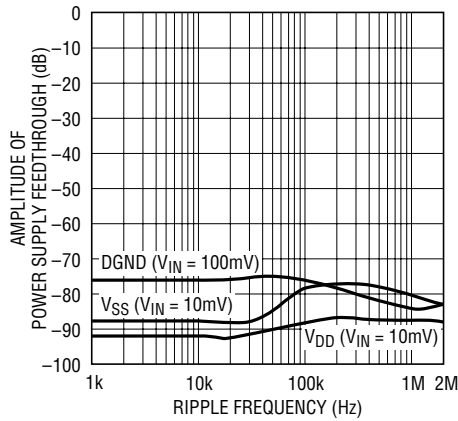### Intermodulation Distortion Plot

Differential Nonlinearity vs Output Code

Integral Nonlinearity vs Output Code

Power Supply Feedthrough vs Ripple Frequency

Input Common Mode Rejection vs Input Frequency

LTC1416
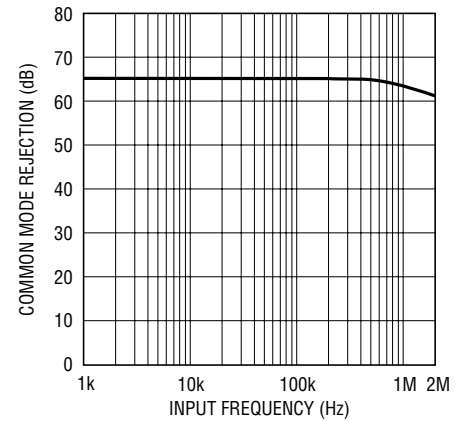
PIN FUNCTIONS

A_{IN}^+ **(Pin 1):** ±2.5V Positive Analog Input.

A_{IN}^- **(Pin 2):** ±2.5V Negative Analog Input.

V_{REF} **(Pin 3):** 2.5V Reference Output. Bypass to AGND with 1μF.

REFCOMP (Pin 4): 4.06V Reference Output. Bypass to AGND with 22μF tantalum in parallel with 0.1μF ceramic, or 22μF ceramic.

AGND (Pin 5): Analog Ground.

D13 to D6 (Pins 6 to 13): Three-State Data Outputs.

DGND (Pin 14): Digital Ground for Internal Logic. Tie to AGND.

D5 to D0 (Pins 15 to 20): Three-State Data Outputs.

SHDN (Pin 21): Power Shutdown Input. Low selects shutdown. Shutdown mode selected by CS. CS = 0 for nap mode and CS = 1 for sleep mode.

RD (Pin 22): Read Input. This enables the output drivers when CS is low.

CONVST (Pin 23): Conversion Start Signal. This active low signal starts a conversion on its falling edge.

CS (Pin 24): The Chip Select input must be low for the ADC to recognize CONVST and RD inputs. CS also sets the shutdown mode when SHDN goes low. CS and SHDN low select the quick wake-up nap mode. CS high and SHDN low select sleep mode.

BUSY (Pin 25): The BUSY output shows the converter status. It is low when a conversion is in progress. Data is valid on the rising edge of BUSY.

V_{SS} **(Pin 26):** –5V Negative Supply. Bypass to AGND with 10μF tantalum in parallel with 0.1μF ceramic, or 10μF ceramic.

DV_{DD} **(Pin 27):** 5V Positive Supply. Tie to Pin 28.

AV_{DD} **(Pin 28):** 5V Positive Supply. Bypass to AGND with 10μF tantalum in parallel with 0.1μF ceramic, or 10μF ceramic.
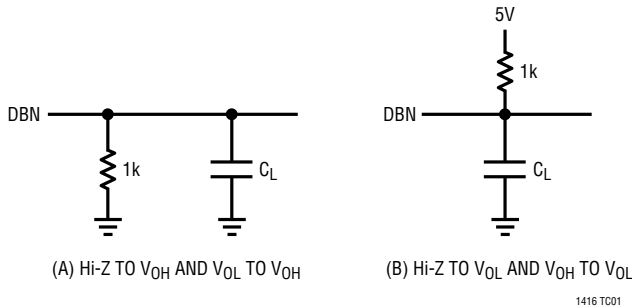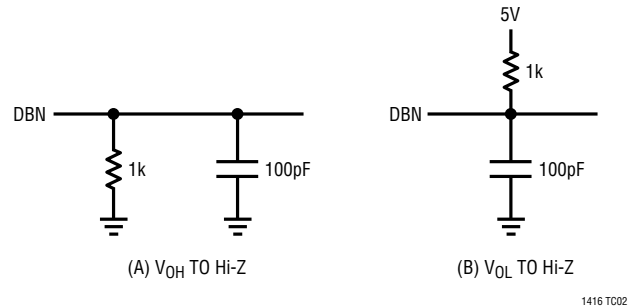
FUNCTIONAL BLOCK DIAGRAM

1416 BD

6
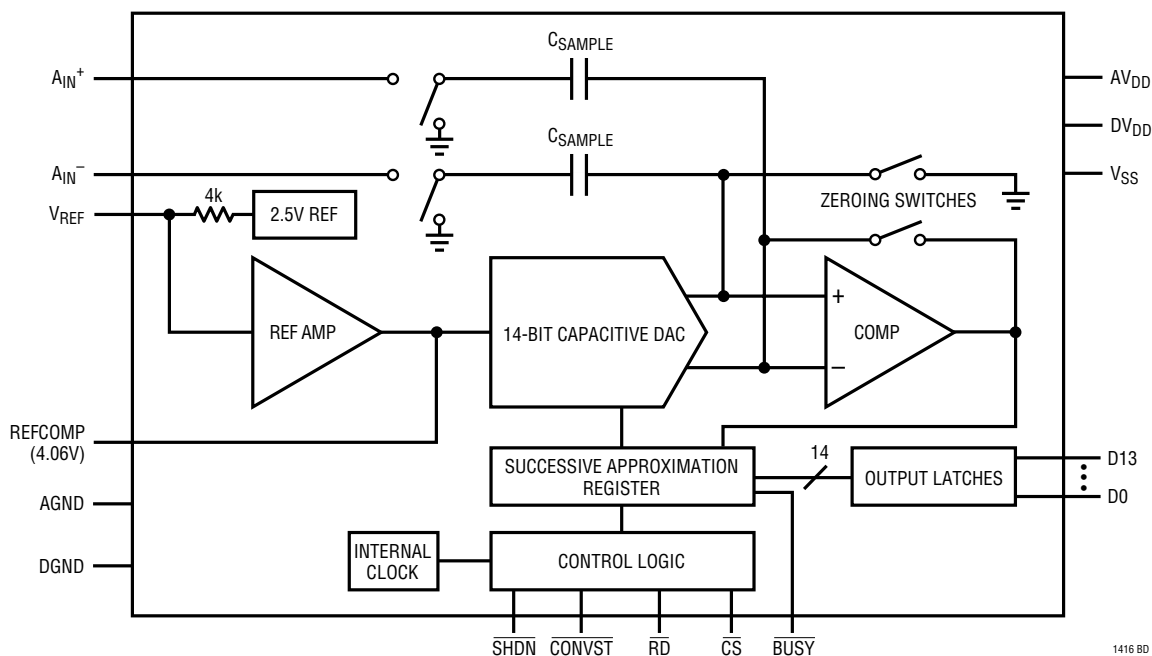
TEST CIRCUITS

Load Circuits for Access Timing

(A) Hi-Z TO V_{OH} AND V_{OL} TO V_{OH}

(B) Hi-Z TO V_{OL} AND V_{OH} TO V_{OL}

1416 TC01

Load Circuits for Output Float Delay

(A) V_{OH} TO Hi-Z

(B) V_{OL} TO Hi-Z

1416 TC02

APPLICATIONS INFORMATION

CONVERSION DETAILS

The LTC1416 uses a successive approximation algorithm and an internal sample-and-hold circuit to convert an analog signal to a 14-bit parallel output. The ADC is complete with a precision reference and an internal clock. The control logic provides easy interface to microprocessors and DSPs. (Please refer to the Digital Interface section for the data format.)
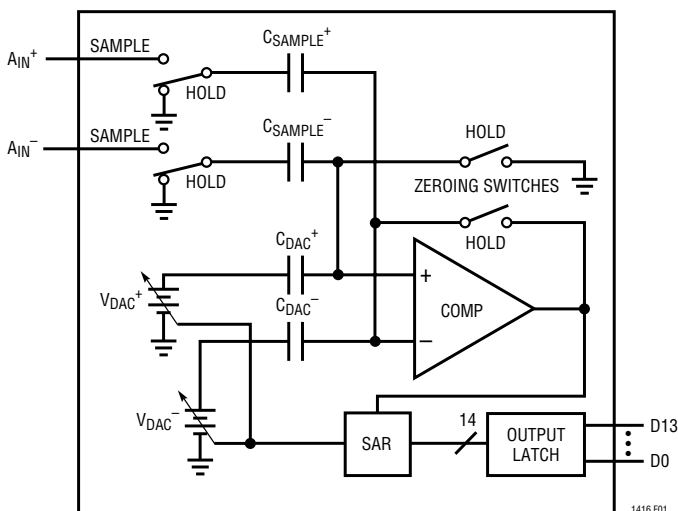
Figure 1. Simplified Block Diagram

Conversion start is controlled by the $\overline{CS}$ and $\overline{CONVST}$ inputs. At the start of the conversion, the successive approximation register (SAR) is reset. Once a conversion cycle has begun, it cannot be restarted.

During the conversion, the internal differential 14-bit capacitive DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 1, the A_{IN}^+ and A_{IN}^- inputs are connected to the sample-and-hold capacitors (C_{SAMPLE}) during the acquire phase and the comparator offset is nulled by the zeroing switches. In this acquire phase, a minimum delay of 400ns will provide enough time for the sample-and-hold capacitors to acquire the analog signal. During the convert phase the comparator zeroing switches open, putting the comparator into compare mode. The input switches connect the C_{SAMPLE} capacitors to ground, transferring the differential analog input charge onto the summing junction. This input charge is successively compared with the binary-weighted charges supplied by the differential capacitive DAC. Bit decisions are made by the high speed comparator. At the end of a conversion, the differential DAC output balances the A_{IN}^+ and A_{IN}^- input charges. The SAR contents (a 14-bit data word) which represents the difference of A_{IN}^+ and A_{IN}^- are loaded into the 14-bit output latches.

7

APPLICATIONS INFORMATION

DYNAMIC PERFORMANCE

The LTC1416 has excellent high speed sampling capability. FFT (Fast Fourier Transform) test techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. Figure 2 shows a typical LTC1416 FFT plot.
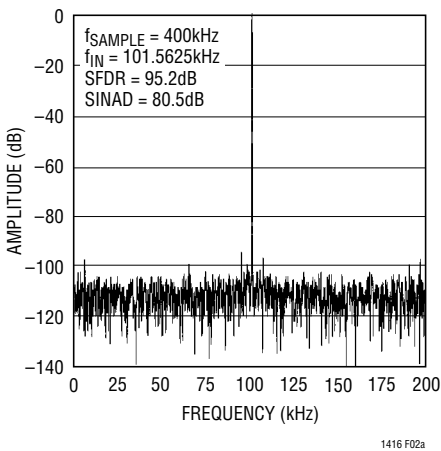

f$_{SAMPLE}$ = 400kHz
f$_{IN}$ = 101.5625kHz
SFDR = 95.2dB
SINAD = 80.5dB

Figure 2a. LTC1416 Nonaveraged, 4096 Point FFT, Input Frequency = 100kHz

f$_{SAMPLE}$ = 400kHz
f$_{IN}$ = 189.9414kHz
SFDR = 94.8dB
SINAD = 80.2dB
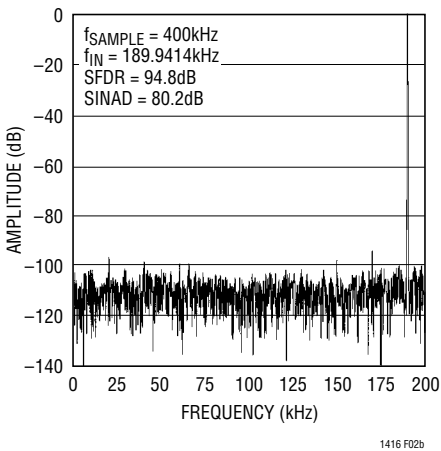
Figure 2b. LTC1416 Nonaveraged, 4096 Point FFT, Input Frequency = 190kHz

Signal-to-Noise Ratio

The Signal-to-Noise plus Distortion Ratio [S/(N + D)] is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. The output is band limited to frequencies from above DC and below half the sampling frequency. Figure 2a shows a typical spectral content with a 400kHz sampling rate and a 100kHz input. The dynamic performance is excellent for input frequencies up to and beyond the Nyquist limit of 200kHz, Figure 2b.

Effective Number of Bits

The Effective Number of Bits (ENOBs) is a measurement of the resolution of an ADC and is directly related to the S/(N + D) by the equation:

$$ENOB = [S/(N + D) - 1.76]/6.02$$

where ENOB is the Effective Number of Bits of resolution and S/(N + D) is expressed in dB. At the maximum sampling rate of 400kHz, the LTC1416 maintains near ideal ENOBs up to the Nyquist input frequency of 200kHz (refer to Figure 3).
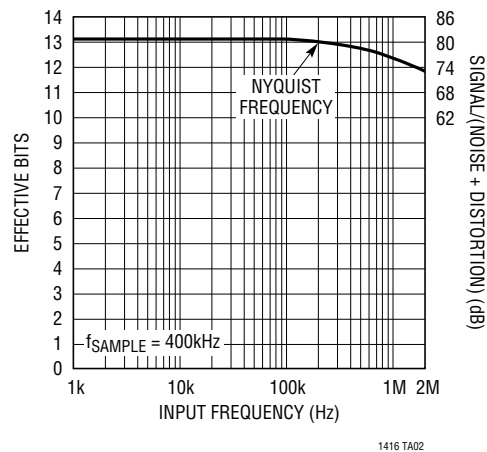

f$_{SAMPLE}$ = 400kHz

Figure 3. Effective Bits and Signal/(Noise + Distortion) vs Input Frequency

APPLICATIONS INFORMATION

Total Harmonic Distortion

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = 20 \log \frac{\sqrt{V2^2 + V3^2 + V4^2 + ...Vn^2}}{V1}$$

where V1 is the RMS amplitude of the fundamental frequency and V2 through Vn are the amplitudes of the second through Nth harmonics. THD versus input frequency is shown in Figure 4. The LTC1416 has good distortion performance up to the Nyquist frequency and beyond.
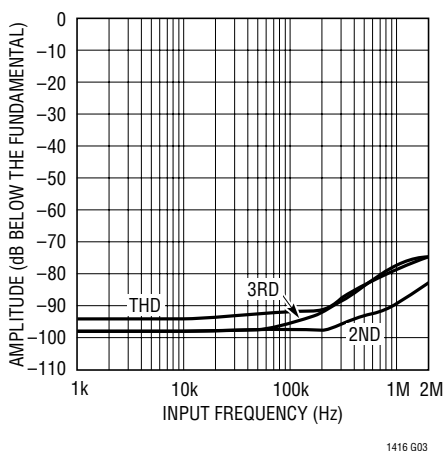
Figure 4. Distortion vs Input Frequency

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies fa and fb are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at the sum and difference frequencies of mfa ± nfb, where m and n = 0, 1, 2, 3, etc. For example, the 2nd order IMD terms include (fa + fb). If the two input sine waves are equal in magnitude, the value (in decibels) of the 2nd order IMD products can be expressed by the following formula:

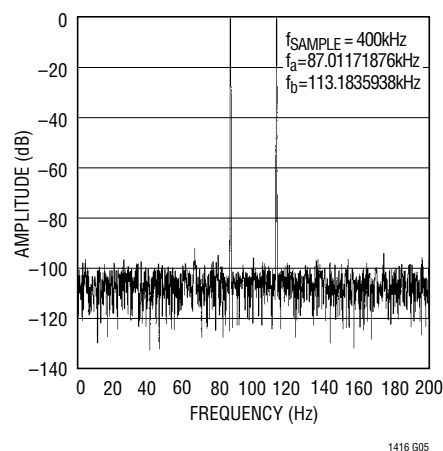$$IMD(fa + fb) = 20 \log \frac{\text{Amplitude at } (fa + fb)}{\text{Amplitude at fa}}$$

Figure 5. Intermodulation Distortion Plot

Peak Harmonic or Spurious Noise

The peak harmonic or spurious noise is the largest spectral component excluding the input signal and DC. This value is expressed in decibels relative to the RMS value of a full-scale input signal.

Full-Power and Full-Linear Bandwidth

The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full-scale input signal. The full-linear bandwidth is the input frequency at which the S/(N + D) has dropped to 77dB (12.5 effective bits). The LTC1416 has been designed to optimize input bandwidth, allowing the ADC to undersample input signals with frequencies above the converter's Nyquist frequency. The noise floor stays very low at high frequencies; S/(N + D) becomes dominated by distortion at frequencies far beyond Nyquist.

APPLICATIONS INFORMATION

Driving the Analog Input

The differential analog inputs of the LTC1416 are easy to drive. The inputs may be driven differentially or as a single-ended input (i.e., the A_{IN}^- input is grounded). The A_{IN}^+ and A_{IN}^- inputs are sampled at the same instant. Any unwanted signal that is common mode to both inputs will be reduced by the common mode rejection of the sample-and-hold circuit. The inputs draw only one small current spike while charging the sample-and-hold capacitors at the end of conversion. During conversion, the analog inputs draw only a small leakage current. If the source impedance of the driving circuit is low, then the LTC1416 inputs can be driven directly. As source impedance increases so will acquisition time (see Figure 6). For minimum acquisition time, with high source impedance, a buffer amplifier should be used. The only requirement is that the amplifier driving the analog input(s) must settle after the small current spike before the next conversion starts (settling time must be 400ns for full throughput rate).
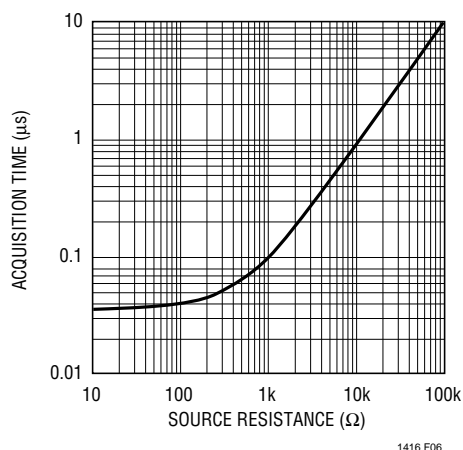

1416 F06

Figure 6. Acquisition Time vs Source Resistance

Choosing an Input Amplifier

Choosing an input amplifier is easy if a few requirements are taken into consideration. First, to limit the magnitude of the voltage spike seen by the amplifier from charging the sampling capacitor, choose an amplifier that has a low output impedance (<100Ω) at the closed-loop bandwidth

frequency. For example, if an amplifier is used in a gain of 1 and has a unity-gain bandwidth of 50MHz, then the output impedance at 50MHz should be less than 100Ω. The second requirement is that the closed-loop bandwidth must be greater than 10MHz to ensure adequate small-signal settling for full throughput rate. If slower op amps are used, more settling time can be provided by increasing the time between conversions.

The best choice for an op amp to drive LTC1416 will depend on the application. Generally, applications fall into two categories: AC applications where dynamic specifications are most critical and time domain applications where DC accuracy and settling time are most critical. The following list is a summary of the op amps that are suitable for driving the LTC1416. More detailed information is available in the Linear Technology Databooks and the LinearView™ CD-ROM.

LT®1220: 30MHz unity-gain bandwidth voltage feedback amplifier. ±5V to ±15V supplies, excellent DC specifications.

LT1223: 100MHz video current feedback amplifier. 6mA supply current, ±5V to ±15V supplies, low distortion at frequencies above 400kHz, low noise, good for AC applications.

LT1227: 140MHz video current feedback amplifier. 10mA supply current, ±5V to ±15V supplies, lowest distortion at frequencies above 400kHz, low noise, best for AC applications.

LT1229/LT1230: Dual and quad 100MHz current feedback amplifiers. ±2V to ±15V supplies, low noise, good AC specs, 6mA supply current each amplifier.

LT1360: 50MHz voltage feedback amplifier. 3.8mA supply current, good AC and DC specs, ±5V to ±15V supplies.

LT1363: 70MHz, 1000V/μs op amps. 6.3mA supply current, good AC and DC specs.

LT1364/LT1365: Dual and quad 70MHz, 100V/μs op amps. 6.3mA supply current per amplifier.

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Input Filtering

The noise and the distortion of the input amplifier and other circuitry must be considered since they will add to the LTC1416 noise and distortion. The small-signal bandwidth of the sample-and-hold circuit is 15MHz. Any noise or distortion products that are present at the analog inputs will be summed over this entire bandwidth. Noisy input circuitry should be filtered prior to the analog inputs to minimize noise. A simple 1-pole RC filter is sufficient for many applications. For example, Figure 7 shows a 1000pF capacitor from A_{IN}^+ to ground and a 200Ω source resistor to limit the input bandwidth to 800kHz. The 1000pF capacitor also acts as a charge reservoir for the input sample-and-hold and isolates the ADC input from sampling glitch sensitive circuitry. High quality capacitors and resistors should be used since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can also generate distortion from self-heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.
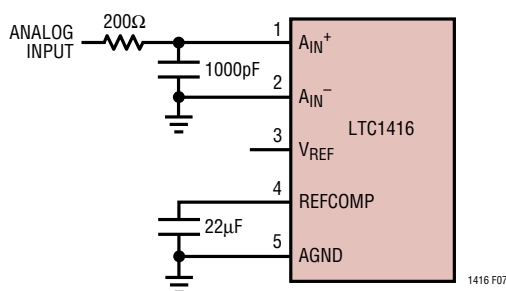

Figure 7. RC Input Filter

Input Range

The ±2.5V input range of the LTC1416 is optimized for low noise and low distortion. Most op amps also perform best over this same range, allowing direct coupling to the analog inputs and eliminating the need for special translation circuitry.

Some applications may require other input ranges. The LTC1416 differential inputs and reference circuitry can accommodate other input ranges often with little or no additional circuitry. The following sections describe the reference and input circuitry and how they affect the input range.

Internal Reference

The LTC1416 has an on-chip, temperature compensated, curvature corrected, bandgap reference that is factory trimmed to 2.500V. It is connected internally to a reference amplifier and is available at V_{REF} (Pin 3). See Figure 8a. A 4k resistor is in series with the output so that it can be easily overdriven by an external reference or other circuitry (see Figure 8b). The reference amplifier gains the voltage at the V_{REF} pin by 1.625 to create the required internal reference voltage. This provides buffering between the V_{REF} pin and the high speed capacitive DAC. The
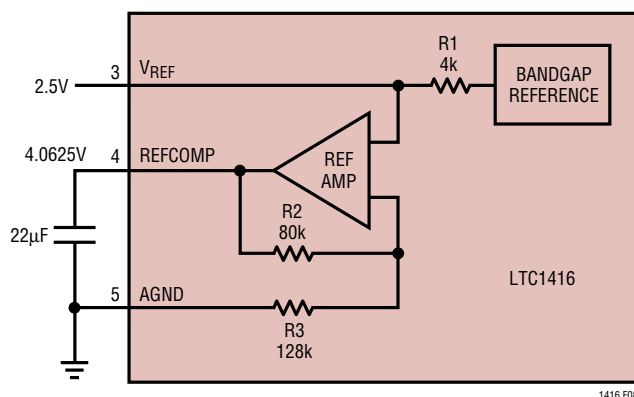

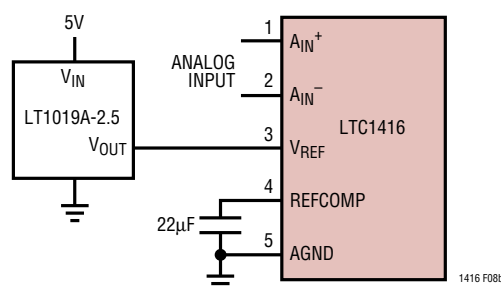**Figure 8a. LTC1416 Reference Circuit**

Figure 8b. Using the LT1019-2.5 as an External Reference

APPLICATIONS INFORMATION

reference amplifier compensation pin, REFCOMP (Pin 4), must be bypassed with a capacitor to ground. The reference amplifier is stable with capacitors of 1µF or greater. For the best noise performance, a 22µF ceramic or 22µF tantalum in parallel with a 0.1µF ceramic is recommended.

The V_{REF} pin can be driven with a DAC or other means shown in Figure 9. This is useful in applications where the peak input signal amplitude may vary. The input span of the ADC can then be adjusted to match the peak input signal, maximizing the signal-to-noise ratio. The filtering of the internal LTC1416 reference amplifier will limit the bandwidth and settling time of this circuit. A settling time of 5ms should be allowed for after a reference adjustment.

Figure 10a. CMRR vs Input Frequency

Figure 9. Driving V_{REF} with a DAC

Figure 10b. Selectable 0V to 5V or ±2.5V Input Range

Differential Inputs

The LTC1416 has a unique differential sample-and-hold circuit that allows rail-to-rail inputs. The ADC will always convert the difference of $A_{IN}^+ - A_{IN}^-$ independent of the common mode voltage. The common mode rejection holds up to extremely high frequencies (see Figure 10a). The only requirement is that both inputs cannot exceed the AV_{DD} or AV_{SS} power supply voltages. Integral nonlinearity errors (INL) and differential nonlinearity errors (DNL) are independent of the common mode voltage, however, the bipolar zero error (BZE) will vary. The change in BZE is typically less than 0.1% of the common mode voltage. Dynamic performance is also affected by the common mode voltage. THD will degrade as the inputs approach either power supply rail, from 90dB with a common mode of 0V to 79dB with a common mode of 2.5V or –2.5V.

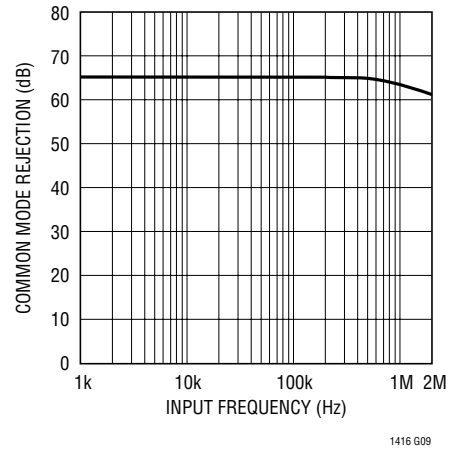Differential inputs allow greater flexibility for accepting different input ranges. Figure 10b shows a circuit that
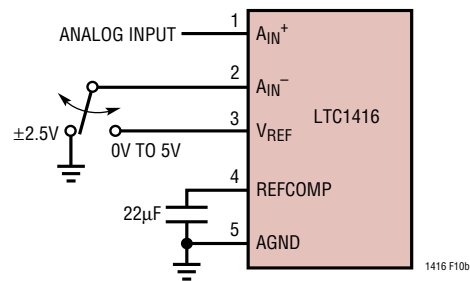
converts a 0V to 5V analog input signal with no additional translation circuitry.

Full-Scale and Offset Adjustment

Figure 11a shows the ideal input/output characteristics for the LTC1416. The code transitions occur midway between successive integer LSB values (i.e., –FS + 0.5LSB, –FS + 1.5LSB, –FS + 2.5LSB, . . . FS – 1.5LSB, FS – 0.5LSB). The output is two's complement binary with 1LSB = FS – (–FS)/16384 = 5V/16384 = 305.2µV.

In applications where absolute accuracy is important, offset and full-scale errors can be adjusted to zero. Offset error must be adjusted before full-scale error. Figure 11b shows the extra components required for full-scale error adjustment. Zero offset is achieved by adjusting the offset applied to the A_{IN}^- input. For zero offset error, apply –152µV (i.e., –0.5LSB) at A_{IN}^+ and adjust the offset at the A_{IN}^- input until the output code flickers between 0000

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0000 0000 00 and 1111 1111 1111 11. For full-scale adjustment, an input voltage of 2.499544V (FS/2 – 1.5LSB) is applied to A_{IN} and R2 is adjusted until the output code flickers between 0111 1111 1111 10 and 0111 1111 1111 11.
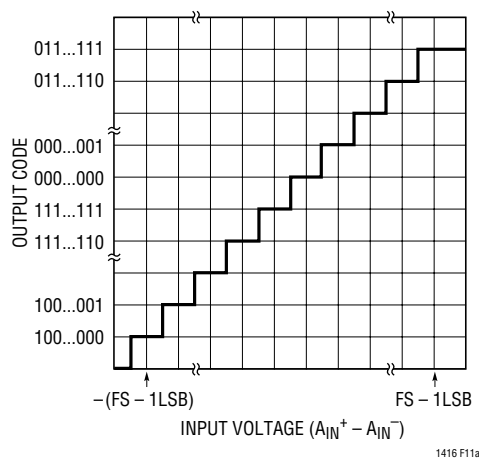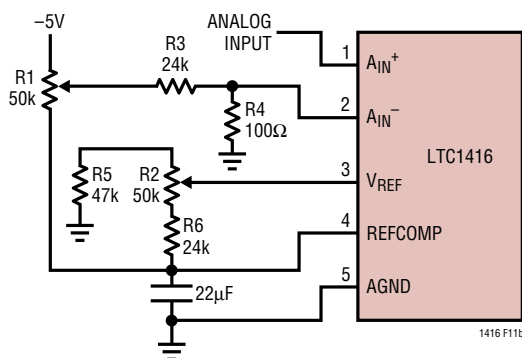

Figure 11a. LTC1416 Transfer Characteristics

Figure 11b. Offset and Full-Scale Adjust Circuit

Generating a –5V Supply

There are several advantages to using ±5V supplies rather than a single 5V supply. A larger signal magnitude is possible which increases the dynamic range and improves the signal-to-noise ratio. Operating on ±5V supplies also offers increased headroom which eases the requirements for signal conditioning circuitry, avoids the limitations of rail-to-rail operation and widens the selection of high performance operational amplifiers. Some

applications, however, do not have a –5V supply readily available and most ADCs have inadequate PSRR to sufficiently attenuate the noise created by a switching or charge pump supply. The LTC1416's excellent PSRR makes it possible to achieve good performance, even at 14 bits, using a switch based regulator for a –5V supply. Figure 12a shows a circuit using an LT1373 configured as a Cuk converter creating –5V from a 5V supply. The circuit shown in Figure 12b uses an LT1054 regulated charge pump to provide –5V. This circuit has the advantage of reduced board space and fewer passive components. (For further details refer to *Linear Technology* Magazine, June 1997, Page 29.)

BOARD LAYOUT AND BYPASSING

Wire wrap boards are not recommended for high resolution or high speed A/D converters. To obtain the best performance from the LTC1416, a printed circuit board with ground plane is required. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC. The analog input should be screened by AGND.

An analog ground plane separate from the logic system ground should be established under and around the ADC (see Figure 13). Pin 5 (AGND), Pins 14 and 19 (ADC's DGND) and all other analog grounds should be connected to this single analog ground point. The REFCOMP bypass capacitor and the DV_{DD} bypass capacitor should also be connected to this analog ground plane. No other digital grounds should be connected to this analog ground plane. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and the foil width for these tracks should be as wide as possible. In applications where the ADC data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get errors in the conversion results. These errors are due to feedthrough from the microprocessor to the successive approximation comparator. The problem can be eliminated by forcing the microprocessor into a Wait state during conversion or by using three-state buffers to isolate the ADC data bus. The
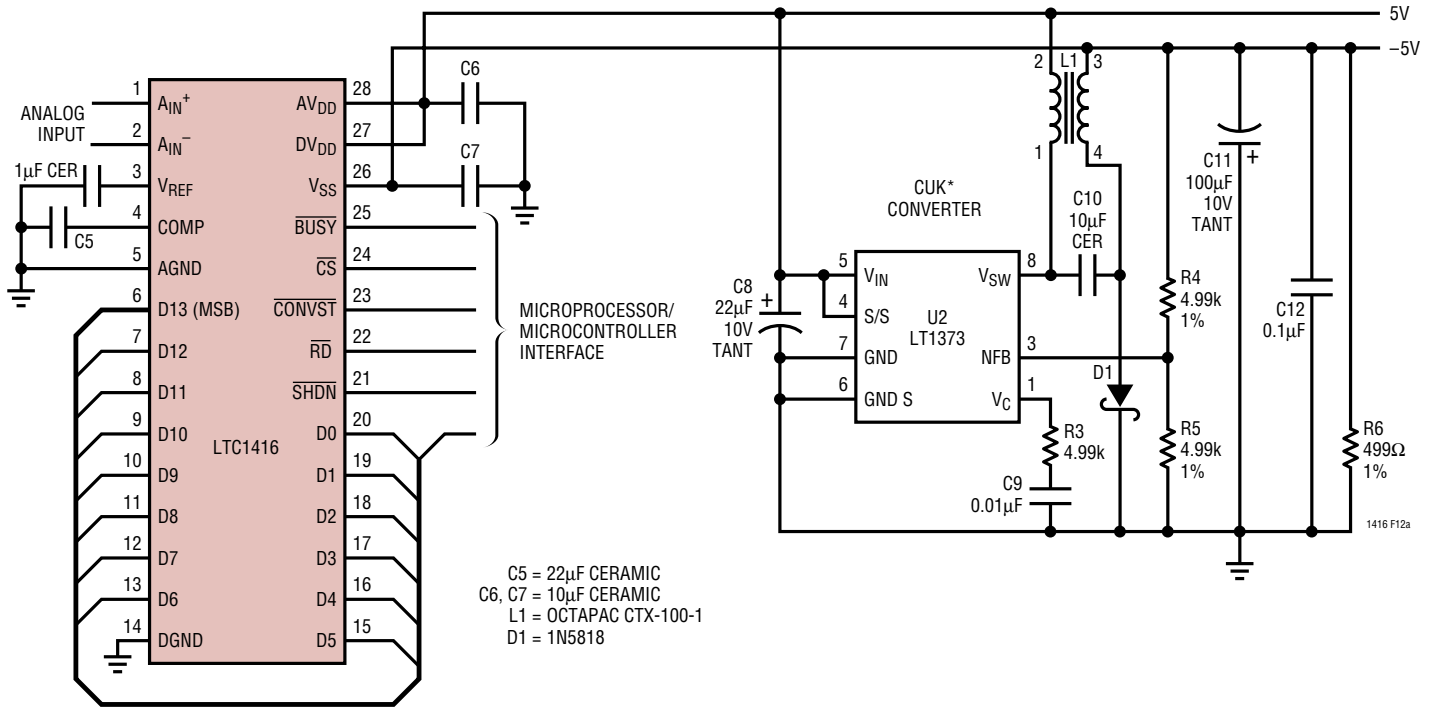
APPLICATIONS INFORMATION

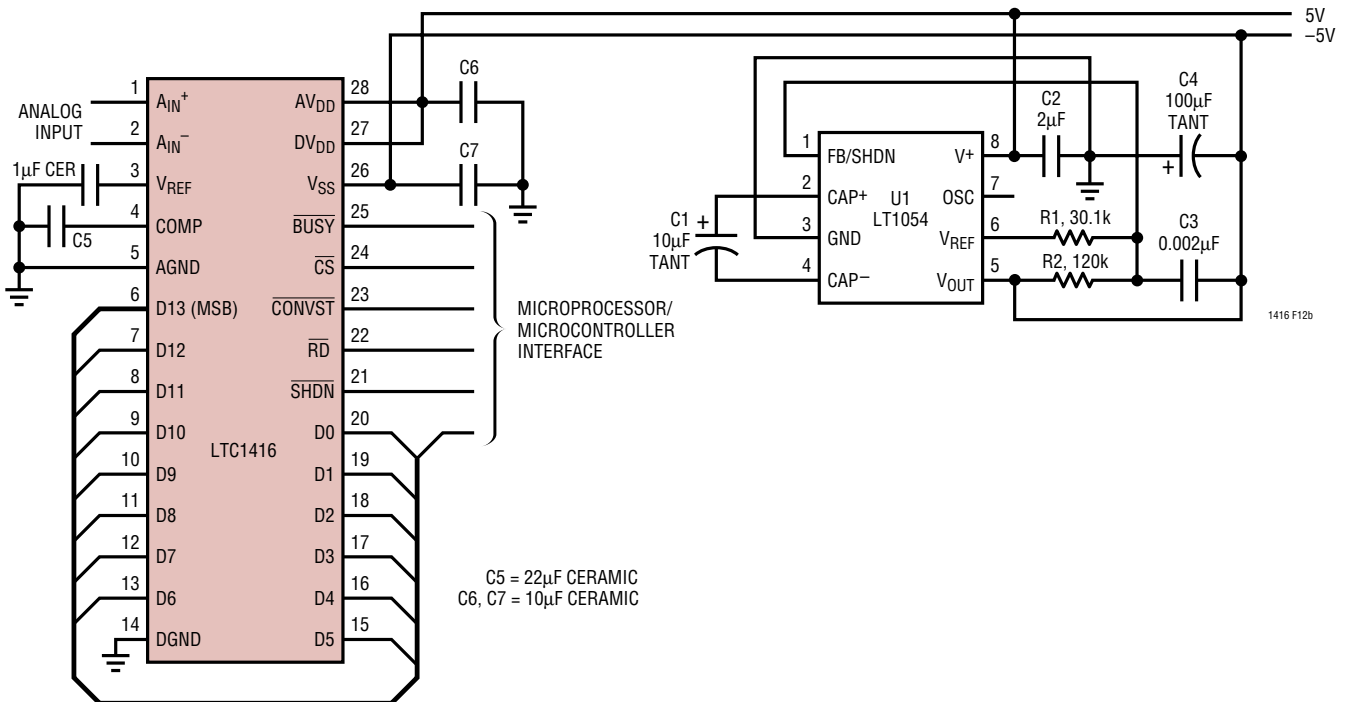**Figure 12a. Using the LT1373 to Generate a −5V Supply**

Figure 12b. Using the LT1054 to Generate a −5V Supply
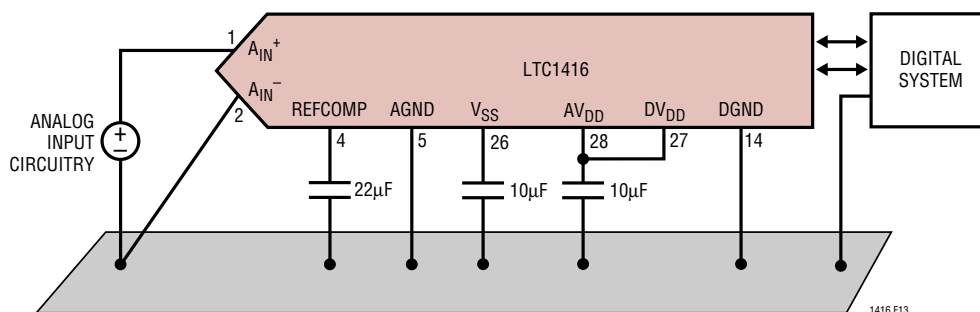
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Figure 13. Power Supply Grounding Practice.

traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

The LTC1416 has differential inputs to minimize noise coupling. Common mode noise on the A_{IN}^+ and A_{IN}^- leads will be rejected by the input CMRR. The A_{IN}^- input can be used as a ground sense for the A_{IN}^+ input; the LTC1416 will hold and convert the difference voltage between A_{IN}^+ and A_{IN}^-. The leads to A_{IN}^+ (Pin 1) and A_{IN}^- (Pin 2) should be kept as short as possible. In applications where this is not possible, the A_{IN}^+ and A_{IN}^- traces should be run side by side to equalize coupling.

Supply Bypassing

High quality, low series resistance ceramic, bypass capacitors should be used at the V_{DD} (10μF) and REFCOMP (22μF) pins as shown in the Typical Application on the first page of this data sheet. Surface mount ceramic capacitors such as Murata GRM235Y5V106Z016 provide excellent bypassing in a small board space. Alternatively tantalum capacitors in parallel with 0.1μF ceramic capacitors can be used. Bypass capacitors must be located as close to the pins as possible. The traces connecting the pins and the bypass capacitors must be kept short and should be made as wide as possible.

Example Layout

Figures 14a, 14b, 14c and 14d show the schematic and layout of an evaluation board. The layout demonstrates the proper use of decoupling capacitors and ground plane with a 2-layer printed circuit board.

DIGITAL INTERFACE

The A/D converter is designed to interface with microprocessors as a memory mapped device. The $\overline{CS}$ and $\overline{RD}$ control inputs are common to all peripheral memory interfacing. A separate $\overline{CONVST}$ is used to initiate a conversion.

Internal Clock

The A/D converter has an internal clock that eliminates the need for synchronization between the external clock and the $\overline{CS}$ and $\overline{RD}$ signals found in other ADCs. The internal clock is factory trimmed to achieve a typical conversion time of 1.8μs, and a maximum conversion time over the full operating temperature range of 2.2μs. No external adjustments are required. The guaranteed maximum acquisition time is 400ns. In addition, a throughput time of 2.5μs and a minimum sampling rate of 400ksps is guaranteed.

Power Shutdown

The LTC1416 provides two power shutdown modes—nap mode and sleep mode to save power during inactive periods. The nap mode reduces the power by 95% and leaves only the digital logic and reference powered up. The wake-up time from nap to active is 400ns. In sleep mode, the reference is shut down and only a small current of 120μA remains. Wake-up time from sleep mode is much slower since the reference circuit must power up and settle to 0.005% for full 14-bit accuracy. Sleep mode wake-up time is dependent on the value of the capacitor connected to the REFCOMP (Pin 4). The wake-up time is 20ms with the recommended 22μF capacitor.

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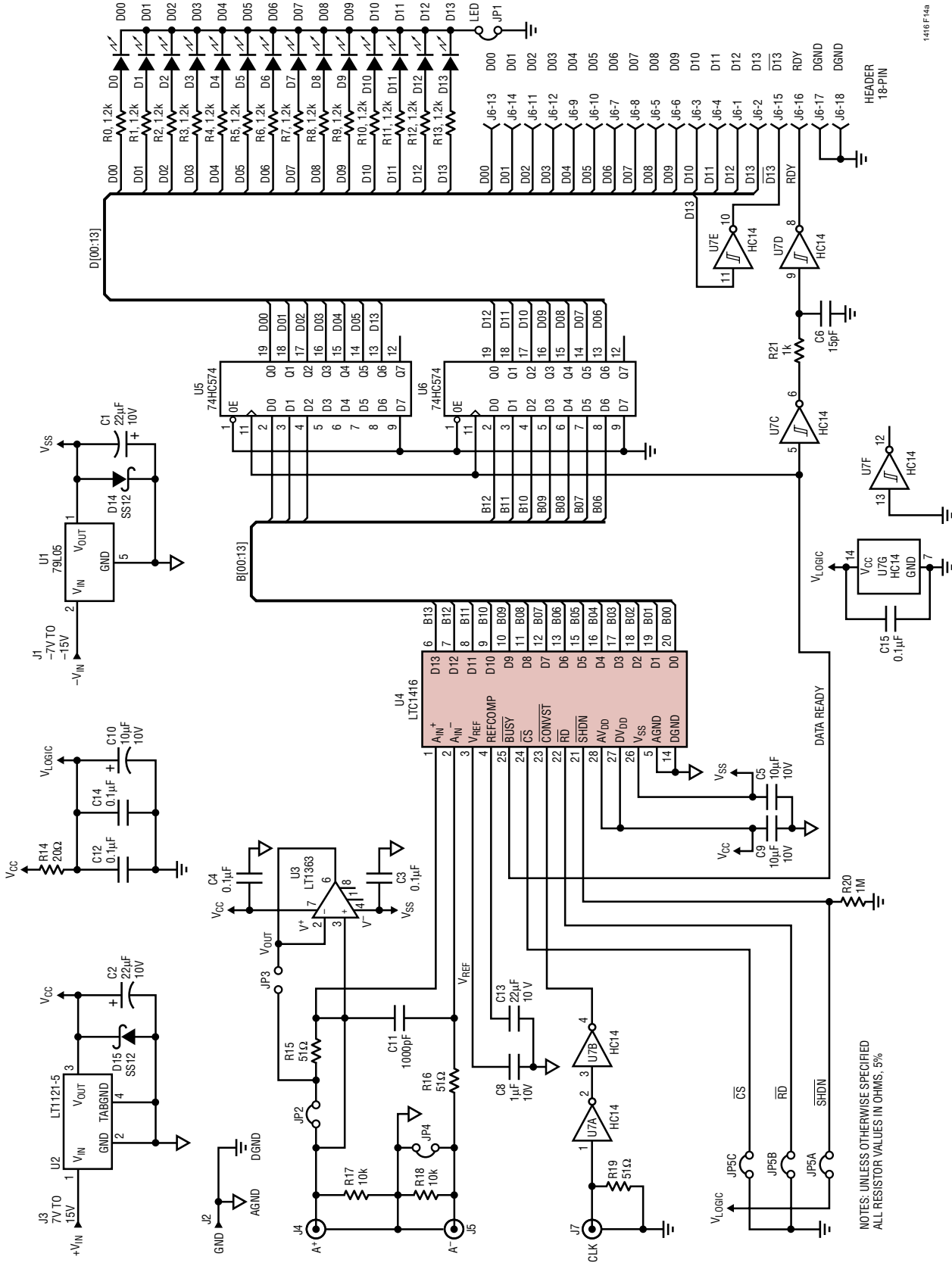
Figure 14a. Suggested Evaluation Circuit Schematic
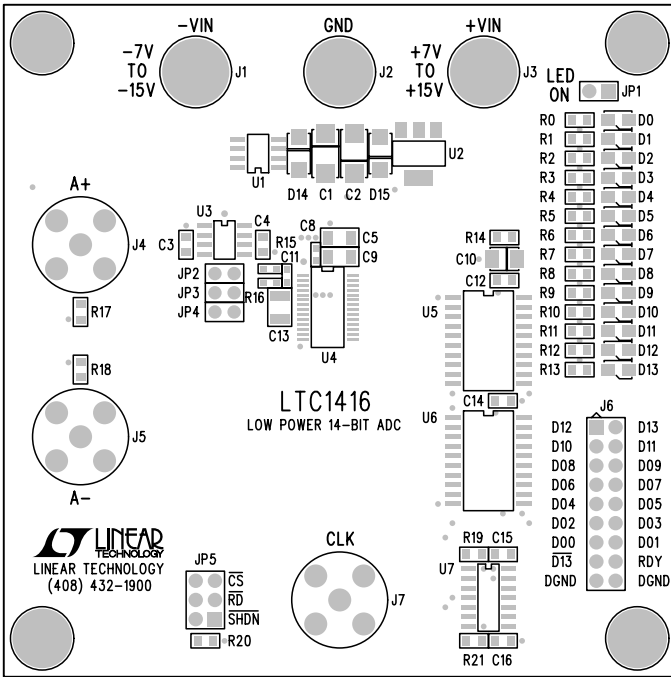
APPLICATIONS INFORMATION

Figure 14b. Suggested Evaluation Circuit Board—
Component Side Silkscreen
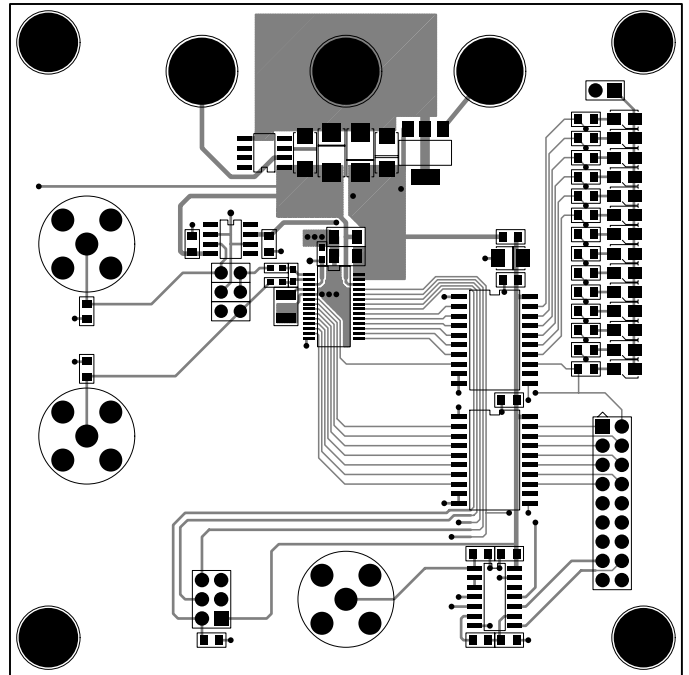

Figure 14c. Suggested Evaluation Circuit Board—
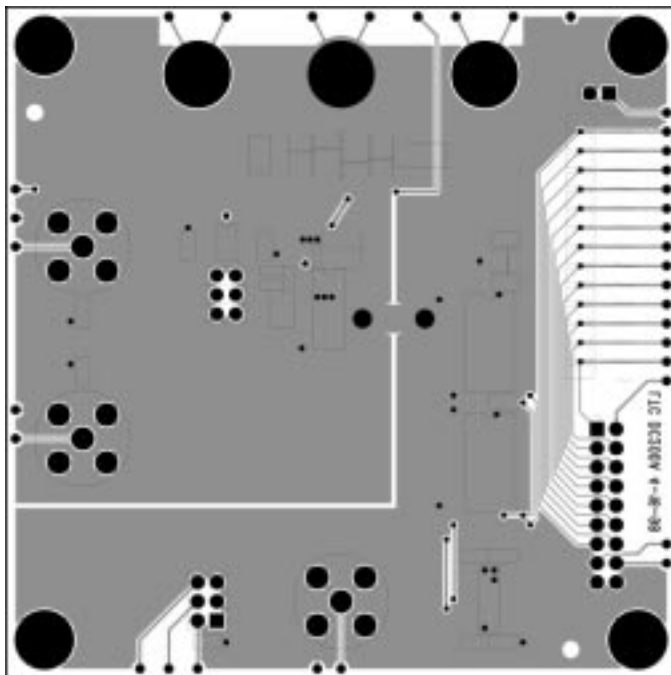Component Side Layout

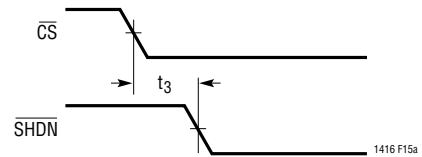Figure 14d. Suggested Evaluation Circuit Board—
Solder Side Layout

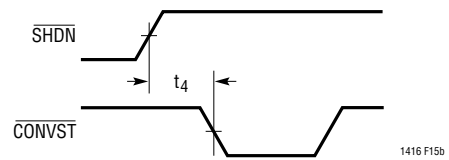
Figure 15a. $\overline{CS}$ to $\overline{SHDN}$ Timing

Figure 15b. $\overline{SHDN}$ to $\overline{CONVST}$ Wake-Up Timing

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Shutdown is controlled by Pin 21 ($\overline{\text{SHDN}}$), the ADC is in shutdown when it is low. The shutdown mode is selected with Pin 20 ($\overline{\text{CS}}$), low selects nap.

Timing and Control

Conversion start and data read operations are controlled by three digital inputs: $\overline{\text{CONVST}}$, $\overline{\text{CS}}$ and $\overline{\text{RD}}$. A logic "0" applied to the $\overline{\text{CONVST}}$ pin will start a conversion after the ADC has been selected (i.e., $\overline{\text{CS}}$ is low). Once initiated, it cannot be restarted until the conversion is complete. Converter status is indicated by the $\overline{\text{BUSY}}$ output. $\overline{\text{BUSY}}$ is low during a conversion.

Figures 16 through 21 show several different modes of operation. In modes 1a and 1b (Figures 17 and 18), $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are both tied low. The falling edge of $\overline{\text{CONVST}}$ starts the conversion. The data outputs are always enabled and data can be latched with the $\overline{\text{BUSY}}$ rising edge. Mode 1a shows operation with a narrow logic low $\overline{\text{CONVST}}$ pulse. Mode 1b shows a narrow logic high $\overline{\text{CONVST}}$ pulse.

In mode 2 (Figure 19), $\overline{\text{CS}}$ is tied low. The falling edge of $\overline{\text{CONVST}}$ signal again starts the conversion. Data outputs are in three-state until read by the MPU with the $\overline{\text{RD}}$ signal. Mode 2 can be used for operation with a shared MPU data bus.

In slow memory and ROM modes (Figures 20 and 21), $\overline{\text{CS}}$ is tied low and $\overline{\text{CONVST}}$ and $\overline{\text{RD}}$ are tied together. The MPU starts the conversion and reads the output with the $\overline{\text{RD}}$ signal. Conversions are started by the MPU or DSP (no external sample clock).

In slow memory mode, the processor applies a logic low to $\overline{\text{RD}}$ (= $\overline{\text{CONVST}}$), starting the conversion. $\overline{\text{BUSY}}$ goes low, forcing the processor into a Wait state. The previous conversion result appears on the data outputs. When the conversion is complete, the new conversion results appear on the data outputs; $\overline{\text{BUSY}}$ goes high releasing the processor, and the processor takes $\overline{\text{RD}}$ (= $\overline{\text{CONVST}}$) back high and reads the new conversion data.

In ROM mode, the processor takes $\overline{\text{RD}}$ (= $\overline{\text{CONVST}}$) low, starting a conversion and reading the previous conversion result. After the conversion is complete, the processor can read the new result and initiate another conversion.
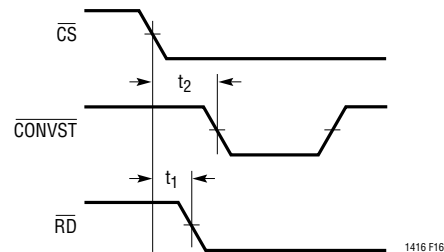

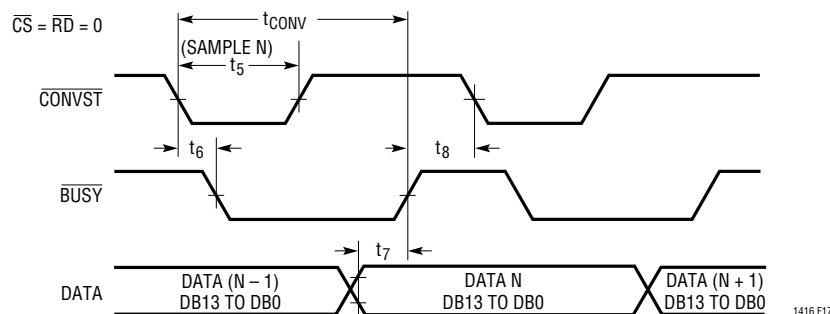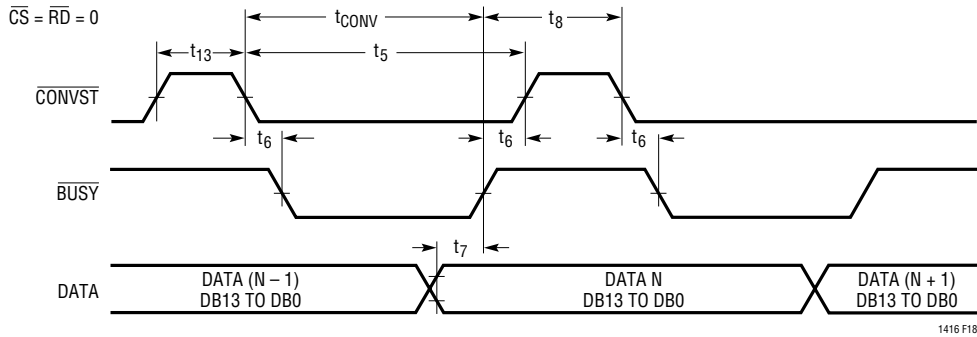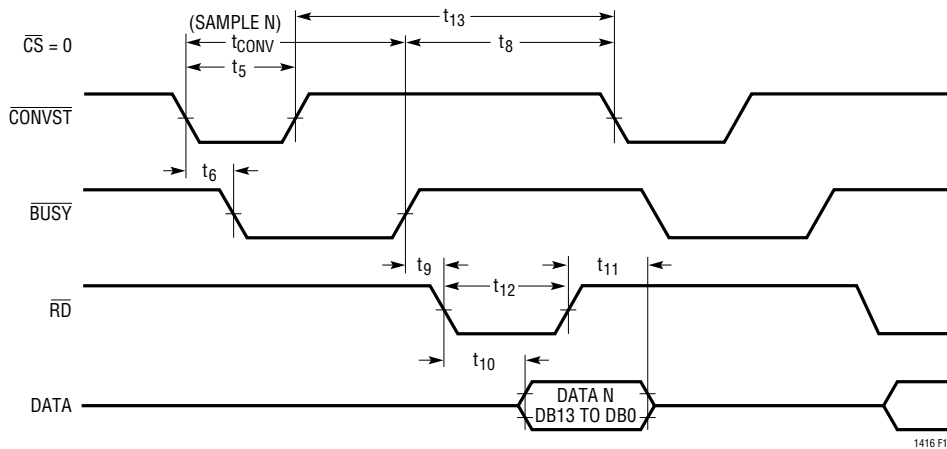**Figure 16. $\overline{\text{CS}}$ to $\overline{\text{CONVST}}$ Setup Timing**

Figure 17. Mode 1a. $\overline{\text{CONVST}}$ Starts a Conversion. Data Outputs Always Enabled
($\overline{\text{CONVST}}$ = ⎴⎵⎴⎵⎴)

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$\overline{CS} = \overline{RD} = 0$

$\overline{CONVST}$

$\overline{BUSY}$

DATA

t_{13} t_{CONV} t_5 t_8 t_6 t_6 t_6 t_7

DATA (N − 1) DB13 TO DB0

DATA N DB13 TO DB0

DATA (N + 1) DB13 TO DB0

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Figure 18. Mode 1b. $\overline{CONVST}$ Starts a Conversion. Data Outputs Always Enabled ($\overline{CONVST}$ = ⎍⎍)

$\overline{CS} = 0$

$\overline{CONVST}$

$\overline{BUSY}$

$\overline{RD}$

DATA

(SAMPLE N) t_{CONV} t_5 t_{13} t_8 t_6 t_9 t_{12} t_{11} t_{10}

DATA N DB13 TO DB0

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Figure 19. Mode 2. $\overline{CONVST}$ Starts a Conversion. Data Is Read by $\overline{RD}$

$\overline{CS} = 0$

$\overline{RD} = \overline{CONVST}$

$\overline{BUSY}$

DATA

t_{CONV} t_8 (SAMPLE N) t_6 t_{11} t_{10} t_7

DATA (N − 1) DB13 TO DB0

DATA N DB13 TO DB0

DATA N DB13 TO DB0

DATA (N + 1) DB13 TO DB0
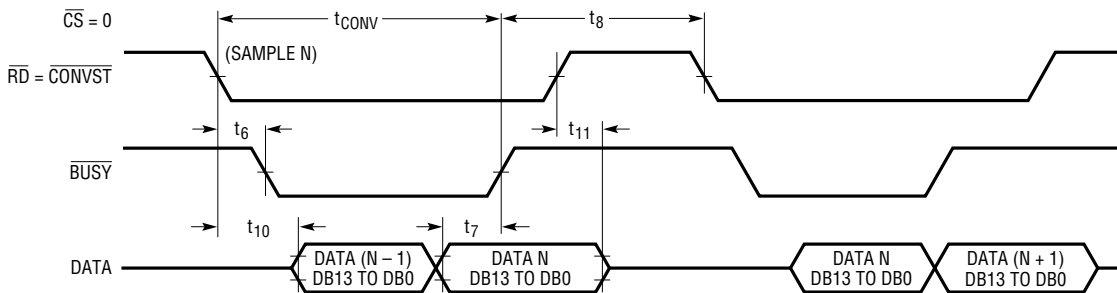
1416 F20

Figure 20. Slow Memory Mode Timing
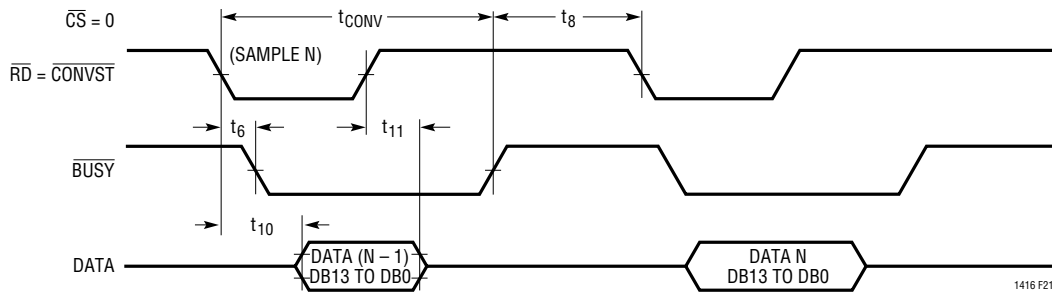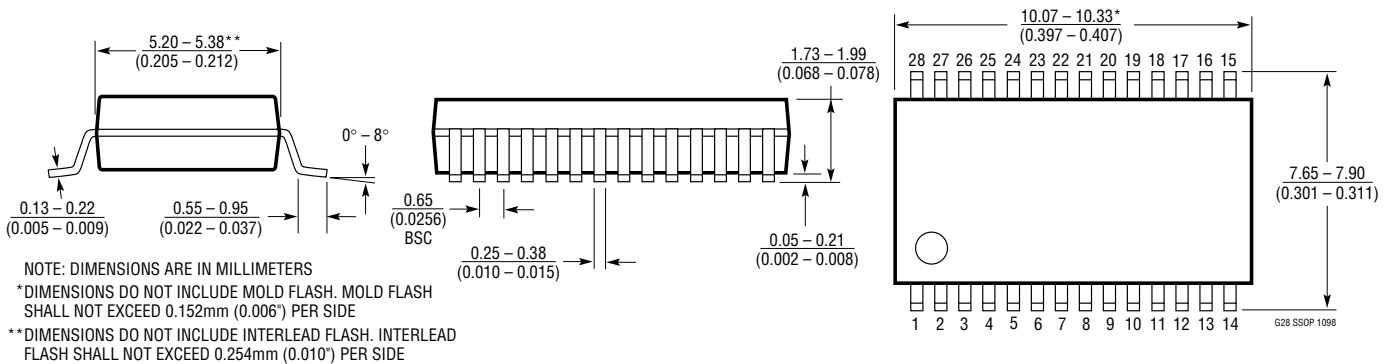
LTC1416

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Figure 21. ROM Mode Timing

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

G Package
28-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)

NOTE: DIMENSIONS ARE IN MILLIMETERS
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH
  SHALL NOT EXCEED 0.152mm (0.006") PER SIDE
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD
   FLASH SHALL NOT EXCEED 0.254mm (0.010") PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1278/LTC1279	Single Supply, 12-Bit, 500ksps/600ksps ADCs	Low Power, 5V or ±5V Supply
LTC1400	High Speed Serial 12-Bit ADC	400ksps, Complete with V_{REF}, CLK, Sample-and-Hold in SO-8
LTC1409/LTC1410	12-Bit, 800ksps/1.25Msps Sampling ADCs with Shutdown	Best Dynamic Performance, THD = 84dB and SINAD = 71dB at Nyquist
LTC1412	12-Bit, 3Msps Sampling ADC	Best Dynamic Performance, SINAD = 72dB at Nyquist
LTC1415	Single 5V, 12-Bit, 1.25Msps ADC	Single Supply, 55mW Dissipation
LTC1418	14-Bit, 200ksps Sampling ADC	16mW Dissipation, Serial and Parallel Outputs
LTC1419	14-Bit, 800ksps Sampling ADC with Shutdown	81.5dB SINAD, 150mW from ±5V Supplies
LTC1604	16-Bit, 333ksps Sampling ADC	±2.5V Input, SINAD = 90dB, THD = 100dB
LTC1605	Single 5V, 16-Bit, 100ksps ADC	Low Power, ±10V Inputs
LTC1606	16-Bit, 250ksps ADC	±10V Inputs, Pin Compatible with the LTC1605
LTC1608	16-Bit, 500ksps ADC	16-Bit, No Missing Codes, Pin Compatible with the LTC1604

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408)432-1900 • FAX: (408) 434-0507 • www.linear-tech.com

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