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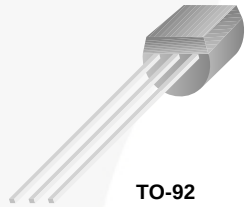
September 2014

MPSA06 / MMBTA06 / PZTA06
NPN General-Purpose Amplifier

Features

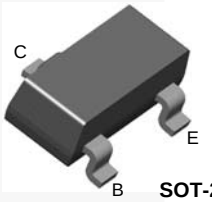
- This device is designed for general-purpose amplifier applications at collector currents to 300 mA.
- Sourced from process 12.

MPSA06



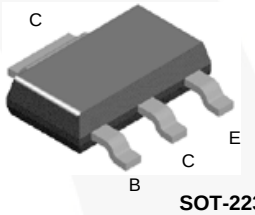
TO-92

MMBTA06



SOT-23
Mark: 1G

PZTA06



SOT-223

Ordering Information

Part Number	Top Mark	Package	Packing Method
MPSA06	MPSA06	TO-92 3L	Bulk
MMBTA06	1G	SOT-23 3L	Tape and Reel
PZTA06	A06	SOT-223 4L	Tape and Reel

Absolute Maximum Ratings(1), (2)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Value	Unit
V_{CEO}	Collector-Emitter Voltage	80	V
V_{CBO}	Collector-Base Voltage	80	V
V_{EBO}	Emitter-Base Voltage	4.0	V
I_C	Collector Current - Continuous	500	mA
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Notes:

1. These ratings are based on a maximum junction temperature of 150°C.
2. These are steady-state limits. Fairchild Semiconductor should be consulted on applications involving pulsed or low-duty-cycle operations.

Thermal Characteristics

Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Max.			Unit
		MPSA06	MMBTA06[3]	PZTA06[4]	
P_D	Total Device Dissipation	625	350	1000	mW
	Derate Above 25°C	5.0	2.8	8.0	mW/°C
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	83.3			°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	200	357	125	°C/W

Notes:

3. Device is mounted on FR-4 PCB 1.6 inch x 1.6 inch x 0.06 inch.

4. Device is mounted on FR-4 PCB 36 mm x 18 mm x 1.5 mm, mounting pad for the collector lead minimum 6 cm^2.

Electrical Characteristics

Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Max.	Unit
Off Characteristics					
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage[5]	I_C = 1.0 mA, I_B = 0	80		V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 100 µA, I_C = 0	4.0		V
I_{CEO}	Collector Cut-Off Current	V_{CE} = 60 V, I_B = 0		0.1	µA
I_{CBO}	Collector Cut-Off Current	V_{CB} = 80 V, I_E = 0		0.1	µA
On Characteristics					
h_{FE}	DC Current Gain	I_C = 10 mA, V_{CE} = 1.0 V	100		
		I_C = 100 mA, V_{CE} = 1.0 V	100		
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_C = 100 mA, I_B = 10 mA		0.25	V
$V_{BE(on)}$	Base-Emitter On Voltage	I_C = 100 mA, V_{CE} = 1.0 V		1.2	V
Small Signal Characteristics					
f_T	Current Gain - Bandwidth Product	I_C = 10 mA, V_{CE} = 2.0 V, f = 100 MHz	100		MHz

Notes:

5. Pulse test: pulse width ≤ 300 µs, duty cycle ≤ 2%.

Typical Performance Characteristics

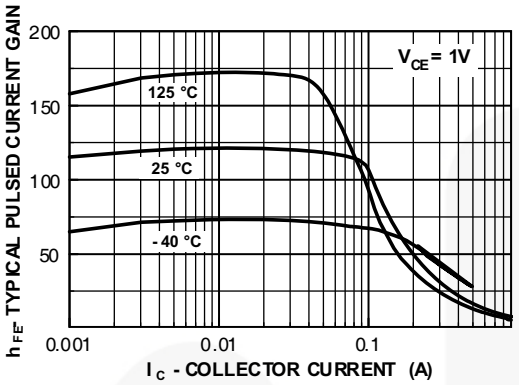


Figure 1. Typical Pulsed Current Gain vs. Collector Current

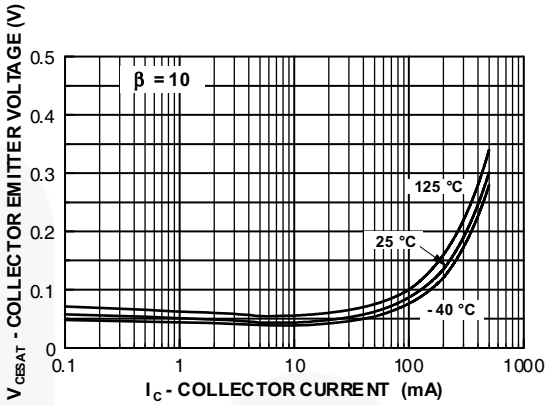


Figure 2. Collector-Emitter Saturation Voltage vs. Collector Current

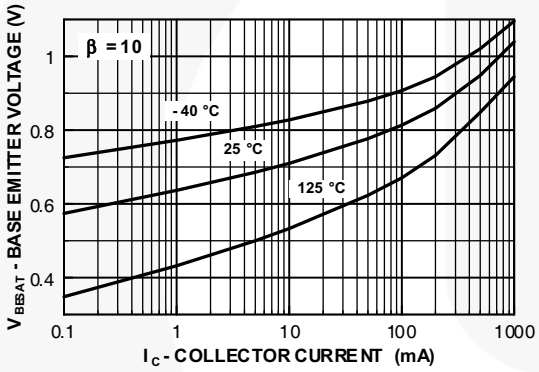


Figure 3. Base-Emitter Saturation Voltage vs. Collector Current

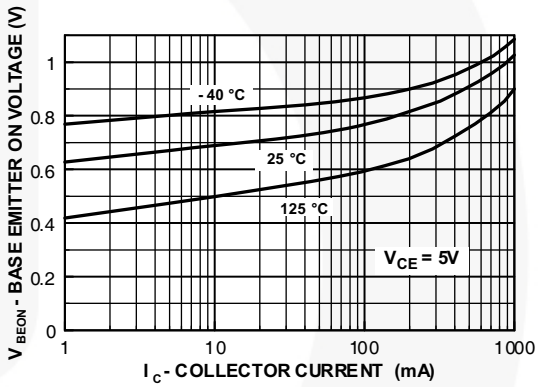


Figure 4. Base-Emitter On Voltage vs. Collector Current

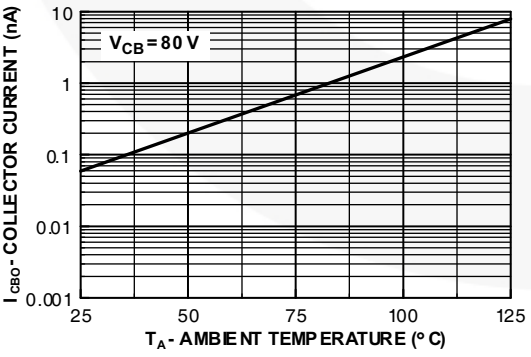


Figure 5. Collector Cut-Off Current vs. Ambient Temperature

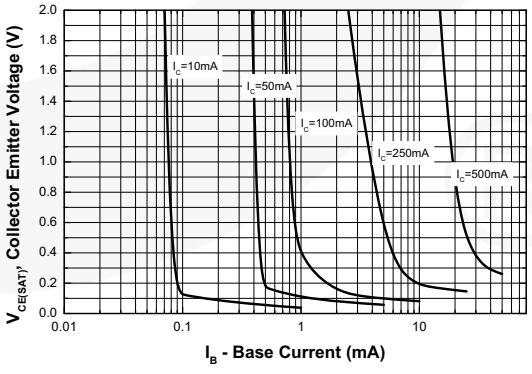


Figure 6. Collector Saturation Region

Typical Performance Characteristics (Continued)

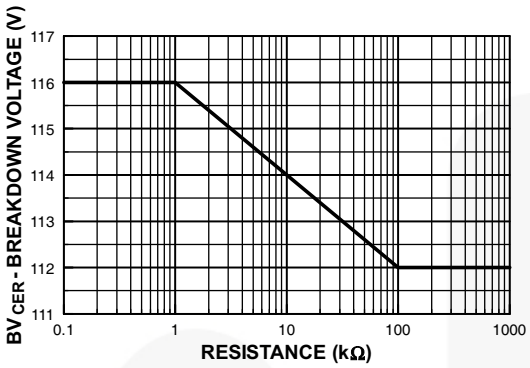


Figure 7. Collector-Emitter Breakdown Voltage with Resistance Between Emitter-Base

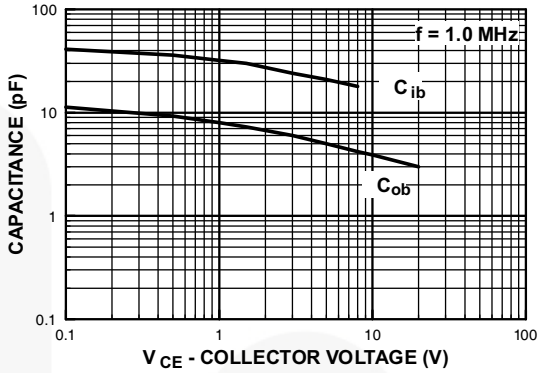


Figure 8. Input and Output Capacitance vs. Reverse Current

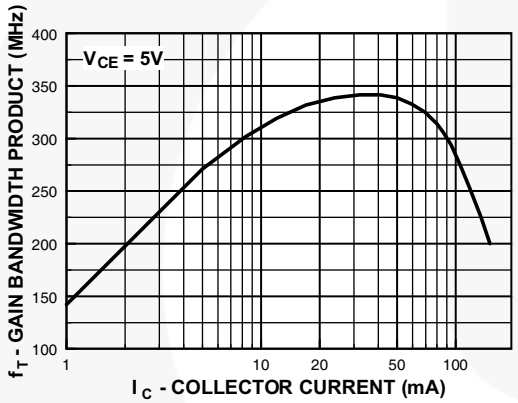


Figure 9. Gain Bandwidth Product vs. Collector Current

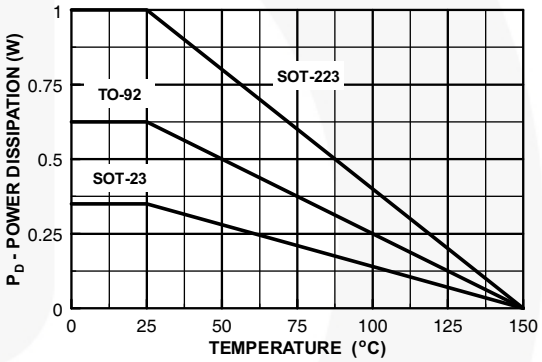
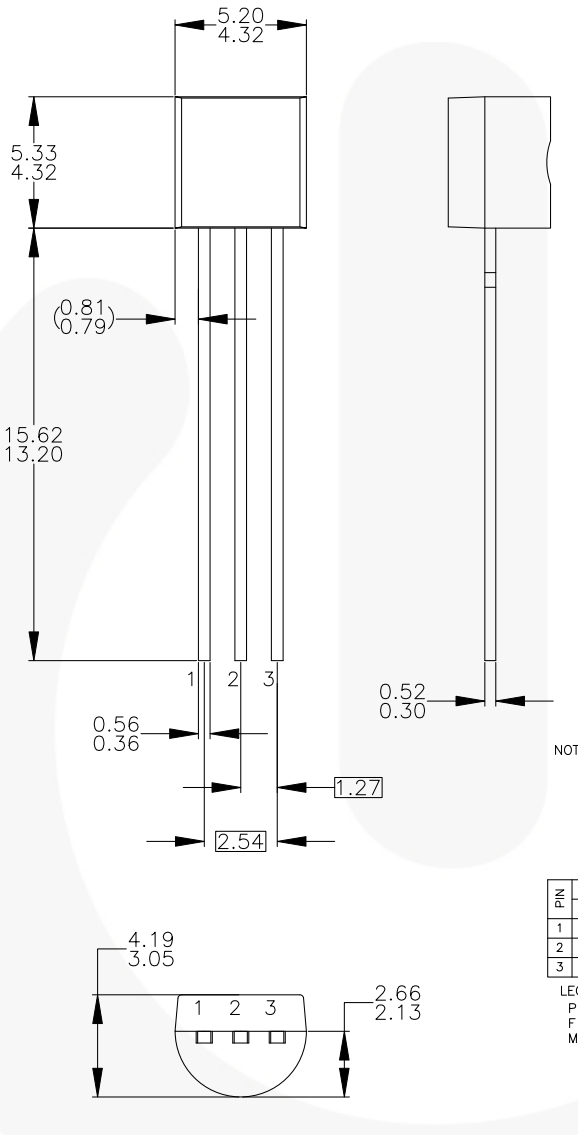


Figure 10. Power Dissipation vs. Ambient Temperature

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

A) DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DRAWING CONFORMS TO ASME Y14.5M-1994.
D) TO-92 (92,94,96,97,98) PIN CONFIGURATION:

PIN	92			94			96			97			98		
	P	F	M	P	F	M	B	F	M	P	F	M	P	F	M
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G

LEGEND:
P – BIPOLAR
F – JFET
M – DMOS
E – EMITTER
B – BASE
C – COLLECTOR
D – DRAIN
S – SOURCE
G – GATE

E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEAGLE AT JFET "F" OPTION.
F) DRAWING FILENAME: MKT-ZA03DREV3.

Figure 11. 3-LEAD, TO-92, MOLDED, STD STRAIGHT LEAD (NO EOL CODE)

Physical Dimensions (Continued)

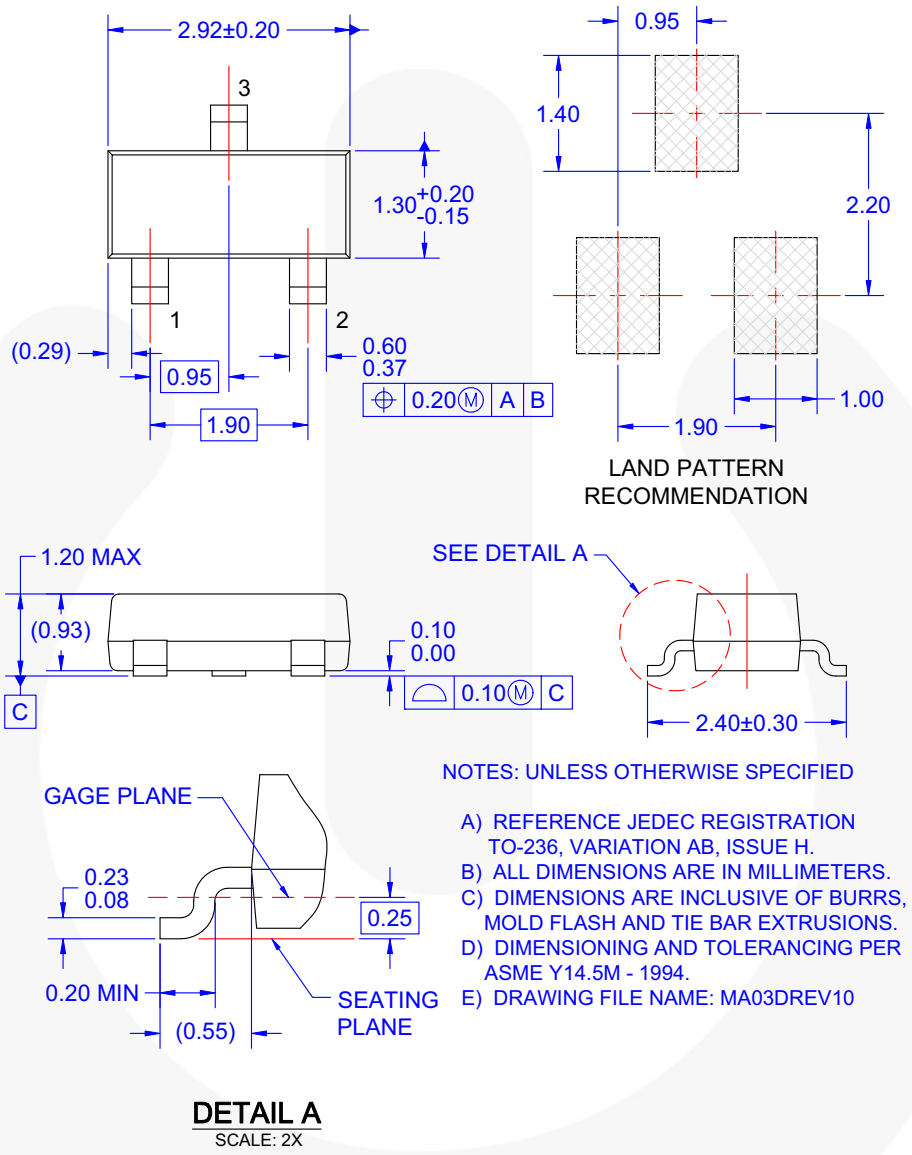


Figure 12. 3-LEAD, SOT23, JEDEC TO-236, LOW PROFILE

Physical Dimensions (Continued)

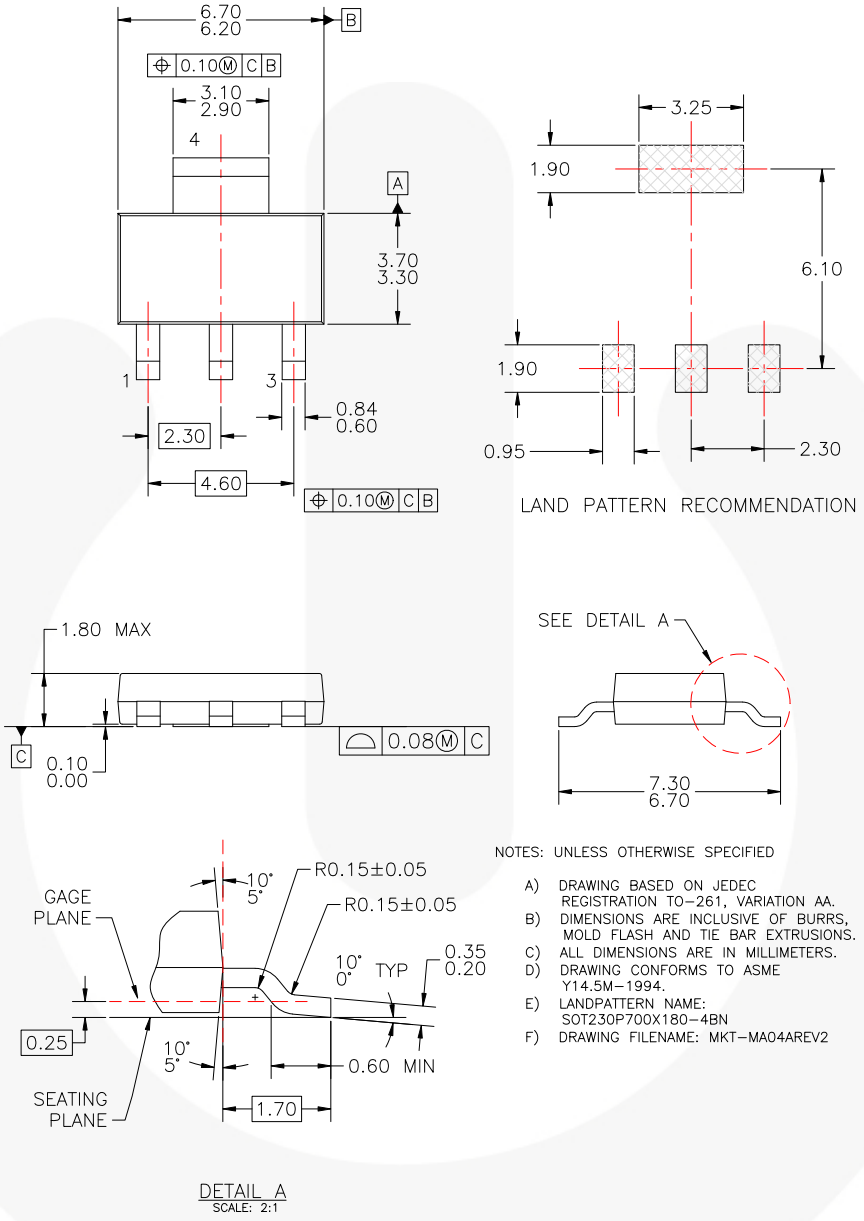


Figure 13. MOLDED PACKAGING, SOT-223, 4-LEAD

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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