P-Channel 40 V (D-S) 175 °C MOSFET

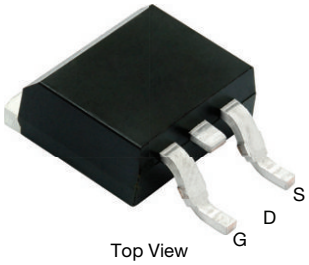
PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) [d]
-40	0.0042 at V_{GS} = -10 V	-110
	0.0062 at V_{GS} = -4.5 V	-110

FEATURES

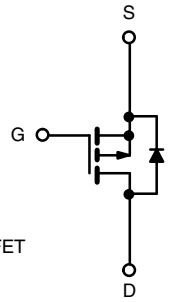
- TrenchFET® Power MOSFET
- Low thermal resistance
- Material categorization:
  For definitions of compliance please see
  www.vishay.com/doc?99912

RoHS COMPLIANT

TO-263



Top View



P-Channel MOSFET

Ordering Information:
SUM110P04-04L-E3 (Lead (Pb)-free)

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage		V_{DS}	-40	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 175 °C) [d]	T_C = 25 °C	I_D	-110	A
	T_C = 125 °C		-110	
Pulsed Drain Current		I_{DM}	-240	
Avalanche Current	L = 0.1 mH	I_{AS}	-75	
Single Pulse Avalanche Energy [a]		E_{AS}	281	mJ
Power Dissipation	T_C = 25 °C	P_D	375 [c]	W
	T_A = 25 °C [b]		3.75	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 175	°C

THERMAL RESISTANCE RATINGS			
PARAMETER	**SYMBOL**	**LIMIT**	**UNIT**
Junction-to-Ambient PCB Mount [b]	R_{thJA}	40	°C/W
Junction-to-Case	R_{thJC}	0.4	

Notes

a. Duty cycle ≤ 1 %.
b. When mounted on 1" square PCB (FR-4 material).
c. See SOA curve for voltage derating.
d. Limited by package.

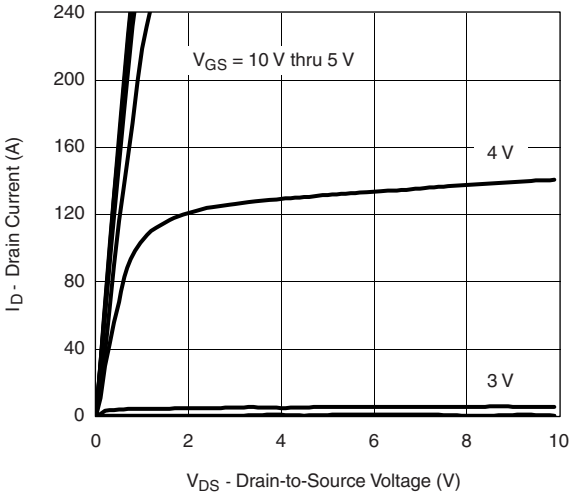
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = -250 µA	-40			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 µA	-1		-3	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -40 V, V_{GS} = 0 V			-1	µA
		V_{DS} = -40 V, V_{GS} = 0 V, T_J = 125 °C			-50	
		V_{DS} = -40 V, V_{GS} = 0 V, T_J = 175 °C			-250	
On-State Drain Current [a]	$I_{D(on)}$	V_{DS} = -5 V, V_{GS} = -10 V	-120			A
Drain-Source On-State Resistance [a]	$R_{DS(on)}$	V_{GS} = -10 V, I_D = -30 A		0.0034	0.0042	Ω
		V_{GS} = -10 V, I_D = -30 A, T_J = 125 °C			0.0063	
		V_{GS} = -10 V, I_D = -30 A, T_J = 175 °C			0.0076	
		V_{GS} = -4.5 V, I_D = -20 A		0.005	0.0062	
Forward Transconductance [a]	g_{fs}	V_{DS} = -15 V, I_D = -30 A	20			S
Dynamic [b]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = -25 V, f = 1 MHz		11 200		pF
Output Capacitance	C_{oss}			1650		
Reverse Transfer Capacitance	C_{rss}			1200		
Total Gate Charge [c]	Q_g	V_{DS} = -20 V, V_{GS} = -10 V, I_D = -110 A		235	350	nC
Gate-Source Charge [c]	Q_{gs}			45		
Gate-Drain Charge [c]	Q_{gd}			65		
Gate Resistance	R_g			3		Ω
Turn-On Delay Time [c]	$t_{d(on)}$	V_{DD} = -20 V, R_L = 0.18 Ω $I_D \cong$ -110 A, V_{GEN} = -10 V, R_g = 2.5 Ω		25	40	ns
Rise Time [c]	t_r			30	45	
Turn-Off Delay Time [c]	$t_{d(off)}$			190	300	
Fall Time [c]	t_f			110	165	
Source-Drain Diode Ratings and Characteristics (T_C = 25 °C) [b]						
Continuous Current	I_S				-110	A
Pulsed Current	I_{SM}				-240	
Forward Voltage [a]	V_{SD}	I_F = -85 A, V_{GS} = 0 V		-1	-1.5	V
Reverse Recovery Time	t_{rr}	I_F = -85 A, dI/dt = 100 A/µs		65	100	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			-3.7	-5.6	A
Reverse Recovery Charge	Q_{rr}			0.12	0.28	µC

Notes

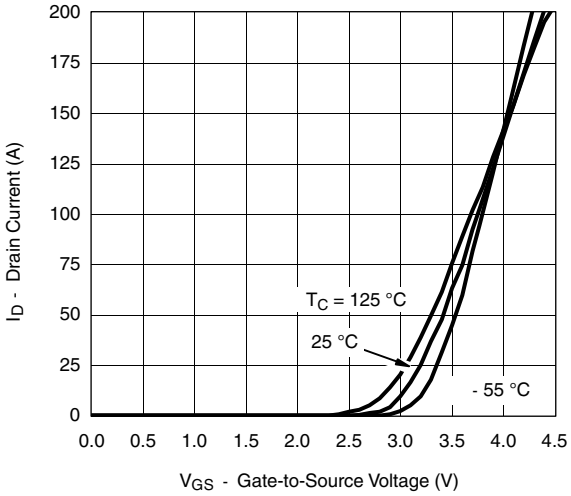
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

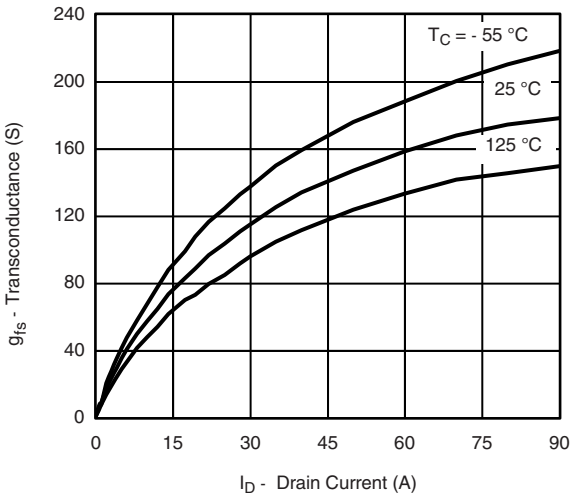
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



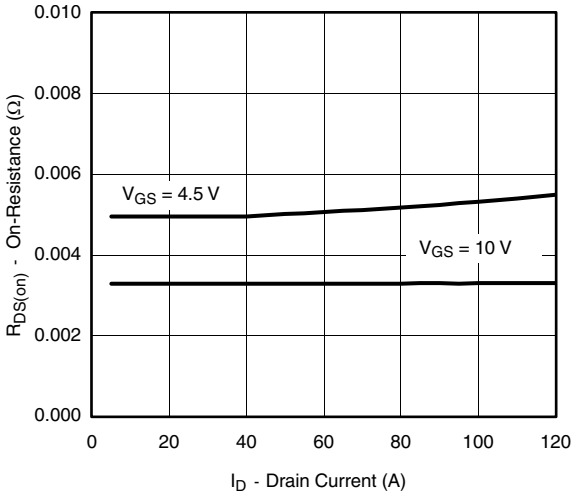
Output Characteristics



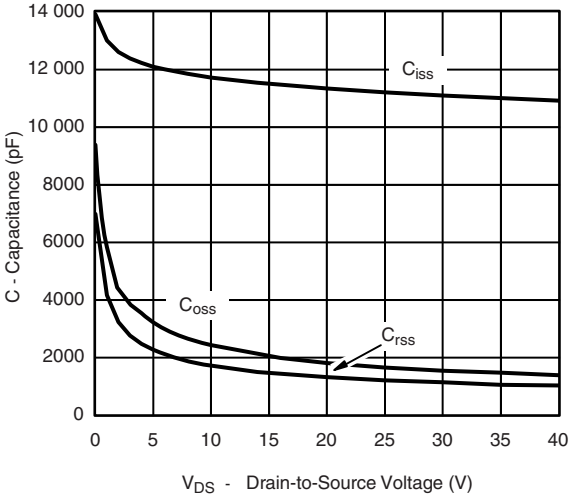
Transfer Characteristics



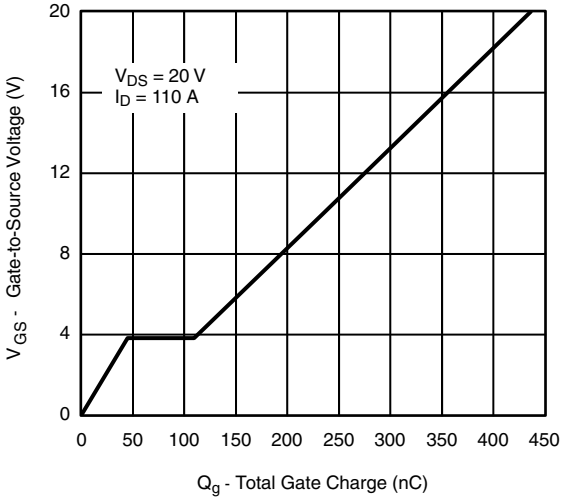
Transconductance



On-Resistance vs. Drain Current

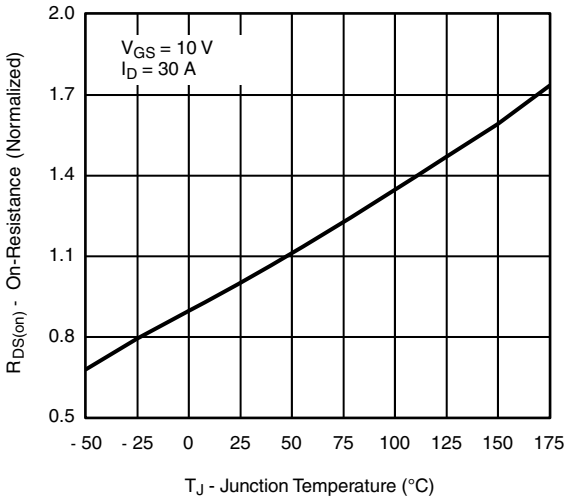


Capacitance

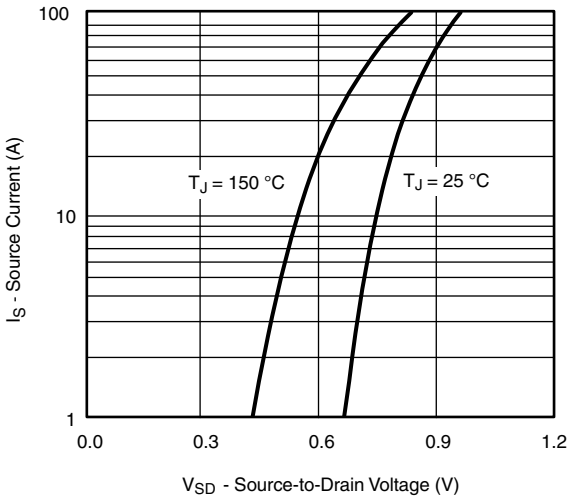


Gate Charge

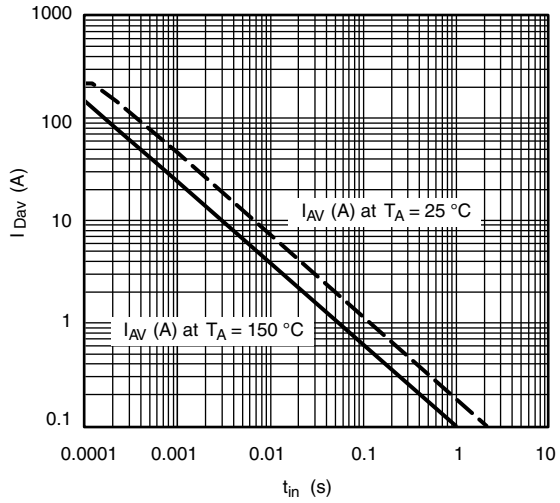
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



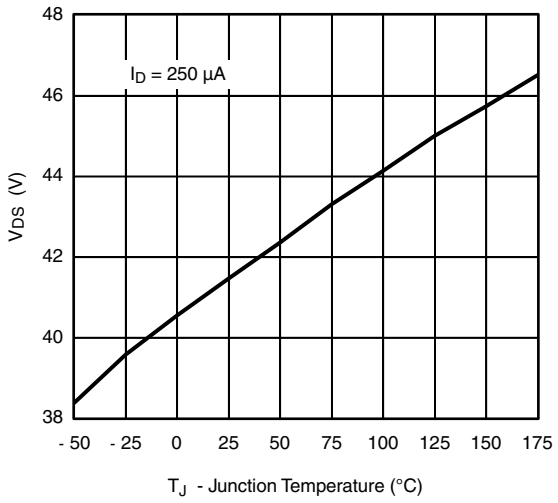
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

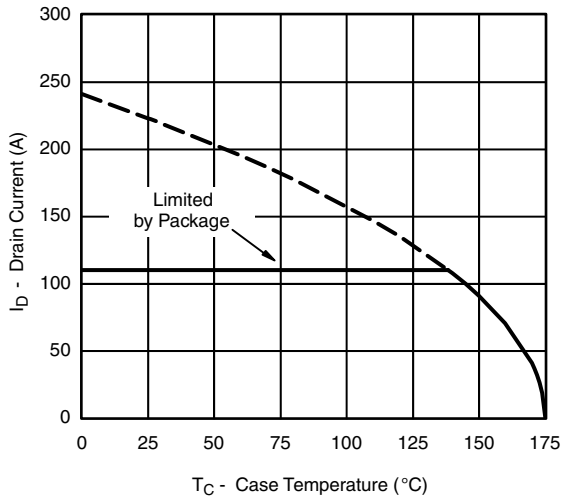


Avalanche Current vs. Time

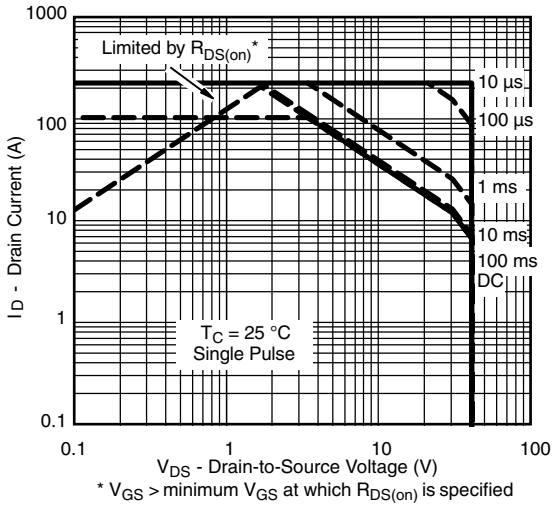


Drain Source Breakdown vs. Junction Temperature

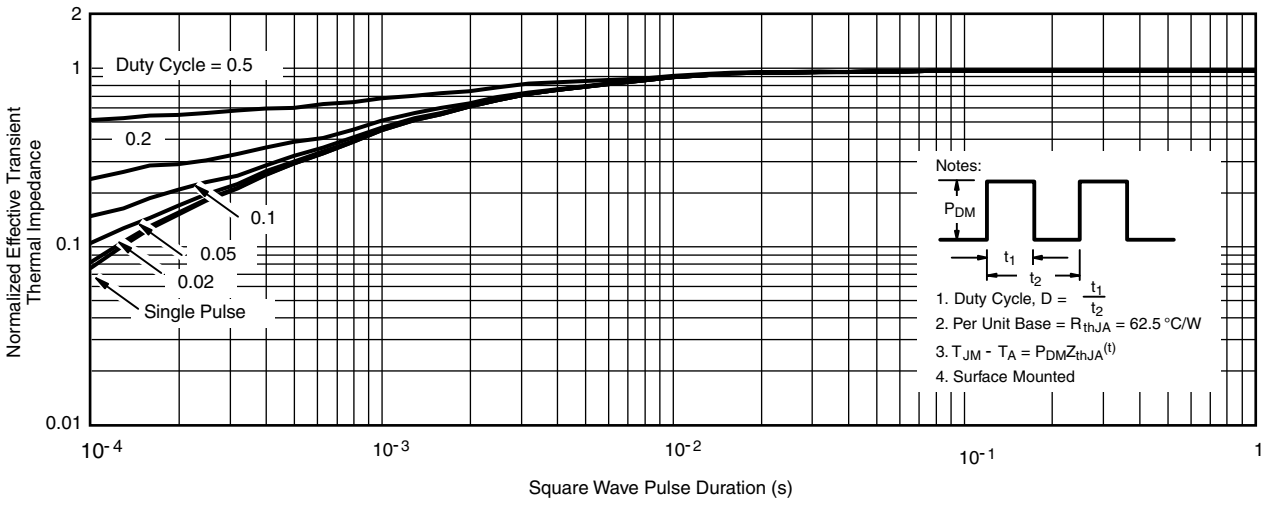
THERMAL RATINGS



Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

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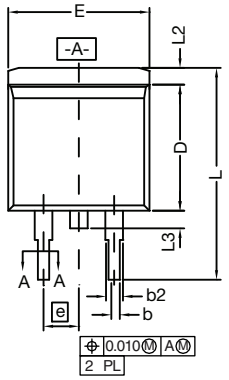
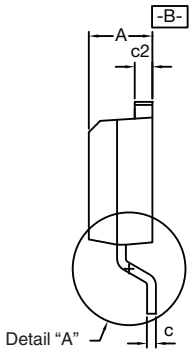
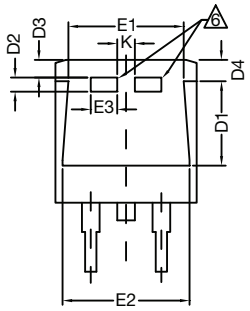
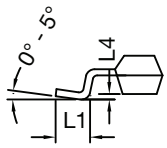
TO-263 (D²PAK): 3-LEAD

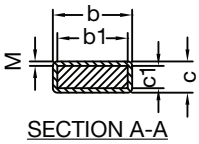








DETAIL A (ROTATED 90°)



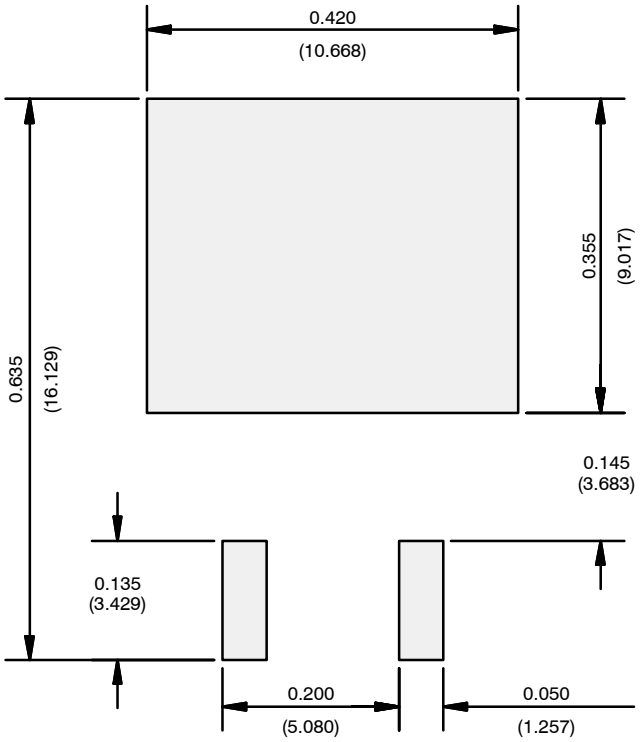
SECTION A-A

DIM.		INCHES		MILLIMETERS	
		MIN.	MAX.	MIN.	MAX.
A		0.160	0.190	4.064	4.826
b		0.020	0.039	0.508	0.990
b1		0.020	0.035	0.508	0.889
b2		0.045	0.055	1.143	1.397
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2		0.045	0.055	1.143	1.397
D		0.340	0.380	8.636	9.652
D1		0.220	0.240	5.588	6.096
D2		0.038	0.042	0.965	1.067
D3		0.045	0.055	1.143	1.397
D4		0.044	0.052	1.118	1.321
E		0.380	0.410	9.652	10.414
E1		0.245	-	6.223	-
E2		0.355	0.375	9.017	9.525
E3		0.072	0.078	1.829	1.981
e		0.100 BSC		2.54 BSC	
K		0.045	0.055	1.143	1.397
L		0.575	0.625	14.605	15.875
L1		0.090	0.110	2.286	2.794
L2		0.040	0.055	1.016	1.397
L3		0.050	0.070	1.270	1.778
L4		0.010 BSC		0.254 BSC	
M		-	0.002	-	0.050
ECN: T13-0707-Rev. K, 30-Sep-13 DWG: 5843					

Notes

1. Plane B includes maximum features of heat sink tab and plastic.
2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
3. Pin-to-pin coplanarity max. 4 mils.
4. *: Thin lead is for SUB, SYB.
   Thick lead is for SUM, SYM, SQM.
5. Use inches as the primary measurement.
6. This feature is for thick lead.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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