Features

- Low-voltage Programmable Logic Device
 - Wide Power Supply Range 3.0V to 5.5V
 - Ideal for Battery Powered Systems
- High-speed Operation
 - 20 ns Maximum Propagation Delay at V_{CC} = 3.0V
- Commercial and Industrial Temperature Ranges
- Familiar 22V10 Logic Architecture
- Low-power 3-volt CMOS Operation

	AT22LV10L	AT22LV10	
Temp	Com./Ind.	Com./Ind.	
I _{CC} (mA)	4/5	35/45	V _{CC} = 3.6V

- CMOS and TTL Compatible Inputs and Outputs – 10 µA Leakage Maximum
- Reprogrammable Tested 100% for Programmability
- High-reliability CMOS Technology
 - 2000V ESD Protection
 - 200 mA Latchup Immunity
- Dual-in-line and Surface Mount Packages

Logic Diagram



Description

The AT22LV10 and AT22LV10L are low-voltage compatible CMOS high-performance Programmable Logic Devices (PLDs). Speeds down to 20 ns and power dissipation as low as 14.4 mW are offered. All speed ranges are specified over the 3.0V to 5.5V range. All pins offer a low $\pm 10 \ \mu$ A leakage.

The AT22LV10L provides the optimum low-power CMOS PLD solution, with low DC power (1 mA typical at V_{CC} = 3.3V) and full CMOS output levels. The AT22LV10L significantly reduces total system power, allowing battery powered operation.

Pin Configurations

(continued)





Low-voltage UV **Erasable** Programmable **Logic Device**

AT22LV10 AT22LV10L

Rev. 0190E-08/99





Full CMOS output levels help reduce power in many other system components.

The AT22LV10 and AT22LV10L logic architectures are identical to the familiar 22V10. Each output is allocated from eight to 16 product terms, which allows highly complex logic functions to be realized.

Two additional product terms are included to provide synchronous preset and asynchronous reset. These terms are common to all ten registers. All registers are automatically cleared upon power-up.

Register preload simplifies testing. A security fuse prevents unauthorized copying of programmed fuse patterns.

Absolute Maximum Ratings*

Temperature Under Bias55°C to +125°C
Storage Temperature65°C to +150°C
Voltage on Any Pin with Respect to Ground2.0V to +7.0V ⁽¹⁾
Voltage on Input Pins with Respect to Ground During Programming
Programming Voltage with Respect to Ground2.0V to +14.0V ⁽¹⁾
Integrated UV Erase Dose7258 W-sec/cm ²

- *NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- Note: 1. Minimum voltage is -0.6V DC which may undershoot to -2.0V for pulses of less than 20 ns. Maximum pin voltage is V_{CC} + 0.75V DC which may undershoot to V_{CC} + 2.0V for pulses of less than 20 ns.

DC and AC Operating Conditions

	Commercial	Industrial
Operating Temperature (Ambient)	0°C - 70°C	-40°C - 85°C
V _{CC} Power Supply	3.0V to 5.5V	3.0V to 5.5V

Logic Options



Output Options





AT22LV10(L)

DC Characteristics

Symbol	Parameter	Condition ⁽²⁾	Condition ⁽²⁾			Тур	Max	Units
I _{LI}	Input Load Current	V_{IN} = -0.1V to V_{CC}	$V_{IN} = -0.1V$ to $V_{CC} + 1V$				10	μA
I _{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{C}	V_{OUT} = -0.1V to V_{CC} + 0.1V				10	μA
				Com.		20/50	35/90	mA
	Power Supply	$V_{\rm CC} = 3.6 \text{V}/5.5 \text{V},$	AT22LV10	Ind.		20/50	45/100	mA
I _{CC}	Current	V _{IN} = GND, Outputs Open		Com.		1/2	4/12	mA
			AT22LV10L	Ind.		1/2	5/15	mA
I _{OS} ⁽¹⁾	Output Short Circuit Current	V _{OUT} = 0.5V					-120	mA
V _{IL1}	Input Low Voltage	$4.5V \le V_{CC \le} 5.5V$	$4.5V \le V_{CC \le} 5.5V$				0.8	V
V _{IL2}	Input Low Voltage	$3.0V \le V_{CC} \le 4.5V$			-0.6		0.6	V
VIH	Input High Voltage				2.0		V _{CC} + 0.75	V
		$V_{CC} = 3.0V$	Com., Ind.	I _{OL} = 8 mA			0.5	V
V _{OL}	Output Low Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{\rm CC} = 4.5 V$	Com., Ind.	I _{OL} = 16 mA			0.5	V
		$V_{CC} = 3.0V$	Com., Ind.	I _{OL} = 6 mA			0.35	V
N/		Output Lligh Valtage $V_{\rm IN} = V_{\rm H} \text{ or } V_{\rm IL},$	I _{OH} = -100 μA		V _{CC} - 0.3			V
V _{OH}	Output High Voltage	$V_{CC} = 3.0 V/4.5 V$	I _{OH} = -0.4 mA/	-4.0 mA	2.4			V

Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec. 2. For DC characteristics, the test condition of V_{CC} = Max corresponds to 3.6V.





AC Characteristics for the AT22LV10

			AT22LV10-2	0		AT22LV10-2	5	
Symbol	Parameter	Min	Тур	Max	Min	Тур	Мах	Units
t _{PD}	Input or Feedback to Non- Registered Output		12	20		15	25	ns
t _{EA}	Input to Output Enable			20		15	25	ns
t _{ER}	Input to Output Disable			20		15	25	ns
t _{CF}	Clock to Feedback	0	4	9	0	5	9	ns
t _{CO}	Clock to Output	0	8	14	0	10	17	ns
t _S	Input or Feedback Setup Time	10	6		12	7		ns
t _H	Hold Time	0			0			ns
t _P	Clock Period	10			12			ns
t _W	Clock Width	5			6			ns
	External Feedback 1/(t _S +t _{CO})			41.6			34.5	MHz
F _{MAX}	Internal Feedback 1/(t _S + t _{CF})			52.6			47.6	MHz
	No Feedback 1/(t _P)			100.0			83.3	MHz
t _{AW}	Asynchronous Reset Width	20	12		25	15		ns
t _{AR}	Asynchronous Reset, Synchronous Preset, Recovery Time	20	12		25	15		ns
t _{AP}	Asynchronous Reset to Registered Output Reset		15	25		18	28	ns

AC Waveforms⁽¹⁾



Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.



AC Characteristics for the AT22LV10L

			AT22LV10L-2	5		
Symbol	Parameter	Min	Тур	Max 25	Units	
t _{PD}	Input or Feedback to Non-Registered Output		15		ns	
t _{EA}	Input to Output Enable		15	25	ns	
t _{ER}	Input to Output Disable		15	25	ns	
t _{CF}	Clock to Feedback	0	5	9	ns	
t _{CO}	Clock to Output	0	10	14	ns	
t _{SF}	Feedback Setup Time	12	7		ns	
t _S	Input Setup Time	17	15		ns	
t _H	Hold Time	0			ns	
t _P	Clock Period	12			ns	
t _W	Clock Width	6			ns	
	External Feedback 1/(t _S + t _{CO})			32.2	MHz	
F _{MAX}	Internal Feedback 1/(t _{SF} + t _{CF})			47.6	MHz	
	No Feedback 1/(t _P)			83.3	MHz	
t _{AW}	Asynchronous Reset Width	25	15		ns	
t _{AR}	Asynchronous Reset Recovery Time	25	15		ns	
t _{AP}	Asynchronous Reset to Registered Output Reset		18	28	ns	

Input Test Waveforms and Measurement Levels



Output Test Loads

Commercial







Functional Logic Diagram AT22LV10(L)



Preload of Registered Outputs

The registers in the AT22LV10 and AT22LV10L are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the I/O pin will force the register high; a V_{IL} will force it low, independent of the polarity bit (C0) setting. The preload state is entered by placing an 11.5V to 13V signal on pin 8 on

DIPs, and pin 10 on SMPs. When the clock pin is pulsed high, the data on the I/O pins is placed into the ten registers.

Level Forced on Registered Output Pin During Preload Cycle	Register State After Cycle
V _{IH}	High
V _{IL}	Low



Power-up Reset

The registers in the AT22LV10 and AT22LV10L are designed to reset during power-up. At a point delayed slightly from V_{CC} crossing 2.5V, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

- 1. The V_{CC} rise must be monotonis;
- 2. After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and
- 3. The clock must remain stable during t_{PR} .

Pin Capacitance

 $(f = 1 \text{ MHz}, T = 25^{\circ}C)^{(1)}$

	Тур	Max	Units	Conditions
C _{IN}	5	8	pF	$V_{IN} = 0V$
C _{OUT}	6	8	pF	$V_{OUT} = 0V$

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Erasure Characteristics

The entire fuse array of an AT22LV10 or AT22LV10L is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 μ W/cm² intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from

the minimum integrated erasure dose of 15 W-sec/cm². To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable PLD which will be subjected to continuous fluorescent indoor lighting or sunlight.





Parameter	Description	Min	Тур	Мах	Units
t _{PR}	Power-up Reset Time		600	1000	ns













SUPPLY CURRENT vs. INPUT FREQUENCY

AT22LV10 (TA = 25°C)

 $V_{CC} = 5.0V$

60



NORMALIZED ICC vs. AMBIENT TEMP.





OUTPUT VOLTAGE (V)

OUTPUT SOURCE CURRENT

vs. OUTPUT VOLTAGE (TA = 25°C)

V_{CC}= 3.3V

2

3

OUTPUT VOLTAGE (V)

 $V_{\rm CC} = 5.0 V$

5

O U T P U T

C U R R E N T

m

А

0

-8

-16

-24

-32

ō







MEL







Ordering Information

t _{PD} (ns)	t _s (ns)	t _{co} (ns)	Ordering Code	Package	Operation Range
20	10	14	AT22LV10-20JC AT22LV10-20PC AT22LV10-20SC	28J 24P3 24S	Commercial (0°C to 70°C)
			AT22LV10-20JI AT22LV10-20PI AT22LV10-20SI	28J 24P3 24S	Industrial (-40°C to 85°C)
25	12	17	AT22LV10-25JC AT22LV10-25PC AT22LV10-25SC	28J 24P3 24S	Commercial (0°C to 70°C)
			AT22LV10-25JI AT22LV10-25PI AT22LV10-25SI	28J 24P3 24S	Industrial (-40°C to 85°C)
25	17	14	AT22LV10L-25JC AT22LV10L-25PC AT22LV10L-25SC	28J 24P3 24S	Commercial (0°C to 70°C)
			AT22LV10L-25JI AT22LV10L-25PI AT22LV10L-25SI	28J 24P3 24S	Industrial (-40°C to 85°C)

Using "C" Product for Industrial

To use commercial product for Industrial temperature ranges, down-grade one speed grade from the "I" to the "C" device (7 ns "C" = 10 ns "I") and de-rate power by 30%.

	Package Type					
28J	28-Jead, Plastic J-leaded Chip Carrier OTP (PLCC)					
24P3	24-lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)					
24S	24S 24-lead, 0.300" Wide, Plastic Gull-Wing Small Outline OTP (SOIC)					

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