

- Qualified for Automotive Applications
- 2-V to 6-V  $V_{CC}$  Operation
- Inputs Accept Voltages to 6 V
- Max  $t_{pd}$  of 6.5 ns at 5 V

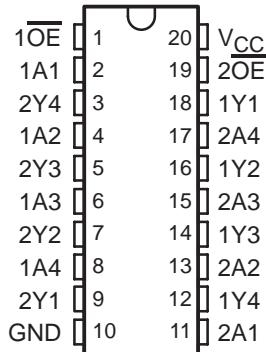
### description/ordering information

This octal buffer and line driver is designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The SN74AC240 device is organized as two 4-bit buffers/drivers with separate output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the device passes inverted data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

DW OR PW PACKAGE  
(TOP VIEW)



### ORDERING INFORMATION

$T_A$	PACKAGE <sup>‡</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SOIC – DW	Tape and reel	SN74AC240QDWQRQ1	AC240Q
	TSSOP – PW	Tape and reel	SN74AC240QPWRQ1	AC240Q

<sup>†</sup> For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

<sup>‡</sup> Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

FUNCTION TABLE  
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

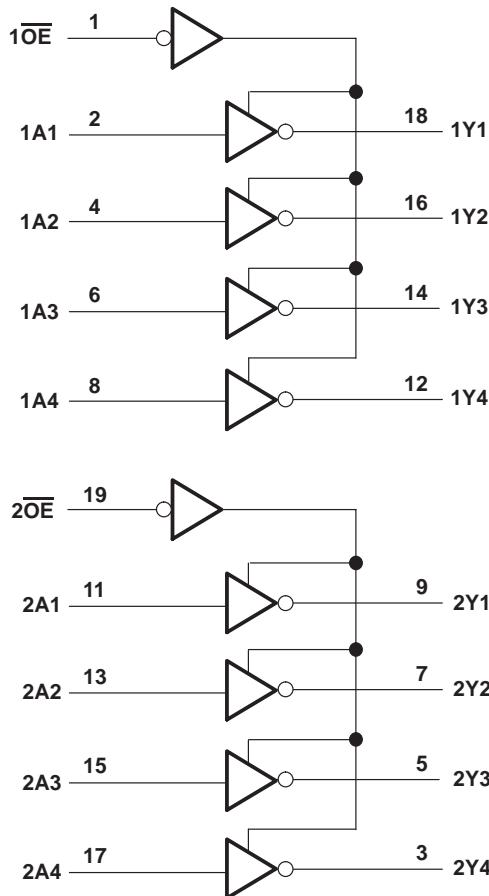


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**SN74AC240-Q1**  
**OCTAL BUFFER/DRIVER**  
**WITH 3-STATE OUTPUTS**

SCAS785A – OCTOBER 2004 – REVISED JANUARY 2008

**logic diagram (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to $V_{CC}$ + 0.5 V
Output voltage range, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 200$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DW package .....	58°C/W
	PW package .....
	83°C/W
Storage temperature range, $T_{STG}$ .....	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JEDEC 51-7.

**recommended operating conditions (see Note 3)**

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 3 V	2.1	V
		V <sub>CC</sub> = 4.5 V	3.15	
		V <sub>CC</sub> = 5.5 V	3.85	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 3 V	0.9	V
		V <sub>CC</sub> = 4.5 V	1.35	
		V <sub>CC</sub> = 5.5 V	1.65	
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 3 V	-12	mA
		V <sub>CC</sub> = 4.5 V	-24	
		V <sub>CC</sub> = 5.5 V	-24	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 3 V	12	mA
		V <sub>CC</sub> = 4.5 V	24	
		V <sub>CC</sub> = 5.5 V	24	
Δt/Δv	Input transition rise or fall rate		8	ns/V
T <sub>A</sub>	Operating free-air temperature	-40	125	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**SN74AC240-Q1**  
**OCTAL BUFFER/DRIVER**  
**WITH 3-STATE OUTPUTS**

SCAS785A – OCTOBER 2004 – REVISED JANUARY 2008

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C TO 125°C		T <sub>A</sub> = -40°C TO 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 µA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I <sub>OH</sub> = -12 mA	3 V	2.56			2.4		2.46		
		4.5 V	3.86			3.7		3.76		
		5.5 V	4.86			4.7		4.76		
	I <sub>OH</sub> = -24 mA	5.5 V				3.85				
		5.5 V						3.85		
	I <sub>OH</sub> = -50 mA <sup>†</sup>	5.5 V								
		5.5 V								
V <sub>OL</sub>	I <sub>OL</sub> = 50 µA	3 V		0.1		0.1		0.1		V
		4.5 V		0.1		0.1		0.1		
		5.5 V		0.1		0.1		0.1		
	I <sub>OL</sub> = 12 mA	3 V		0.36		0.5		0.44		
		4.5 V		0.36		0.5		0.44		
	I <sub>OL</sub> = 24 mA	5.5 V		0.36		0.5		0.44		
		5.5 V		0.36		0.5		0.44		
	I <sub>OL</sub> = 50 mA <sup>†</sup>	5.5 V				1.65				
		5.5 V						1.65		
I <sub>I</sub>	Data inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V		±0.1		±1		±1	µA
	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND			±0.1		±1		±1	
I <sub>OZ</sub> <sup>‡</sup>	V <sub>O</sub> = V <sub>CC</sub> or GND, V <sub>I(OE)</sub> = V <sub>IL</sub> or V <sub>IH</sub>	5.5 V		±0.25		±5		±2.5		µA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4		80		40	µA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2.5						pF

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

<sup>‡</sup> For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

switching characteristics over recommended operating free-air temperature range,  
V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C TO 125°C		T <sub>A</sub> = -40°C TO 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A	Y	1.5	6	8	1	11	1	9	ns
			1.5	5.5	8	1	10.5	1	8.5	
t <sub>PHL</sub>	OE	Y	1.5	6	10.5	1	11.5	1	11	ns
			1.5	7	10	1	13	1	11	
t <sub>PZH</sub>	OE	Y	1.5	7	10	1	12.5	1	10.5	ns
			1.5	7.5	10.5	1	13.5	1	11.5	
t <sub>PZL</sub>										

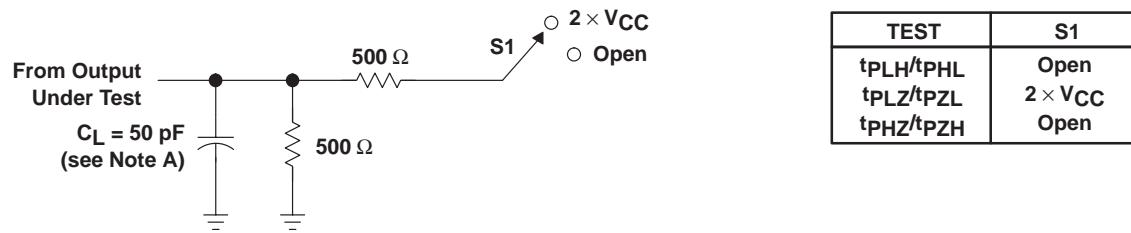
switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ TO $125^\circ\text{C}$		$T_A = -40^\circ\text{C}$ TO $85^\circ\text{C}$		UNIT	
			MIN TYP MAX			MIN MAX		MIN MAX			
			1.5	4.5	6.5	1	8.5	1	7		
$t_{PLH}$	A	Y	1.5	4.5	6.5	1	8.5	1	7	ns	
$t_{PHL}$			1.5	4.5	6	1	8	1	6.5		
$t_{PZH}$	$\overline{OE}$	Y	1.5	5	7	1	9	1	8	ns	
$t_{PZL}$			1.5	5.5	8	1	10.5	1	8.5		
$t_{PHZ}$	$\overline{OE}$	Y	2.5	6.5	9	1	10.5	1	9.5	ns	
$t_{PLZ}$			2	6.5	9	1	11	1	9.5		

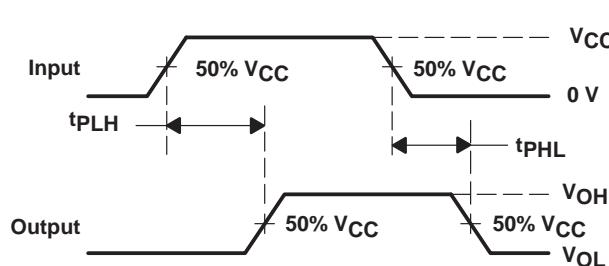
operating characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance per buffer/driver	$C_L = 50 \text{ pF}$ , $f = 1 \text{ MHz}$	45	pF

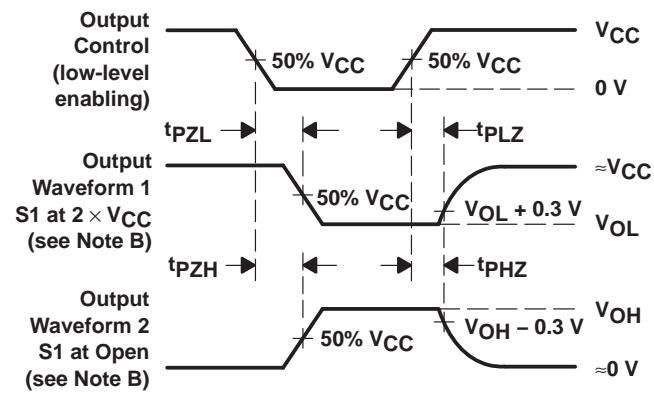
### PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
D. The outputs are measured one at a time, with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AC240QPWRG4Q1	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC240Q	<b>Samples</b>
SN74AC240QPWRQ1	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC240Q	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74AC240-Q1 :

- Catalog: [SN74AC240](#)
- Military: [SN54AC240](#)

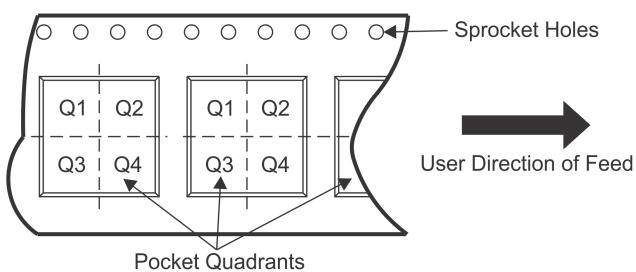
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC240QPWRG4Q1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AC240QPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

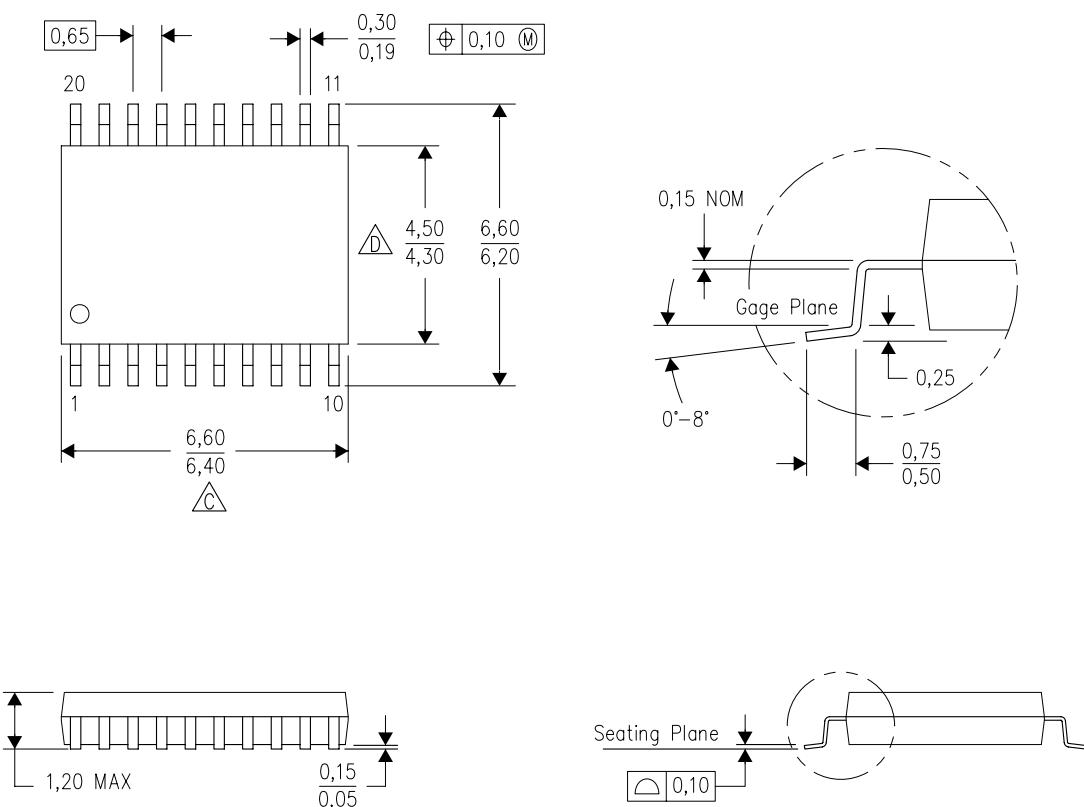
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC240QPWRG4Q1	TSSOP	PW	20	2000	367.0	367.0	38.0
SN74AC240QPWRQ1	TSSOP	PW	20	2000	367.0	367.0	38.0

PW (R-PDSO-G20)

## PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

 Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 each side.

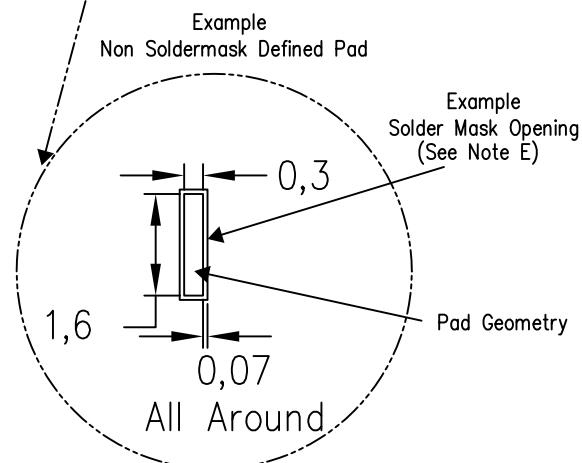
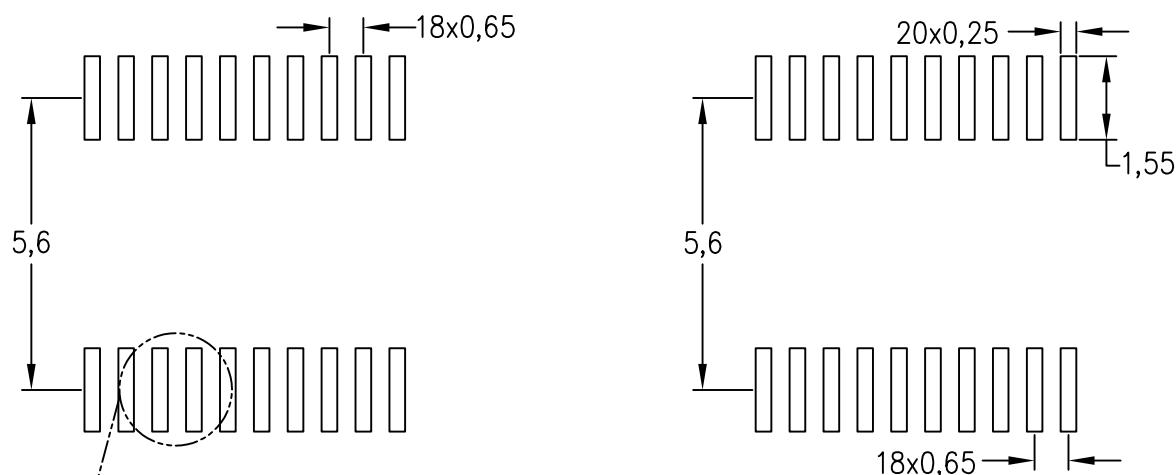
**D** Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

## Example Board Layout

Based on a stencil thickness  
of .127mm (.005inch).

4211284-5/G 08/15

NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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