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# FDP20N50F / FDPF20N50FT

## N-Channel UniFET™ FRFET® MOSFET

500 V, 20 A, 260 mΩ

### Features

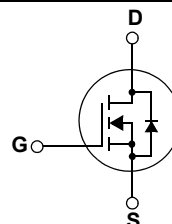
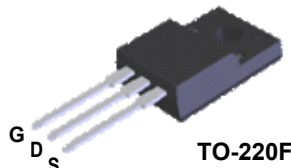
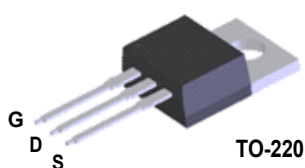
- $R_{DS(on)} = 210 \text{ m}\Omega$  (Typ.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 10 \text{ A}$
- Low Gate Charge (Typ. 50 nC)
- Low  $C_{rss}$  (Typ. 27 pF)
- 100% Avalanche Aested
- Improve dv/dt Capability
- RoHS Compliant

### Applications

- LCD/LED/PDP TV
- Lighting
- Uninterruptible Power Supply
- AC-DC Power Supply

### Description

UniFET™ MOSFET is Fairchild Semiconductor®'s high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. The body diode's reverse recovery performance of UniFET FRFET® MOSFET has been enhanced by lifetime control. Its  $t_{rr}$  is less than 100nsec and the reverse dv/dt immunity is 15V/ns while normal planar MOSFETs have over 200nsec and 4.5V/nsec respectively. Therefore, it can remove additional component and improve system reliability in certain applications in which the performance of MOSFET's body diode is significant. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FDP20N50F	FDPF20N50FT	Unit
$V_{DSS}$	Drain to Source Voltage	500		V
$V_{GSS}$	Gate to Source Voltage	±30		V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	20	20*
		- Continuous ( $T_C = 100^\circ\text{C}$ )	12.9	12.9*
$I_{DM}$	Drain Current	- Pulsed (Note 1)	80	80*
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	1110		mJ
$I_{AR}$	Avalanche Current (Note 1)	20		A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	25		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	20		V/ns
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	250	38.5
		- Derate above $25^\circ\text{C}$	2.0	0.3
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300		$^\circ\text{C}$

\*Drain current limited by maximum junction temperature

### Thermal Characteristics

Symbol	Parameter	FDP20N50F	FDPF20N50FT	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.5	3.3	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Thermal Resistance, Case to Sink, Typ.	0.5	-	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	62.5	

**Package Marking and Ordering Information**  $T_C = 25^\circ\text{C}$  unless otherwise noted

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP20N50F	FDP20N50F	TO-220	-	-	50
FDPF20N50FT	FDPF20N50FT	TO-220F	-	-	50

**Electrical Characteristics**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}, T_J = 25^\circ\text{C}$	500	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	0.7	-	$V/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 50\text{V}, V_{GS} = 0\text{V}$	-	-	10	$\mu\text{A}$
		$V_{DS} = 40\text{V}, T_C = 125^\circ\text{C}$	-	-	100	
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 30\text{V}, V_{DS} = 0\text{V}$	-	-	$\pm 100$	nA

**On Characteristics**

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 10\text{A}$	-	0.22	0.26	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 20\text{V}, I_D = 10\text{A}$	-	25	-	S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	2550	3390	pF
$C_{oss}$	Output Capacitance		-	350	465	pF
$C_{rss}$	Reverse Transfer Capacitance		-	27	40	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 40\text{V}, I_D = 20\text{A}$ $V_{GS} = 10\text{V}$	-	50	65	nC
$Q_{gs}$	Gate to Source Gate Charge		-	14	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	20	-	nC

(Note 4)

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250\text{V}, I_D = 20\text{A}$ $R_G = 25\Omega$	-	45	100	ns
$t_r$	Turn-On Rise Time		-	120	250	ns
$t_{d(off)}$	Turn-Off Delay Time		-	100	210	ns
$t_f$	Turn-Off Fall Time		-	60	130	ns

(Note 4)

**Drain-Source Diode Characteristics**

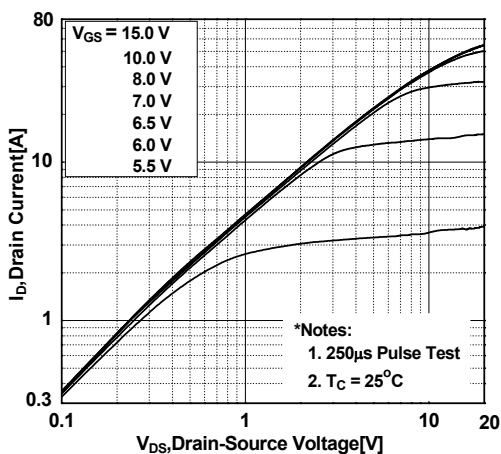
$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	20	A	
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	80	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_{SD} = 20\text{A}$	-	-	1.5	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{V}, I_{SD} = 20\text{A}$	-	154	-	ns
$Q_{rr}$	Reverse Recovery Charge	$di_F/dt = 100\text{A}/\mu\text{s}$	-	0.5	-	$\mu\text{C}$

**Notes:**

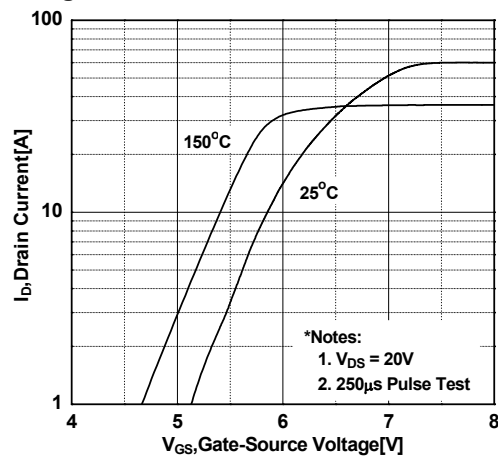
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2.  $L = 5\text{mH}, I_{AS} = 20\text{A}, V_{DD} = 50\text{V}, R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 20\text{A}, di/dt \leq 200\text{A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Essentially Independent of Operating Temperature Typical Characteristics

## Typical Performance Characteristics

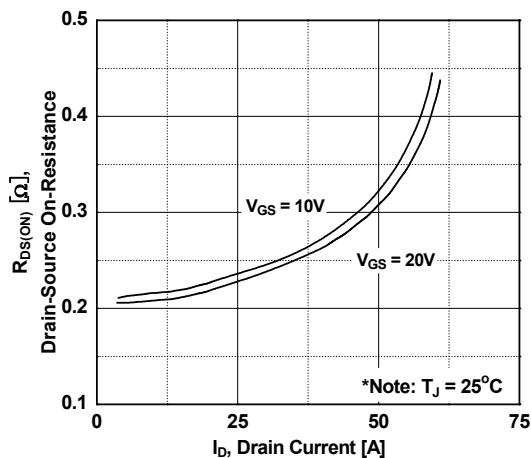
**Figure 1. On-Region Characteristics**



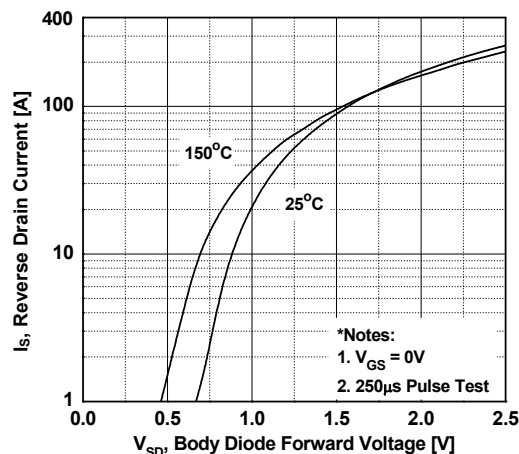
**Figure 2. Transfer Characteristics**



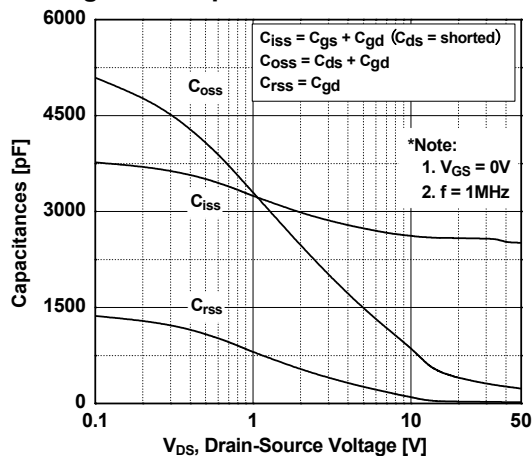
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



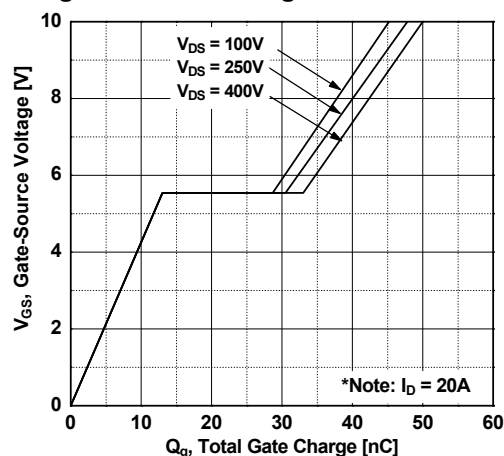
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

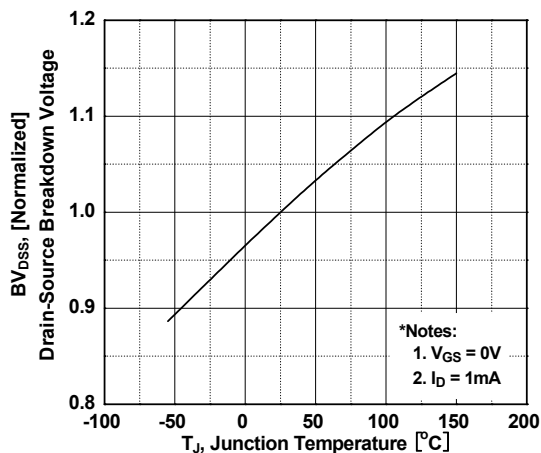


**Figure 6. Gate Charge Characteristics**

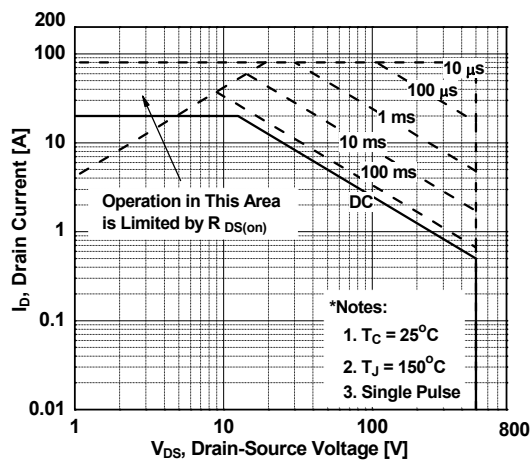


**Typical Performance Characteristics** (Continued)

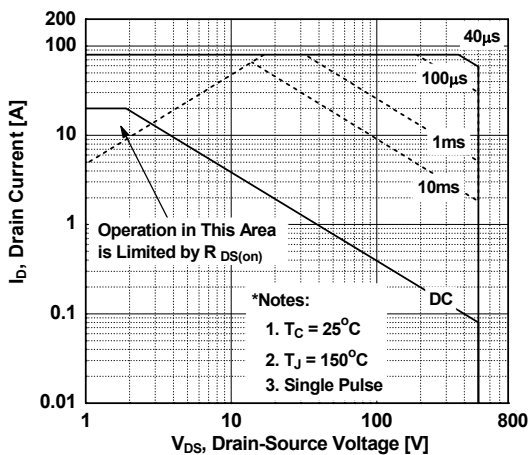
**Figure 7. Breakdown Voltage Variation vs. Temperature**



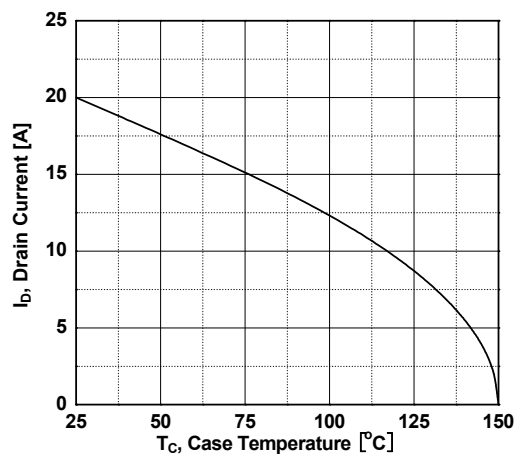
**Figure 8. Maximum Safe Operating Area - FDP20N50F**



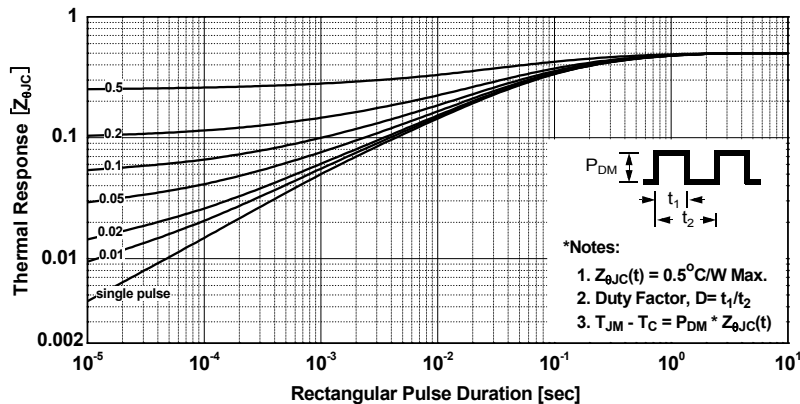
**Figure 9. Maximum Safe Operating Area - FDPF20N50FT**



**Figure 10. Maximum Drain Current vs. Case Temperature**

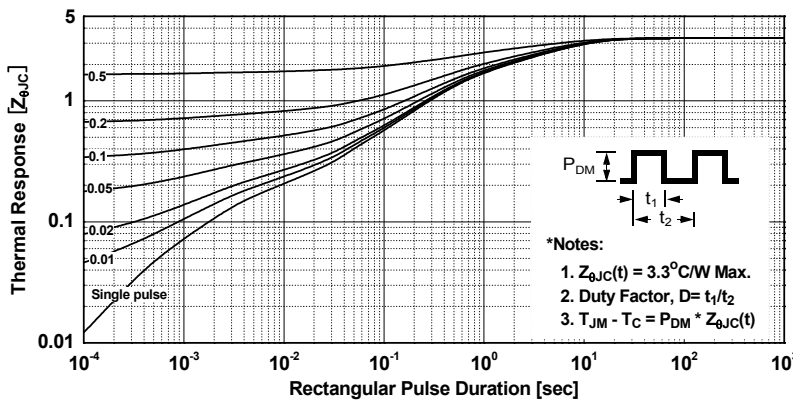


**Figure 11. Transient Thermal Response Curve - FDP20N50F**

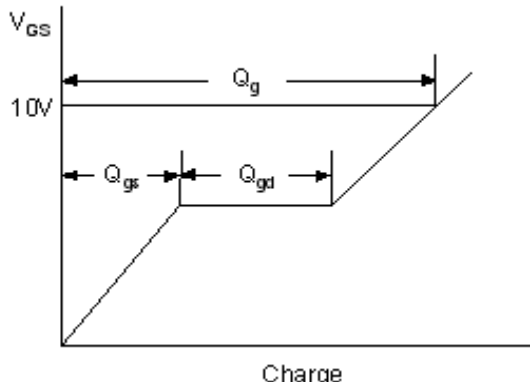
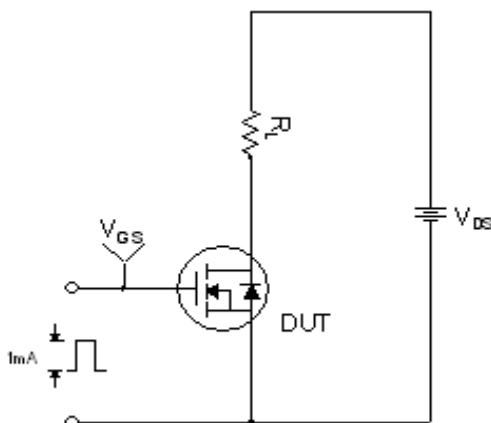


Typical Performance Characteristics (Continued)

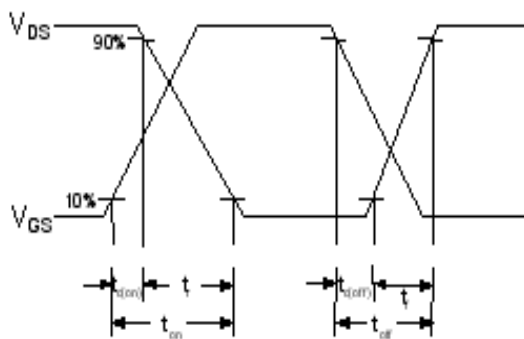
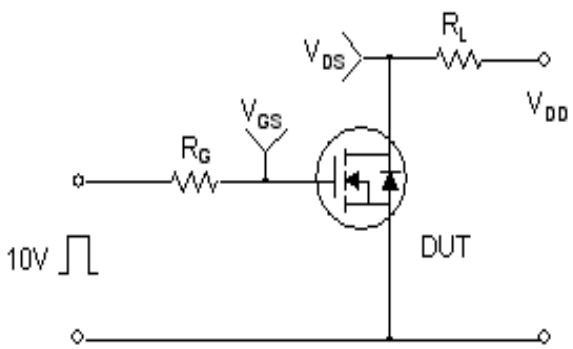
Figure 12. Transient Thermal Response Curve - FDPF20N50FT



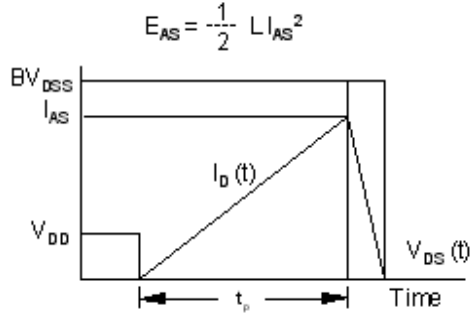
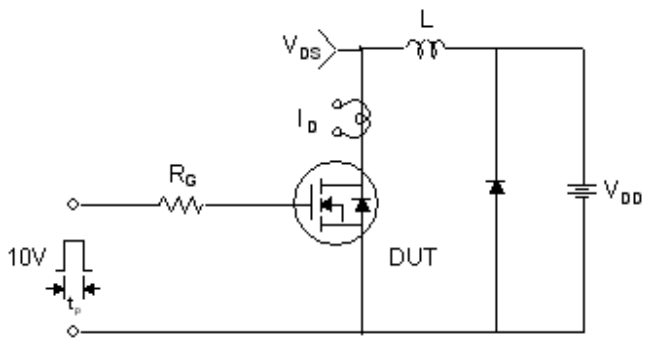
**Gate Charge Test Circuit & Waveform**



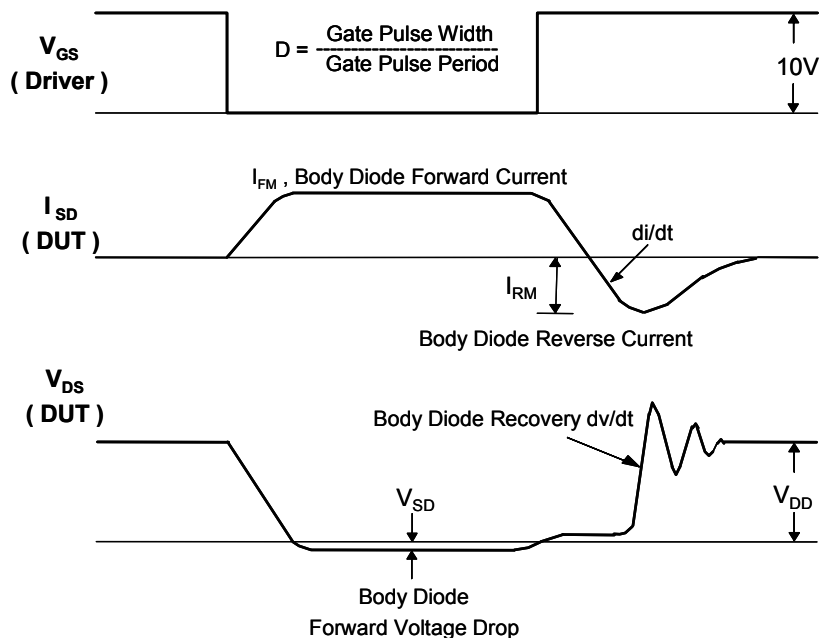
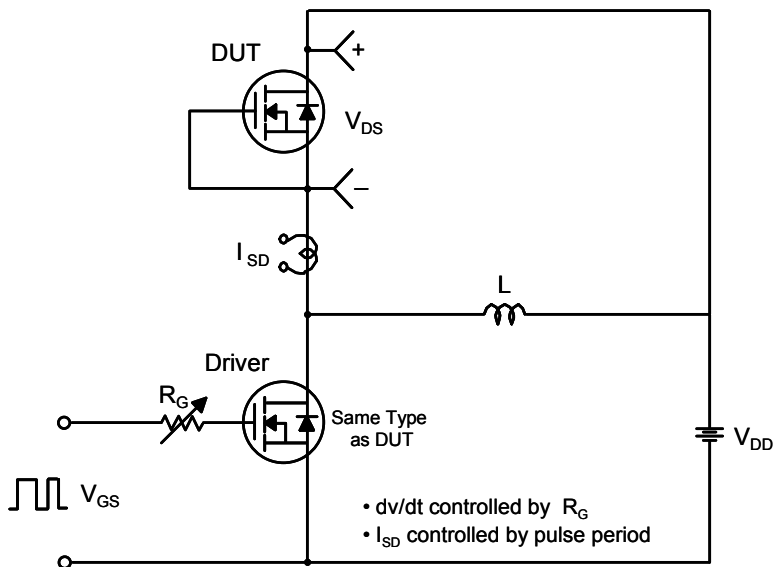
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching Test Circuit & Waveforms**



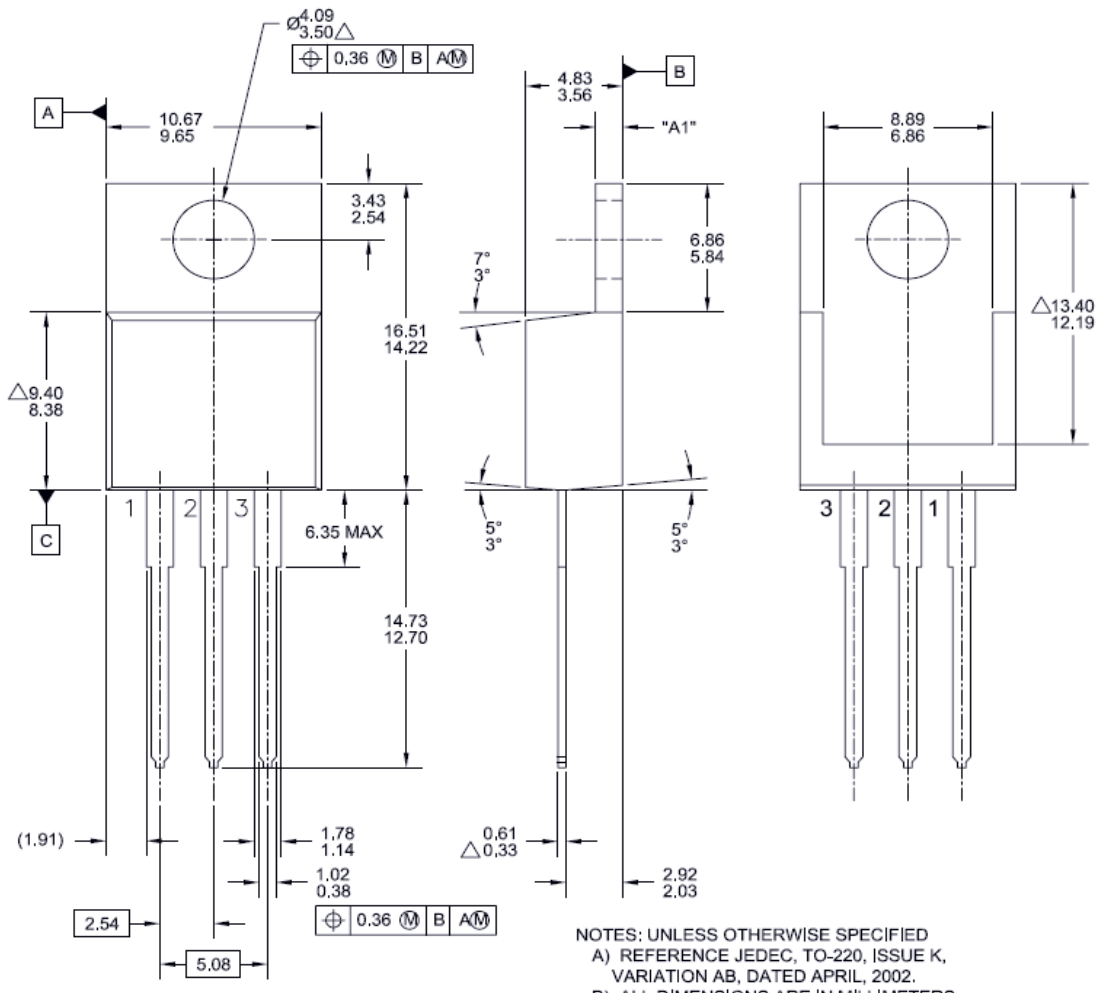
Peak Diode Recovery dv/dt Test Circuit & Waveforms



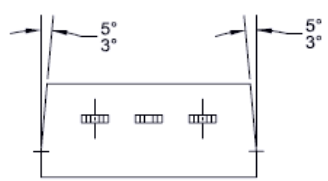


**Mechanical Dimensions**

**TO-220B03**



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) REFERENCE JEDEC, TO-220, ISSUE K, VARIATION AB, DATED APRIL, 2002.
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONING AND TOLERANCING PER ANSI Y14.5 - 1973
  - D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
  - $\Delta$  DOES NOT COMPLY JEDEC STANDARD VALUE.
  - F) "A1" DIMENSIONS REPRESENT LIKE BELOW:  
 SINGLE GAUGE = 0.51 - 0.61  
 DUAL GAUGE = 1.14 - 1.40
  - G) DRAWING FILE NAME: TO220B03REV6







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