SY89833L

3.3V Ultra-Precision 1:4 LVDS Fanout Buffer/Translator with Internal Termination

General Description

The SY89833L is a 3.3V, high-speed 2GHz differential low voltage differential swing (LVDS) 1:4 fanout buffer optimized for ultra-low skew applications. Within device skew is guaranteed to be less than 20ps over supply voltage and temperature.

The differential input buffer has a unique internal termination design that allows access to the termination network through a VT pin. This feature allows the device to easily interface to different logic standards. A VREF-AC reference is included for AC-coupled applications.

The SY89833L is part of Micrel's high-speed clock synchronization family. For 2.5V applications, the SY89832U provides similar functionality while operating from a 2.5V ±5% supply. For applications that require a different I/O combination, consult the Micrel website at www.micrel.com, and choose from a comprehensive product line of high-speed, low-skew fanout buffers, translators and clock generators.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

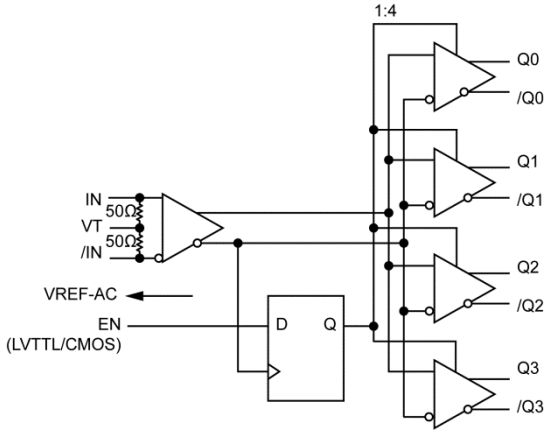
Features

- Guaranteed AC performance over temperature and voltage:
  - DC-to > 2GHz throughput
  - <600ps propagation delay (IN-to-Q)
  - <20ps within-device skew
  - <150ps rise/fall times
- Ultra-low jitter design:
  - 98fs$_{RMS}$ phase jitter
- Patented Any-In input termination and VT pin accepts DC- and AC-coupled inputs
- High-speed LVDS outputs
- 3.3V power supply operation:
  - Industrial temperature range: -40°C to +85°C
- Available in 16-pin (3mm × 3mm) QFN package

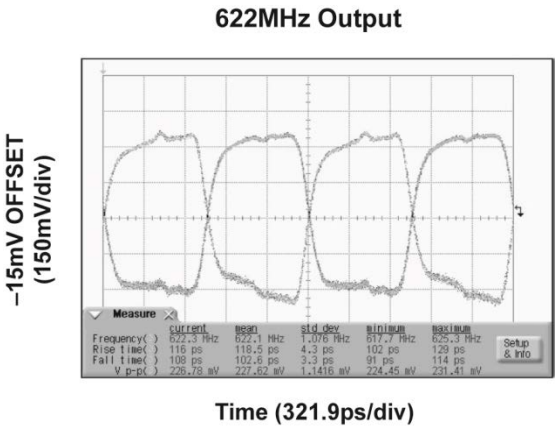
Applications

- Processor clock distribution
- SONET clock distribution
- Fibre Channel clock distribution
- Gigabit Ethernet clock distribution

Functional Block Diagram



Typical Performance



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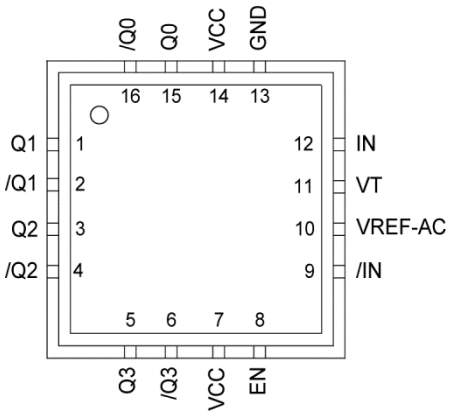
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89833LMG	QFN-16	Industrial	833L with Pb-Free Bar Line Indicator	NiPdAu Pb-Free
SY89833LMG TR[2]	QFN-16	Industrial	833L with Pb-Free Bar Line Indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.

Pin Configuration



16-Pin 3mm × 3mm QFN

Pin Description

Pin Number	Pin Name	Pin Function
15, 16 1, 2 3, 4 5, 6	Q0, /Q0 Q1, /Q1 Q2, /Q2 Q3, /Q3	LVDS Differential Outputs: Normally terminated with 100Ω across the pair (Q, /Q). See “LVDS Outputs” section. Unused outputs should be terminated with a 100Ω resistor across each pair.
8	EN	This single-ended TTL/CMOS-compatible input functions as a synchronous output enable. The synchronous enable ensures that enable/disable will only occur when the outputs are in a logic LOW state. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to logic HIGH state (enabled) if left open.
9, 12	/IN, IN	Differential Inputs: These input pairs are the differential signal inputs to the device. Inputs accept AC- or DC-Coupled differential signals as small as 100mV. Each pin of a pair internally terminates to a VT pin through 50Ω. Note that these inputs will default to an intermediate state if left open. Please refer to the “Input Interface Applications” section for more details.
10	VREF-AC	Reference Voltage: These outputs bias to V_{CC}-1.4V.They are used when AC coupling the inputs (IN, /IN). For AC-Coupled applications, connect VREF-AC to VT pin and bypass with 0.01µF low ESR capacitor to V_{CC}. See “Input Interface Applications” section for more details. Maximum sink/source current is ±1.5mA. Due to the limited drive capability, each VREF-AC pin is only intended to drive its respective VT pin.

Pin Description (Continued)

Pin Number	Pin Name	Pin Function
11	VT	Input Termination Center-Tap: Each side of the differential input pair terminates to a VT pin. The VT pins provide a center-tap to a termination network for maximum interface flexibility. See “Input Interface Applications” section for more details.
13	GND	Ground. GND pins and exposed pad must be connected to the most negative potential of the device ground.
7, 14	VCC	Positive Power Supply: Bypass with 0.1µF//0.01µF low ESR capacitors and place as close to each VCC pin as possible.

Truth Tables

IN	/IN	EN	Q	/Q
0	1	1	0	1
1	0	1	1	0
X	X	0	0[3]	1[3]

Note:

3. On next negative transition of the input signal (IN).

Absolute Maximum Ratings[4]

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5 to VCC +0.3V
LVDS Output Current (I_{OUT}) ..... +10mA
Input Current
  Source or Sink Current on (I_{VT}) ..... ±2mA
Maximum Operating Junction Temperature ..... 125°C
Lead Temperature (Soldering, 20 s) ..... 260°C
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings[5]

Supply Voltage Range ..... +3.0V to +3.6V
Ambient Temperature (T_A) ..... –40°C to +85°C
Junction Thermal Resistance[6]
  QFN (θJ_A)
    Still-Air ..... 60°C/W
  QFN (ΨJ_B) ..... 33°C/W

Electrical Characteristics[7]

T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power Supply Voltage Range		3.0	3.3	3.6	V
I_{CC}	Power Supply Current	No load, maximum V_{CC}		75	100	mA
R_{IN}	Input Resistance (IN-to-VT)		45	50	55	Ω
$R_{DIFF-IN}$	Differential Input Resistance (IN-to-/IN)		90	100	110	Ω
V_{IH}	Input HIGH Voltage (IN-to-/IN)		0.1		V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage (IN-to-/IN)		–0.3		V_{IH} – 0.1	V
V_{IN}	Input Voltage Swing (IN-to-/IN)	Note 8, see Figure 4.	0.1		V_{CC}	V
V_{DIFF_IN}	Differential Input Voltage	Note 8, see Figure 5.	0.2			V
|IIN|	Input Current (IN, /IN)	Note 8.			45	mA
V_{REF-AC}	Reference Voltage		V_{CC} – 1.525	V_{CC} – 1.425	V_{CC} – 1.325	V

Notes:

4. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
5. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
6. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. ψ_{JB} and θ_{JA} values are determined for a 4-layer board in still-air number, unless otherwise stated.
7. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
8. Due to the internal termination (see "Input Buffer Structure" section) the input current depends on the applied voltages at IN, /IN and VT inputs. Do not apply a combination of voltages that causes the input current to exceed the maximum limit.

LVDS Outputs DC Electrical Characteristics[9]

V_{CC} = 3.3V±10%, R_L = 100Ω across the outputs; T_A = -40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OUT}	Output Voltage Swing	See Figure 4.	250	325		mV
V_{DIFF_OUT}	Differential Output Voltage Swing	See Figure 5.	500	650		mV
V_{OCM}	Output Common Mode Voltage		1.125		1.275	V
ΔV_{OCM}	Change in Common Mode Voltage		–50		50	mV

Note:

9. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

LVTTL/CMOS DC Electrical Characteristics[9]

V_{CC} = 3.3V±10%, T_A = -40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage		0		0.8	V
I_{IH}	Input HIGH Current		–125		30	V
I_{IL}	Input LOW Current				-300	mV

AC Electrical Characteristics[10]

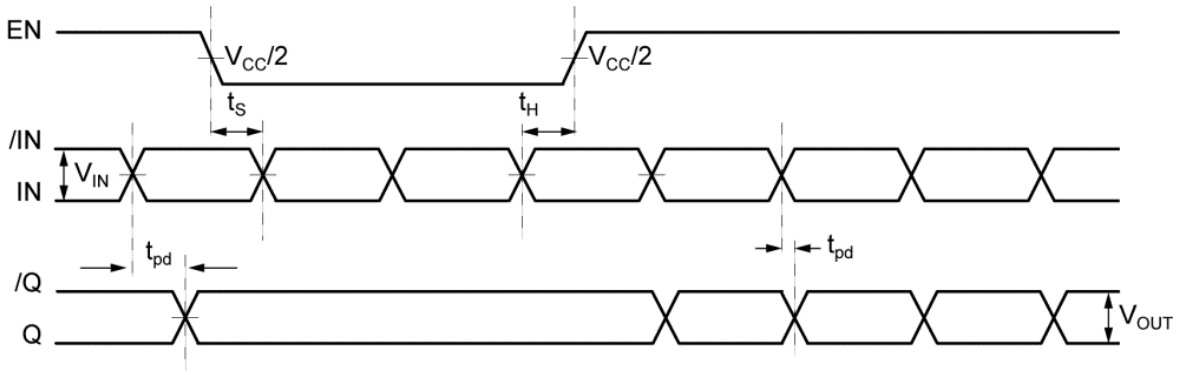
V_{CC} = 3.3V±10%, R_L = 100Ω across the outputs; T_A = -40°C to +85°C unless otherwise stated

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Frequency	V_{OUT} ≥ 200mV	2.0			GHz
t_{pd}	Propagation Delay IN-to-Q	V_{IN} < 400mV	400	500	600	ps
		V_{IN} ≥ 400mV	330	440	530	ps
t_{SKEW}	Within-Device Skew	Note 11		4	20	ps
	Part-to-Part Skew	Note 12			200	ps
t_S	Set-up Time EN to IN, /IN	Note 13	300			ps
t_H	Hold Time EN to IN, /IN	Note 13	500			ps
t_{JITTER}	Additive Jitter	Output = 622MHz Integration Range: 12kHz – 20MHz		98		fs
t_r, t_f	Output Rise/Fall Times (20% to 80%)	At full output swing.	60	110	190	ps

Notes:

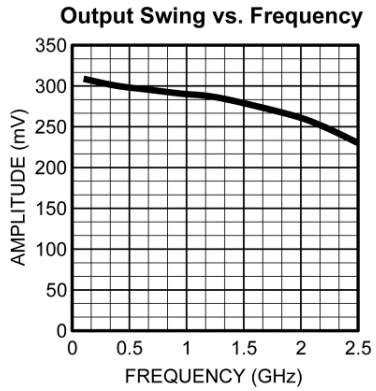
10. High-frequency AC parameters are guaranteed by design and characterization.
11. Within device skew is measured between two different outputs under identical input transitions.
12. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.
13. Set-up and hold times apply to synchronous applications that intend to enable/disable before the next clock cycle. For asynchronous applications, set-up and hold times do not apply.

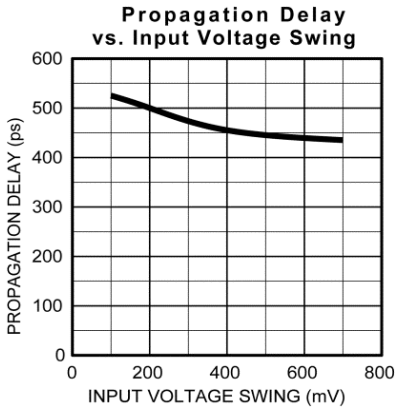
Timing Diagram



Typical Characteristics

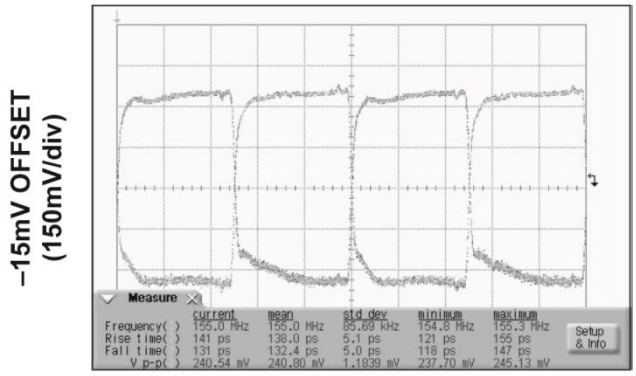
V_{CC} = 3.3V, GND = 0V, V_{IN} = 400mV, R_L = 100Ω across the outputs; T_A = 25°C unless otherwise stated.





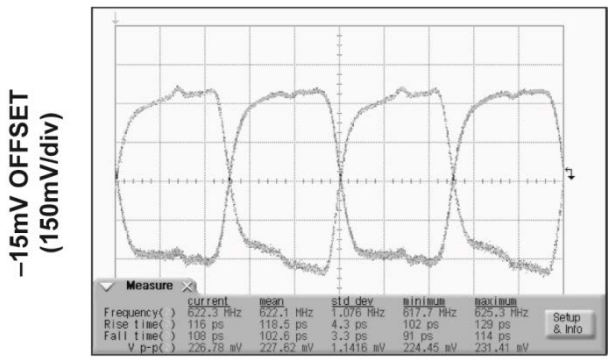
Functional Characteristics

155MHz Output



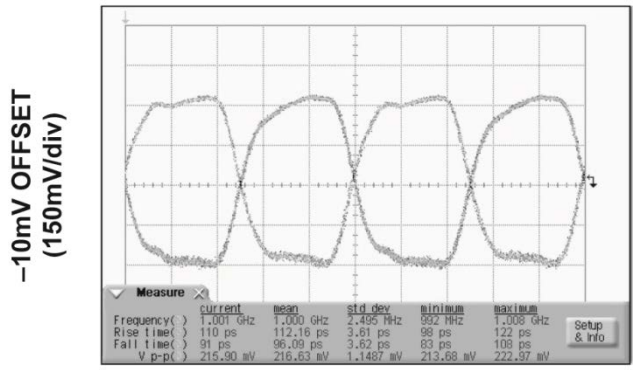
Time (1.29ps/div)

622MHz Output



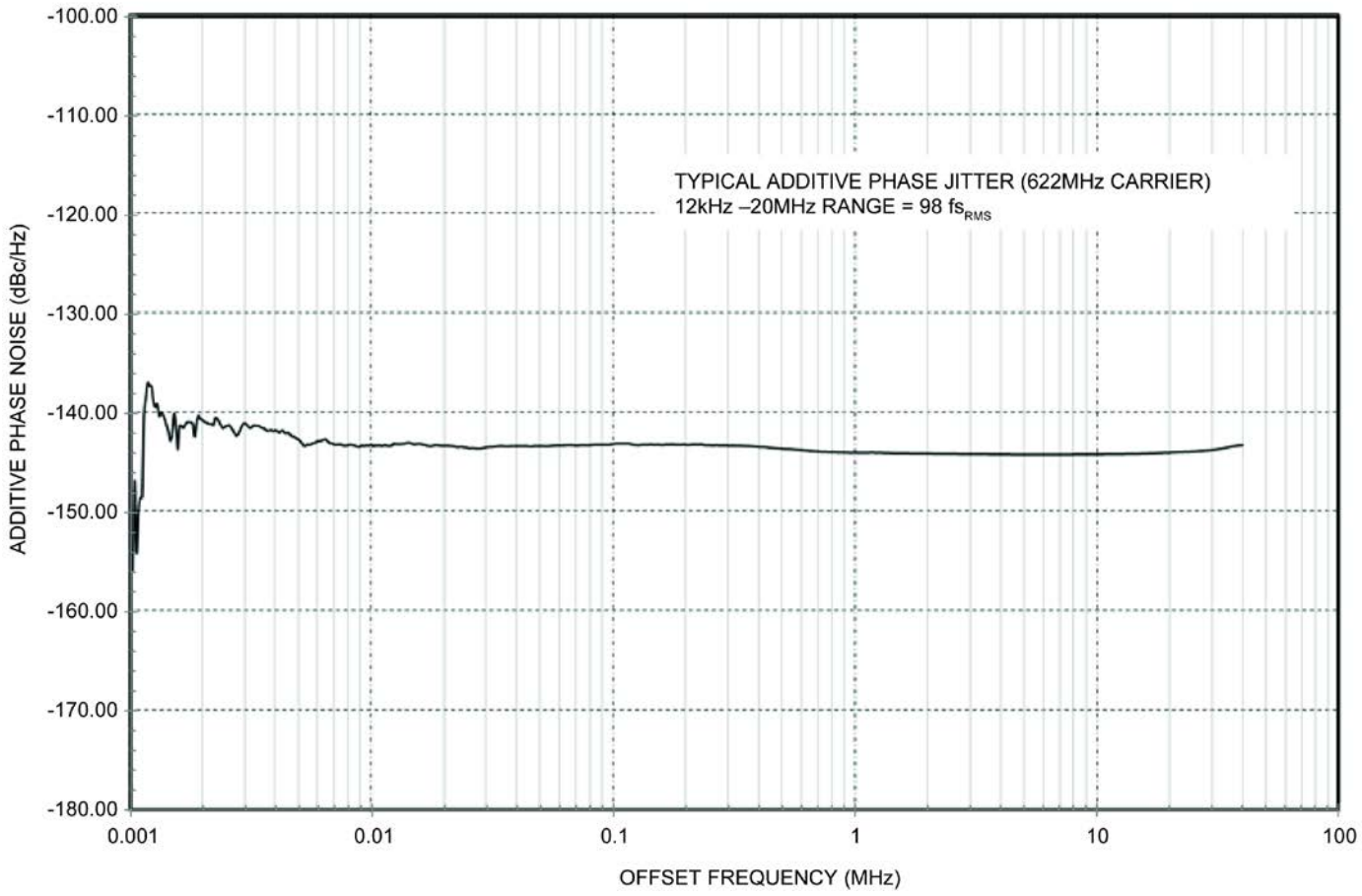
Time (321.9ps/div)

1GHz Output



Time (200ps/div)

Additive Phase Noise Plot



Input Stage

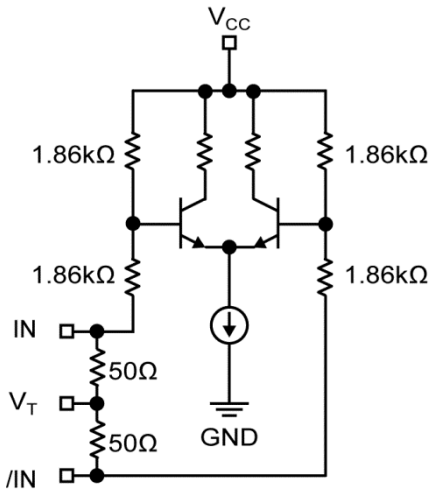


Figure 1. Simplified Differential Input Buffer

LVDS Outputs

LVDS specifies a small swing of 325mV typical, on a nominal 1.20V common mode above ground. The common-mode voltage has tight limits to permit large variations in ground noise between a LVDS driver and receiver.

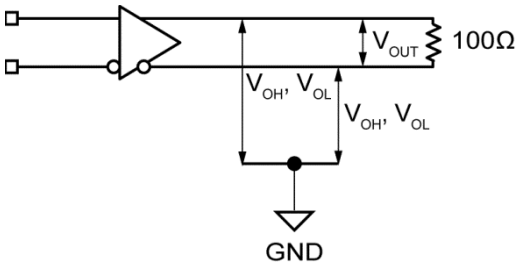


Figure 2. LVDS Differential Measurement

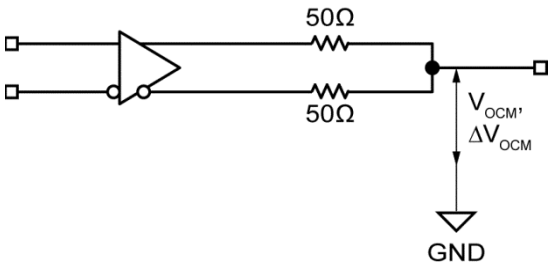


Figure 3. LVDS Common Mode Measurement

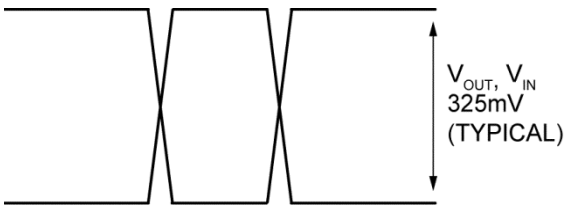


Figure 4. Single-Ended Swing

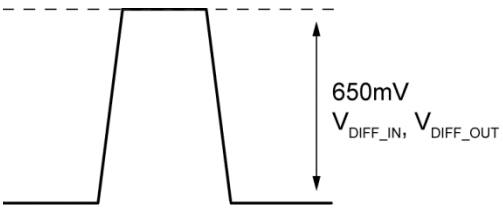


Figure 5. Differential Swing

Input Interface Applications

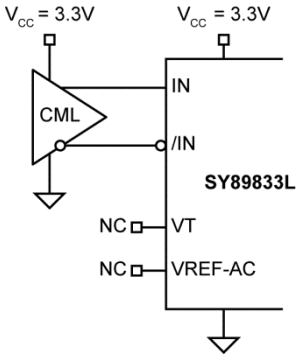


Figure 6. DC-Coupled CML Input Interface

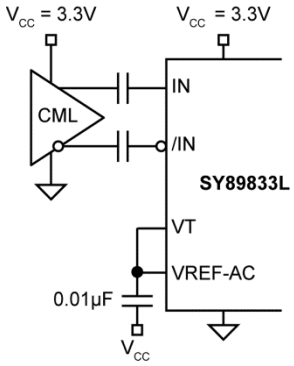


Figure 7. AC-Coupled CML Input Interface

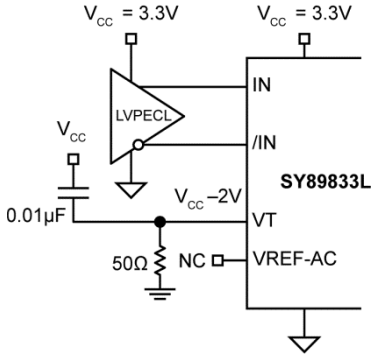


Figure 8. DC-Coupled LVPECL Input Interface

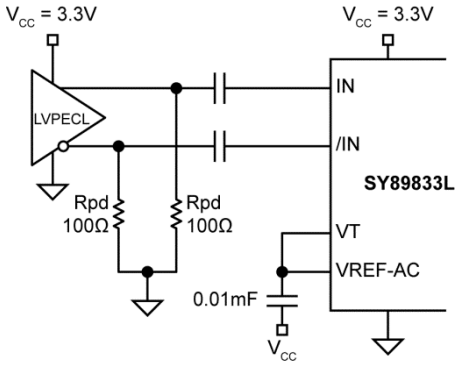


Figure 9. AC-Coupled LVPECL Input Interface

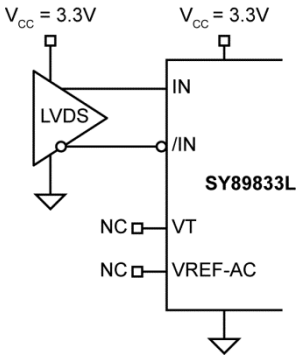


Figure 10. LVDS Input Interface

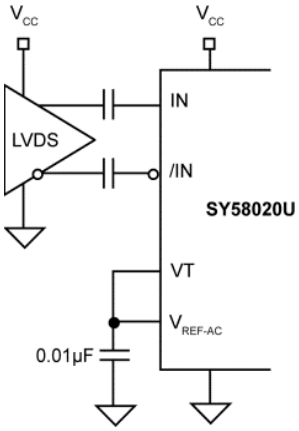
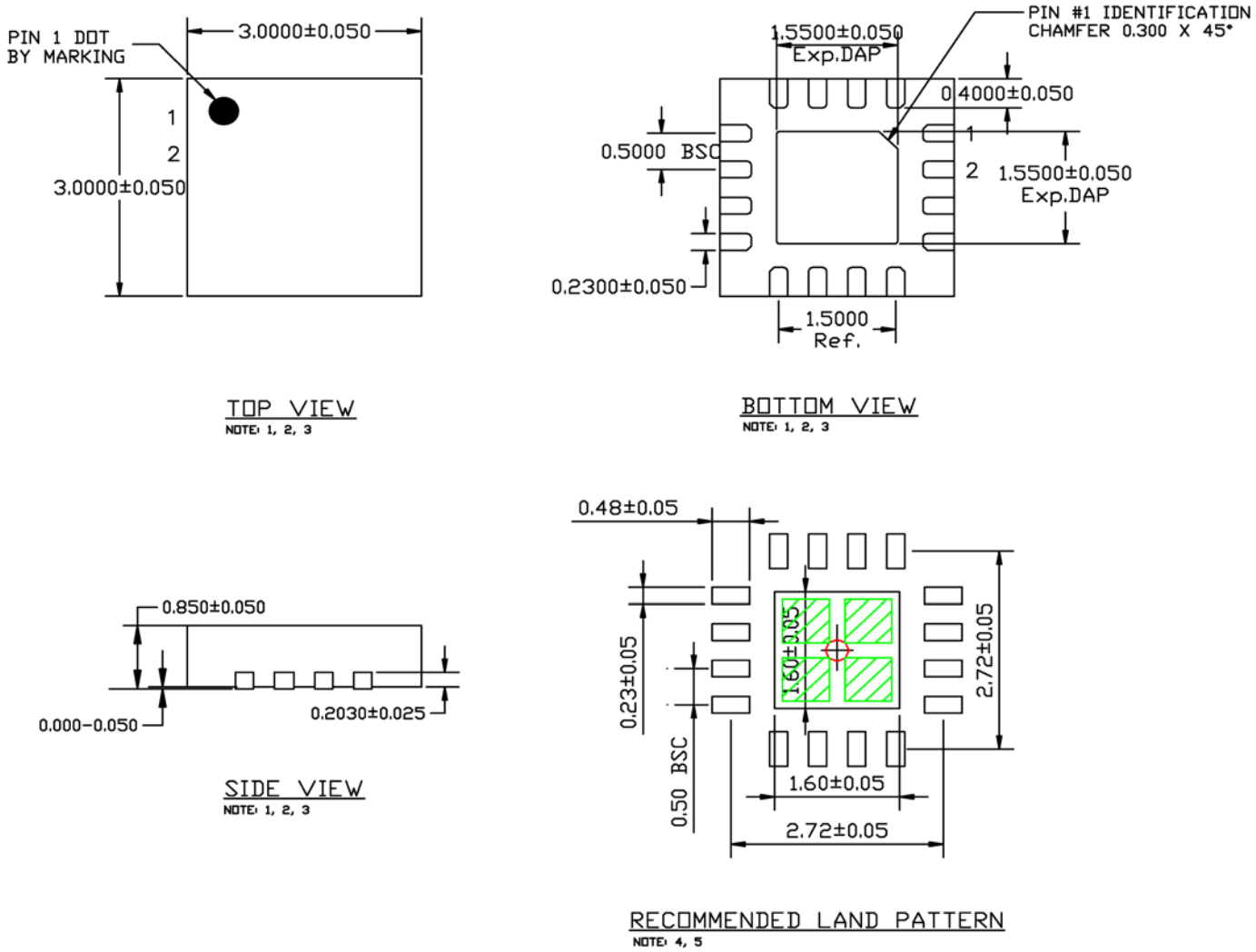


Figure 11. AC-Coupled LVDS Input Interface

Note: Be certain that the LVDS driver can be AC-coupled.

hbwhelp@micrel.com or (408) 955-1690

Package Information[14]



NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.3M IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) Indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.60x0.60 MM IN SIZE, 0.20 MM SPACING.

16-Pin 3mm × 3mm QFN (MM)

Note:

14. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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