AN-2051 LM5050-2EVAL Evaluation Board

1 Introduction

The LM5050-2 evaluation board is designed to demonstrate the capabilities of the LM5050-2 OR-ing Diode Controller. It is intended for evaluation of the functions of the LM5050-2. One high side N-channel power MOSFET is used. The LM5050-2 evaluation board schematic is shown in Figure 5. The evaluation board is designed to highlight applications with a small solution size. For more information about the LM5050-2 functional and electrical characteristics, see the *LM5050-2 High Side OR-ing FET Controller* SNVS679) data sheet.

2 Operating Range

- Minimum Input Voltage, 6V
- Maximum Input Voltage, 50V
- Output Current Range: 0A to 15A
- Ambient Temperature Range 0°C to 50°C
- Board Size 1.50 inches x 2.25 inches

The load current capability is limited at 15A by the ratings of the terminals and the PCB copper area and weight. The PCB layout has not been tested for currents above 15A, so this should only be done with some degree of caution.

The maximum input voltage is limited by the breakdown voltage rating of both D1 and D2.

Typical evaluation board performance and characteristics curves are shown in Figure 1 through Figure 3. The PCB layout is shown in Figure 4 and Figure 5. Test points are provided for optional control and signal monitoring.

3 Evaluation Board Start-Up

Before applying power to the LM5050-2 evaluation board, all external connections should be verified. The external power supply must be turned off and connected with proper polarity to the VIN, VOUT, and GND terminals. Under basic evaluation conditions the nPGD, V_{LOGIC}, and Off test points are left open.

The evaluation board will be in the normal operating mode when power is applied. The Off terminal is used only when there is a desire to disable normal operation and invoke the MOSFET test comparator.

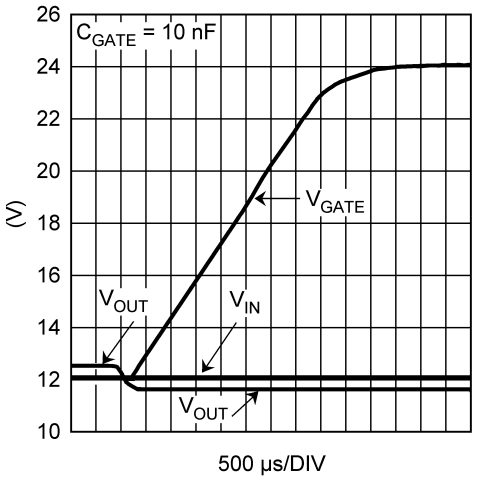

Figure 1. Forward Waveforms

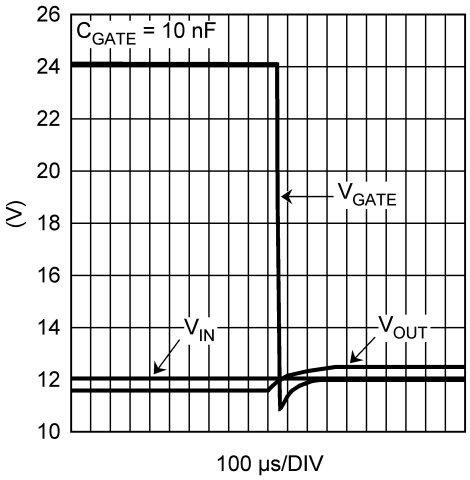

Figure 2. Reverse Waveforms

4 Inductive Kick-Back Protection

Diode D1 and capacitor C1 (as do diode D2 and capacitor C2) serve as inductive kick-back protection to limit negative transient voltage spikes generated on the input when the input supply voltage is abruptly taken to zero volts.

5 Off Test Point

The Off test point provided on the LM5050-2 evaluation board is used to control the LM5050-2 operation. The Off test point is connected directly to the LM5050-2 OFF pin. For more details, see the LM5050 data sheet.

To enable the LM5050-2 apply a voltage less than 0.8V to the Off test point, connect the Off test point to GND, or leave the Off test point open (default). If the Off test point is left open, the LM5050-2 OFF pin internal pull-down will ensure that the LM5050-2 becomes operational.

To disable the LM5050-2, apply a voltage greater than 2.0V to the Off test point.

6 V_{LOGIC} Test Point

An external voltage is applied to the V_{LOGIC} test point so that the logical output of the Status test point can be evaluated. The V_{LOGIC} pin is connected to the LM5050-2 nFGD pin through a 10 kΩ pull-up resistor. The voltage applied to the V_{LOGIC} test point should be between 3.0V and 5.5V.

7 Status (nPGD) Test Point

The nPGD test point is wired directly to the LM5050-2 open-drain nFGD pin (device pin 1), with pull-up bias from the V_{LOGIC} test point through a 10 kΩ pull-up resistor.

While the Off test point is low, or open, the nFGD pin will be in a high impedance state and the nPGD test point voltage will be at a logic high.

When the Off test point is high, the MOSFET Gate drive is OFF. If the MOSFET is normal, current will begin flowing through the body diode and the voltage difference between the IN pin and the OUT pin will be greater than the $V_{DS(TST)}$ threshold of typically 350 mV. In this case the nFGD pin will go to a low impedance stage and the nPGD test point voltage will be at a logic low..

If the MOSFET is shorted, the voltage difference between the IN pin and the OUT pin will be less than the $V_{DS(TST)}$ threshold of typically 350 mV. In this case the nFGD pin will remain in a high impedance state and the nPGD test point voltage will remain at a logic high.

There are several factors that may prevent the nFGD pin from going to a logic low in an otherwise good application. If there is a redundant, parallel, supply in operation, that supply may hold the OUT pin voltage close enough to the IN pin voltage that the $V_{DS(TST)}$ threshold is not exceeded. Additionally, a high output capacitance value, or a low load current, may require that a significant amount of time be allowed for the output capacitance to discharge to the point where the $V_{DS(TST)}$ threshold is exceeded and the nFGD pin goes low.

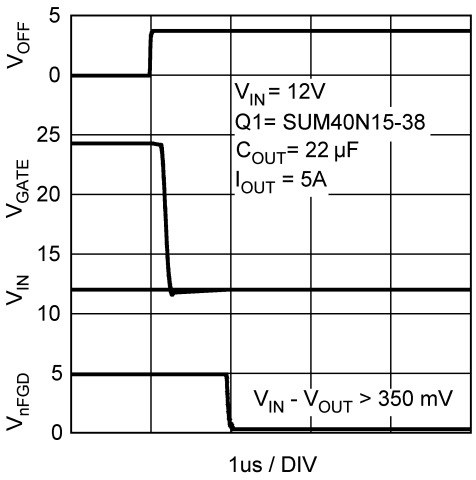

Figure 3. MOSFET Test, No Fault

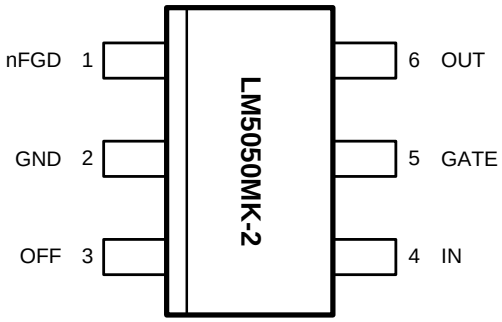

Figure 4. Connection Diagram

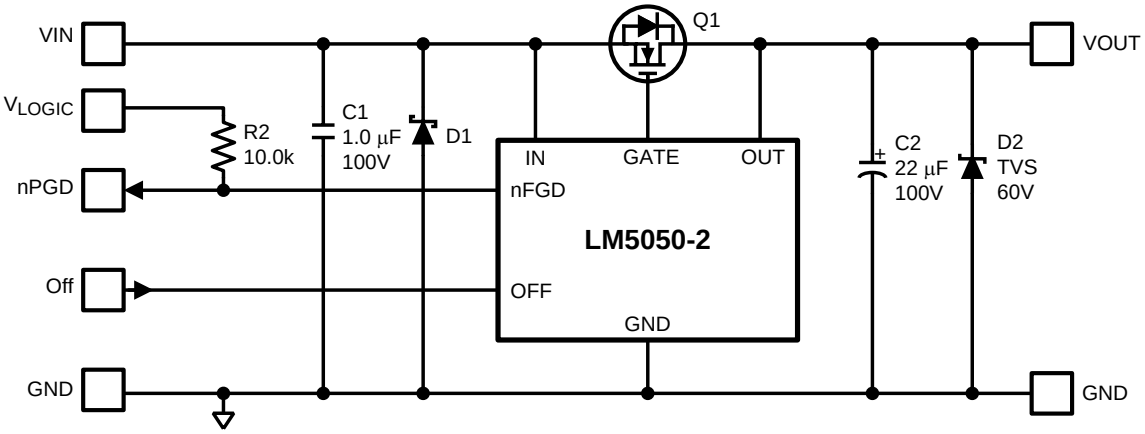

Figure 5. Schematic Diagram

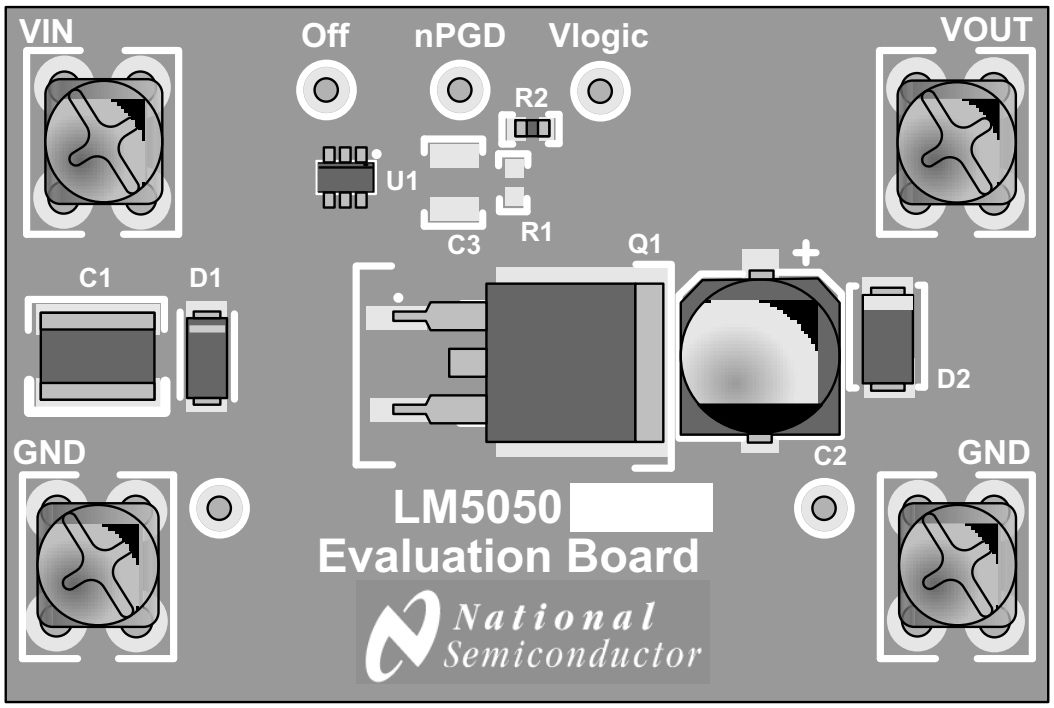

Figure 6. Component Placement

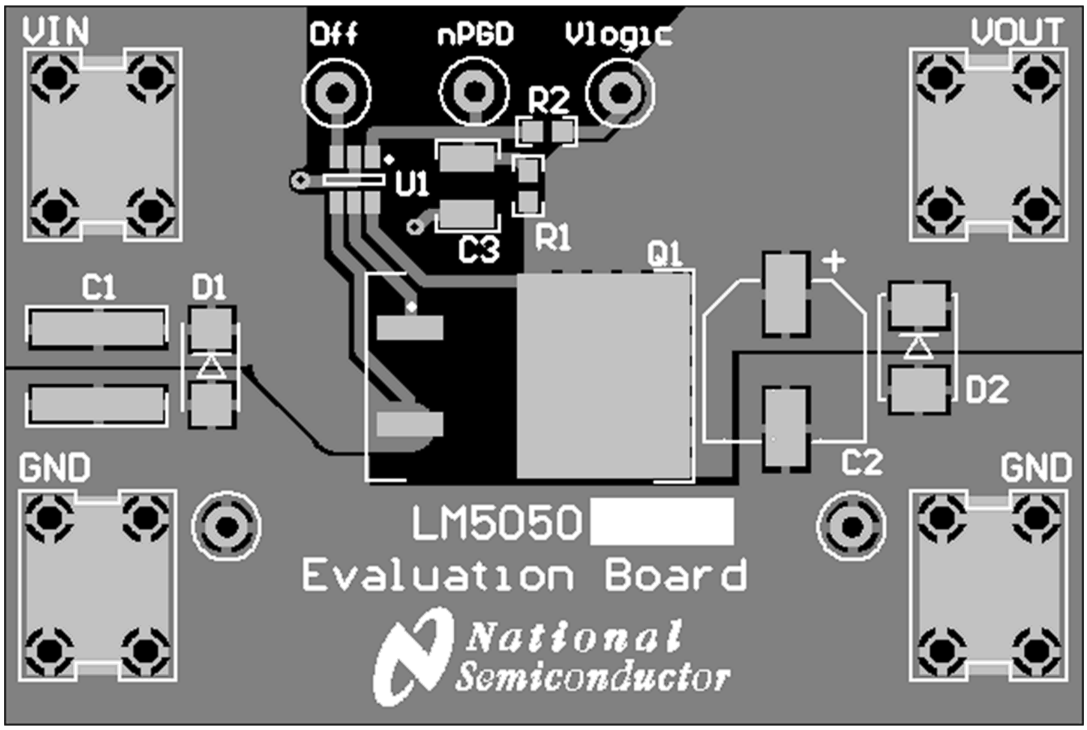

Figure 7. Evaluation Board, Top Side (Component)

Figure 8. Evaluation Board, Bottom Side

8 Bill of Materials

Table 1. Bill of Materials

ID	Description	Manufacturer	Mfgr Part Number
U1	IC; Ideal OR-ing Diode Controller	Texas Instruments	LM5050
C1	Capacitor: MLCC; 1.0µF; ±10%; 100V; X7R; 1825	Vishay/Vitramon	VJ1825Y105KBBAT4X
C2	Capacitor: 22 µF; ±20%; 100V; Aluminum Electrolytic; SMT	Panasonic/ECG	EEE-HA2A220P
C3	Not Installed	-	-
D1	Diode: Schottky Barrier Rectifier; 1A: 60V; SMA	ON Semiconductor	SS16T3G
		Micro Commercial Components	SS16-TP
D2	Diode: TVS; Unidirectional; 600W; 60V; SMB	Diodes Inc	SMBJ60A-13-F
Q1	MOSFET: N-Channel; 100V; 40A; 0.025Ω; D^2PAK	Vishay/Siliconix	SUM40N10-30-E3
R1	Not Installed	-	-
R2	Resistor: 10.0 kΩ; 0.10W; ±1%; 100ppm; Thick Film; 0603	Vishay/Dale	CRCW060310K0FKEA
		ROHM Semiconductor	MCR03EZPFX1002
VIN	Terminal: 6-32 Screw; Vertical; Snap-In PCB Mount; 15A	Keystone Electronics	7693
VOUT			
GND			
GND			
Off	Test Point Terminal: 0.040in Dia Mtg Hole; White	Keystone Electronics	5012
nPGD			
V_{LOGIC}			
GND			
GND			

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