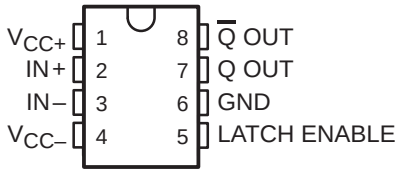
- **Ultrafast Operation . . . 7.6 ns (Typ)**
- **Low Positive Supply Current 10.6 mA (Typ)**
- **Operates From a Single 5-V Supply or From a Split ±5-V Supply**
- **Complementary Outputs**
- **Low Offset Voltage**
- **No Minimum Slew Rate Requirement**
- **Output Latch Capability**
- **Functional Replacement to the LT1016**

D AND PW PACKAGE
(TOP VIEW)



description

The TL3016 is an ultrafast comparator designed to interface directly to TTL logic while operating from either a single 5-V power supply or dual ±5-V supplies. It features extremely tight offset voltage and high gain for precision applications. It has complementary outputs that can be latched using the LATCH ENABLE terminal. Figure 1 shows the positive supply current of this comparator. The TL3016 only requires 10.6 mA (typical) to achieve a propagation delay of 7.6 ns.

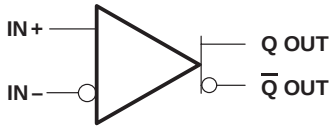
The TL3016 is a pin-for-pin functional replacement for the LT1016 comparator, offering higher speed operation but consuming half the power.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		CHIP FORM‡ (Y)
	SMALL OUTLINE† (D)	TSSOP (PW)	
0°C to 70°C	TL3016CD	TL3016CPWLE	TL3016Y
–40°C to 85°C	TL3016ID	TL3016IPWLE	—

† The PW packages are available left-ended taped and reeled only.
‡ Chip forms are tested at T_A = 25°C only.

symbol (each comparator)



POSITIVE SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

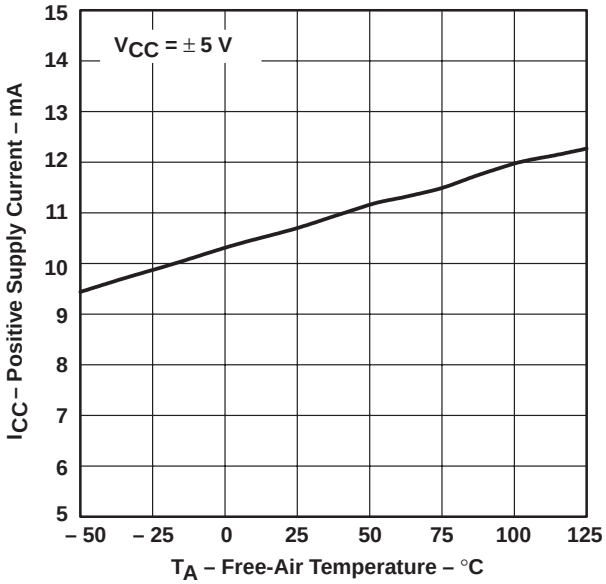
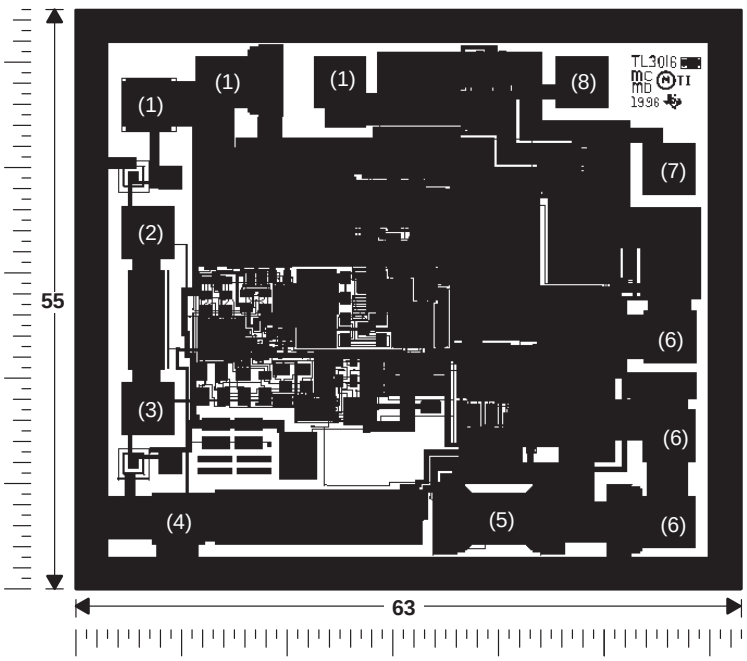


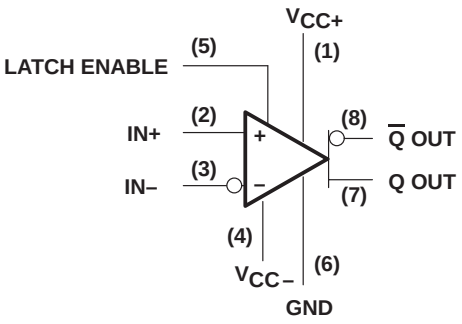
Figure 1

TL3016Y chip information

This chip displays characteristics similar to the TL3016C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 10 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

TERMINALS 1 AND 6 CAN BE CONNECTED TO MULTIPLE PADS.

COMPONENT COUNT	
Bipolars	53
MOSFETs	49
Resistors	46
Capacitors	14

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . – 7 V to 7 V
Differential input voltage, V_{ID} (see Note 2) . . . . . 7 V
Input voltage range, V_I . . . . . 7 V
Input voltage, V_I (LATCH ENABLE) . . . . . 7 V
Output current, I_O . . . . . ± 20 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN–.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
PW	525 mW	4.2 mW/°C	336 mW

electrical characteristics at specified operating free-air temperature, V_{DD} = ±5 V, V_{LE} = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	TL3016C			TL3016I			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	T_A = 25°C		0.5	3		0.5	3	mV
		T_A = full range			3.5			3.5	
α_{VIO}	Temperature coefficient of input offset voltage			–4.8			–4.5		µV/°C
I_{IO}	Input offset current	T_A = 25°C		0.1	0.6		0.1	0.6	µA
		T_A = full range			0.9			1.3	
I_{IB}	Input bias current	T_A = 25°C		6	10		6	10	µA
		T_A = full range			10			10	
V_{ICR}	Common-mode input voltage range	V_{DD} = ±5 V	–3.75		3.5	–3.75		3.5	V
		V_{DD} = 5 V	1.25		3.5	1.25		3.5	
CMRR	Common-mode rejection ratio	–3.75 ≤ V_{IC} ≤ 3.5 V, T_A = 25°C	80	97		80	97		dB
k_{SVR}	Supply-voltage rejection ratio	Positive supply: 4.6 V ≤ +V_{DD} ≤ 5.4 V, T_A = 25°C	60	72		60	72		dB
		Negative supply: –7 V ≤ –V_{DD} ≤ –2 V, T_A = 25°C	80	100		80	100		
V_{OL}	Low-level output voltage	$I_{(sink)}$ = 4 mA, V+ ≤ 4.6 V, T_A = 25°C		500	600		500	600	mV
		$I_{(sink)}$ = 10 mA, V+ ≤ 4.6 V, T_A = 25°C		750			750		
V_{OH}	High-level output voltage	V+ ≤ 4.6 V, I_O = 1 mA, T_A = 25°C	3.6	3.9		3.6	3.9		V
		V+ ≤ 4.6 V, I_O = 10 mA, T_A = 25°C	3.4	3.7		3.4	3.7		
I_{DD}	Positive supply current	T_A = full range		10.6	12.5		10.6	12.5	mA
	Negative supply current		–1.8	–1.3		–2.4	–1.3		
V_{IL}	Low-level input voltage (LATCH ENABLE)				0.8			0.8	V
V_{IH}	High-level input voltage (LATCH ENABLE)		2			2			V
I_{IL}	Low-level input current (LATCH ENABLE)	V_{LE} = 0		0	1		0	1	µA
		V_{LE} = 2 V		24	39		24	45	

† Full range for the TL3016C is T_A = 0°C to 70°C. Full range for the TL3016I is T_A = –40°C to 85°C.
‡ All typical values are measures with T_A = 25°C.

switching characteristics, $V_{DD} = \pm 5$ V, $V_{LE} = 0$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL3016C			TL3016I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd1}	Propagation delay time‡	ΔV_I = 100 mV, V_{OD} = 5 mV	T_A = 25°C		7.8	10		7.8	10	ns
			T_A = full range		7.8	11.2		7.8	12.2	
		ΔV_I = 100 mV, V_{OD} = 20 mV	T_A = 25°C		7.6	10		7.6	10	
			T_A = full range		7.6	11.2		7.6	12.2	
$t_{sk(p)}$	Pulse skew ($\lvert t_{pd+} - t_{pd-} \rvert$)	ΔV_I = 100 mV, T_A = 25°C	V_{OD} = 5 mV,		0.5			0.5		ns
t_{su}	Setup time, LATCH ENABLE				2.5			2.5		ns

† Full range for the TL3016C is 0°C to 70°C. Full range for the TL3016I is –40°C to 85°C.

‡ t_{pd1} cannot be measured in automatic handling equipment with low values of overdrive. The TL3016 is 100% tested with a 1-V step and 500-mV overdrive at T_A = 25°C only. Correlation tests have shown that t_{pd1} limits given can be ensured with this test, if additional dc tests are performed to ensure that all internal bias conditions are correct. For low overdrive conditions, V_{OS} is added to the overdrive.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_{CC}	Positive supply current	vs Input voltage	2
		vs Frequency	3
		vs Free-air temperature	4
I_{CC}	Negative supply current	vs Free-air temperature	5
t_{pd}	Propagation delay time	vs Overdrive voltage	6
		vs Supply voltage	7
		vs Input impedance	8
		vs Load capacitance	9
		vs Free-air temperature	10
V_{IC}	Common-mode input voltage	vs Free-air temperature	11
	Input threshold voltage (LATCH ENABLE)	vs Free-air temperature	12
V_O	Output voltage	vs Output source current	13
		vs Output sink current	14
I_I	Input current (LATCH ENABLE)	vs Input voltage	15

TYPICAL CHARACTERISTICS

POSITIVE SUPPLY CURRENT vs INPUT VOLTAGE

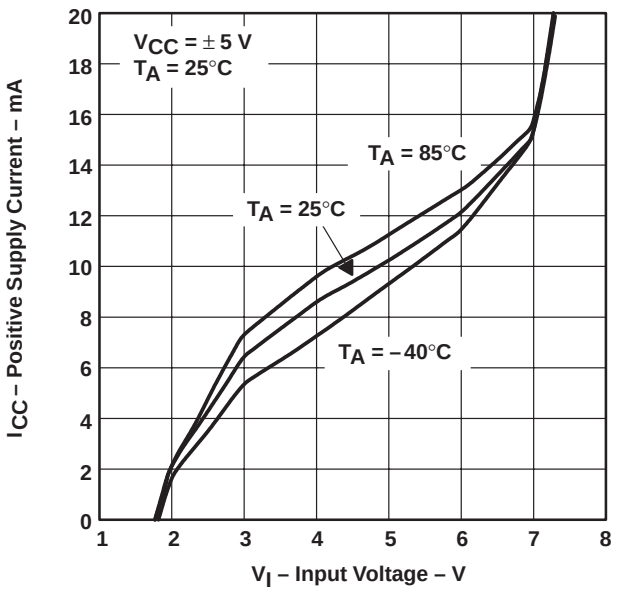


Figure 2

POSITIVE SUPPLY CURRENT vs FREQUENCY

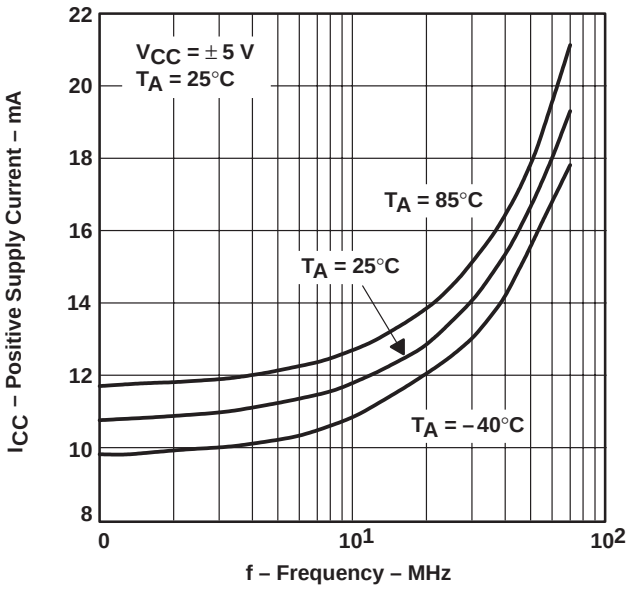


Figure 3

POSITIVE SUPPLY CURRENT vs FREE-AIR TEMPERATURE

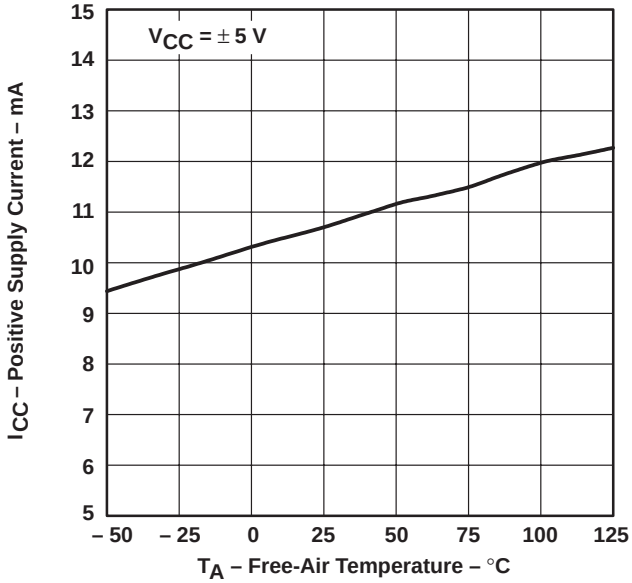


Figure 4

NEGATIVE SUPPLY CURRENT vs FREE-AIR TEMPERATURE

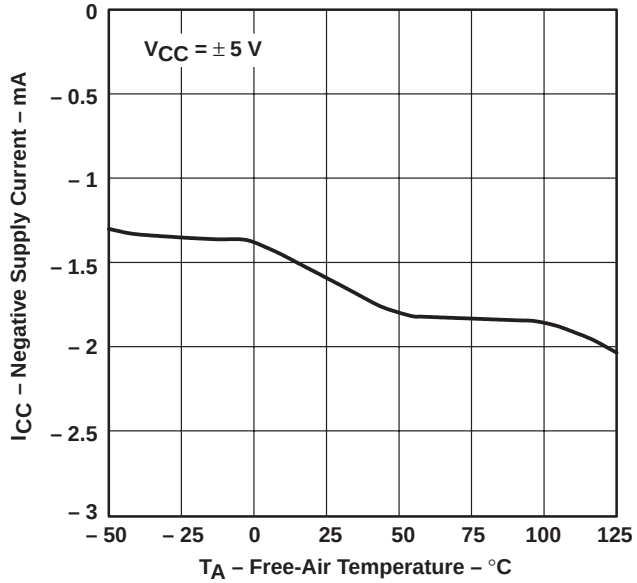


Figure 5

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME vs OVERDRIVE VOLTAGE

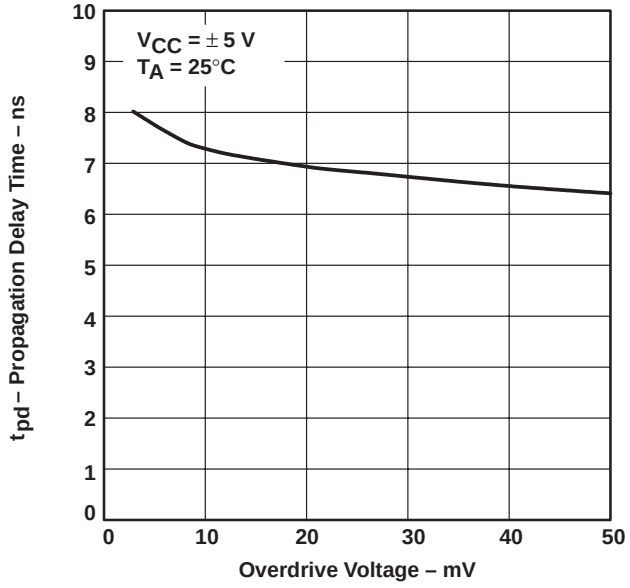


Figure 6

PROPAGATION DELAY TIME vs SUPPLY VOLTAGE

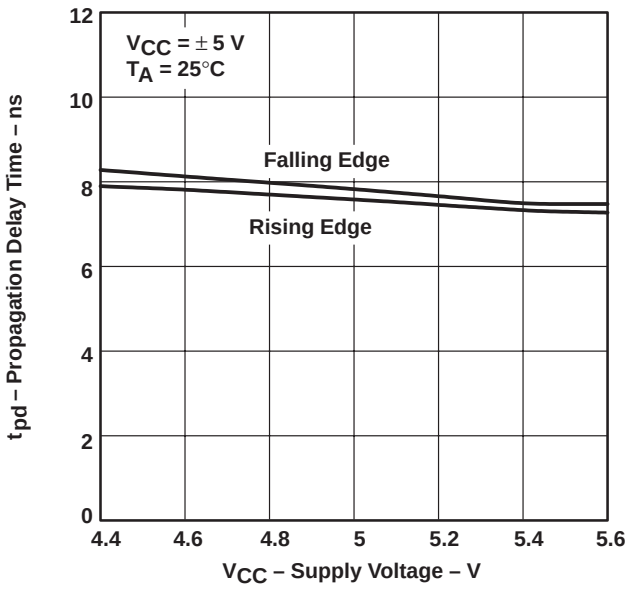


Figure 7

PROPAGATION DELAY TIME vs INPUT IMPEDANCE

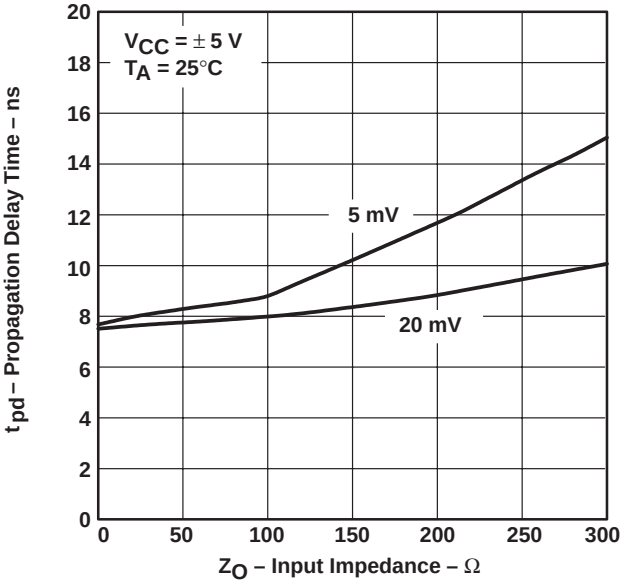


Figure 8

PROPAGATION DELAY TIME vs LOAD CAPACITANCE

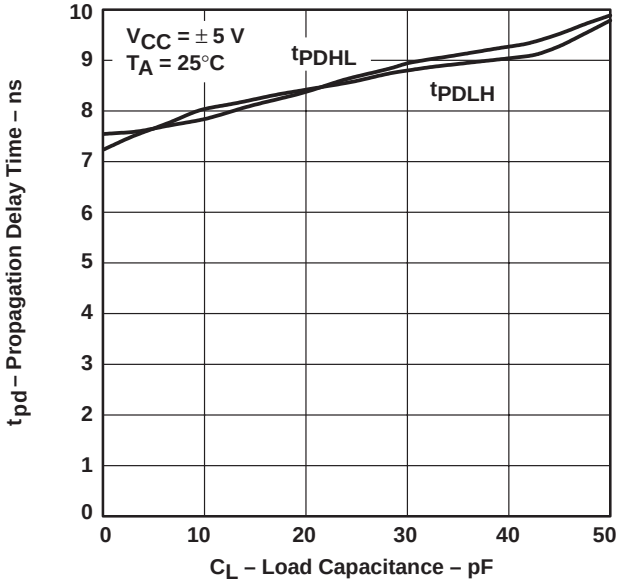


Figure 9

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

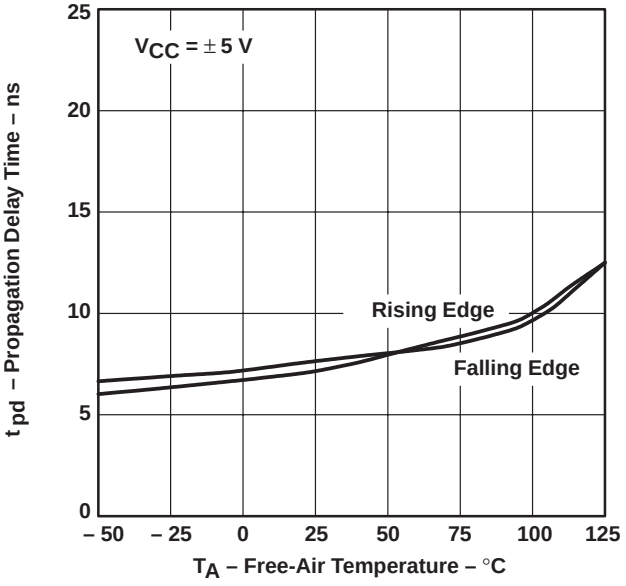


Figure 10

COMMON-MODE INPUT VOLTAGE vs FREE-AIR TEMPERATURE

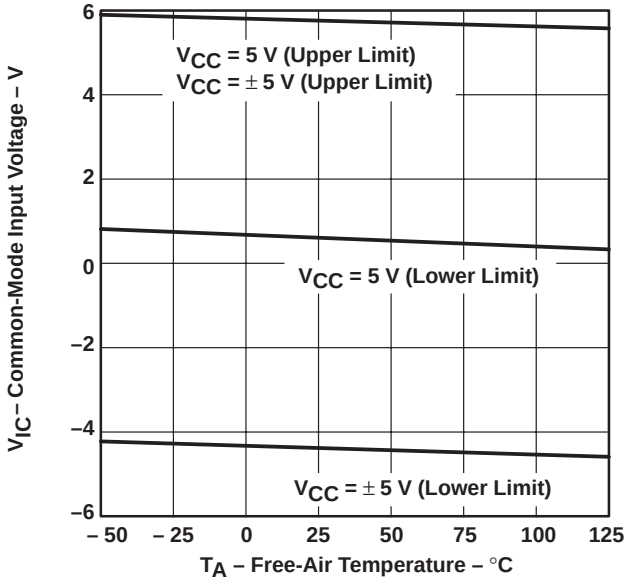


Figure 11

INPUT THRESHOLD VOLTAGE (LATCH ENABLE) vs FREE-AIR TEMPERATURE

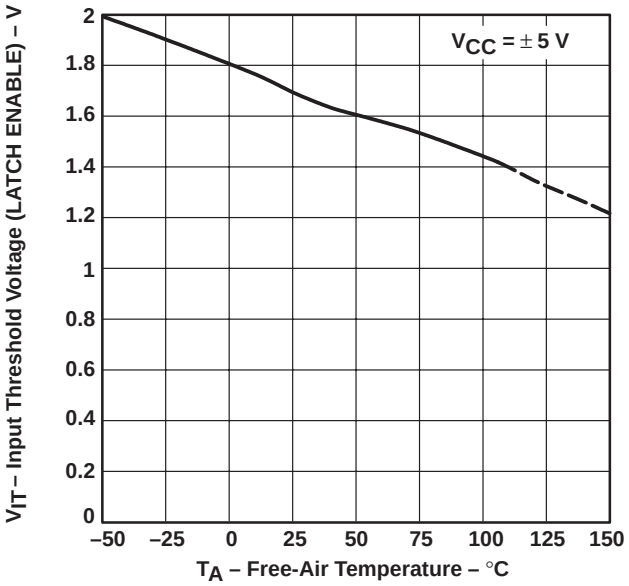


Figure 12

OUTPUT VOLTAGE vs OUTPUT SOURCE CURRENT

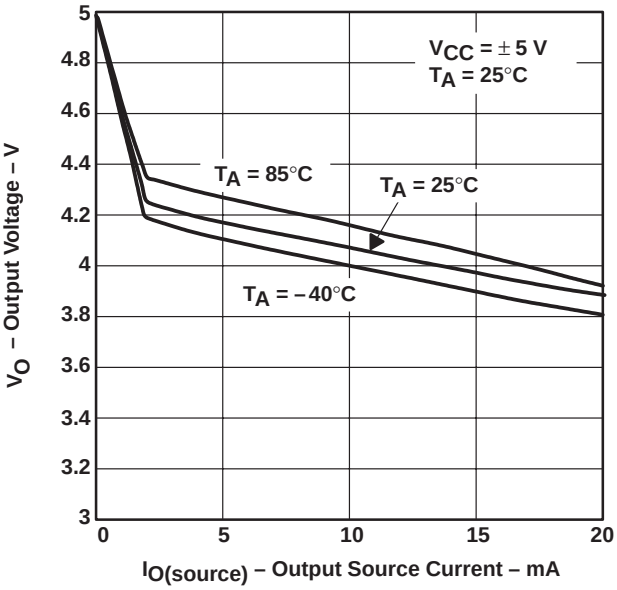


Figure 13

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs OUTPUT SINK CURRENT

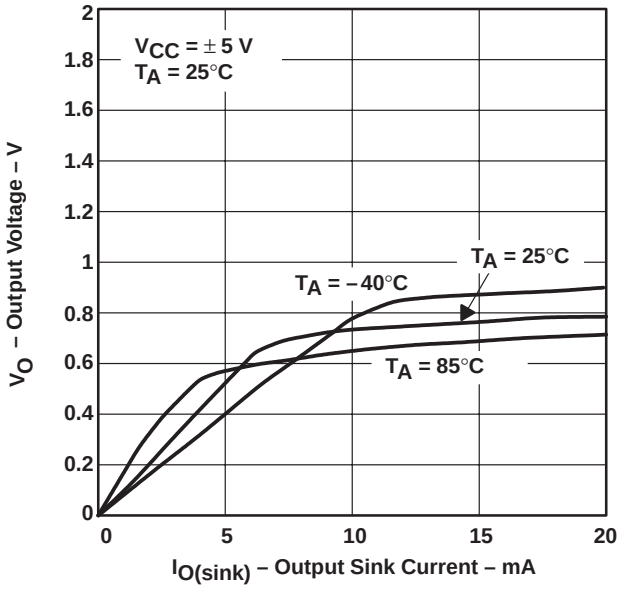


Figure 14

INPUT CURRENT (LATCH ENABLE) vs INPUT VOLTAGE

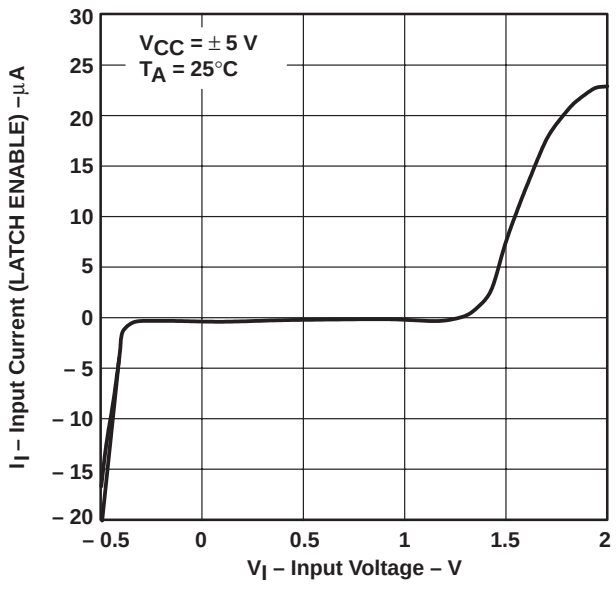


Figure 15

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL3016CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	3016C	Samples
TL3016CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	3016C	Samples
TL3016CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	3016C	Samples
TL3016CPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T3016	Samples
TL3016CPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T3016	Samples
TL3016ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	3016I	Samples
TL3016IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	3016I	Samples
TL3016IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	3016I	Samples
TL3016IPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z3016	Samples
TL3016IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z3016	Samples
TL3016IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z3016	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

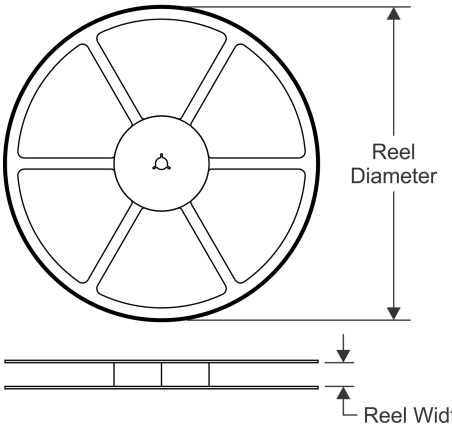
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

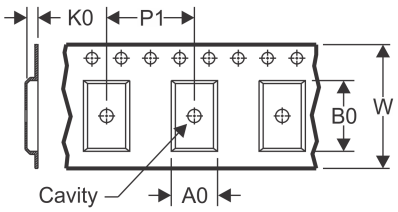
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

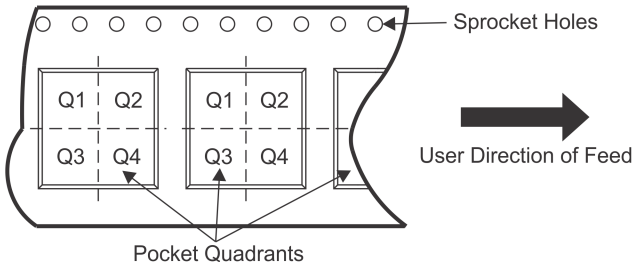


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

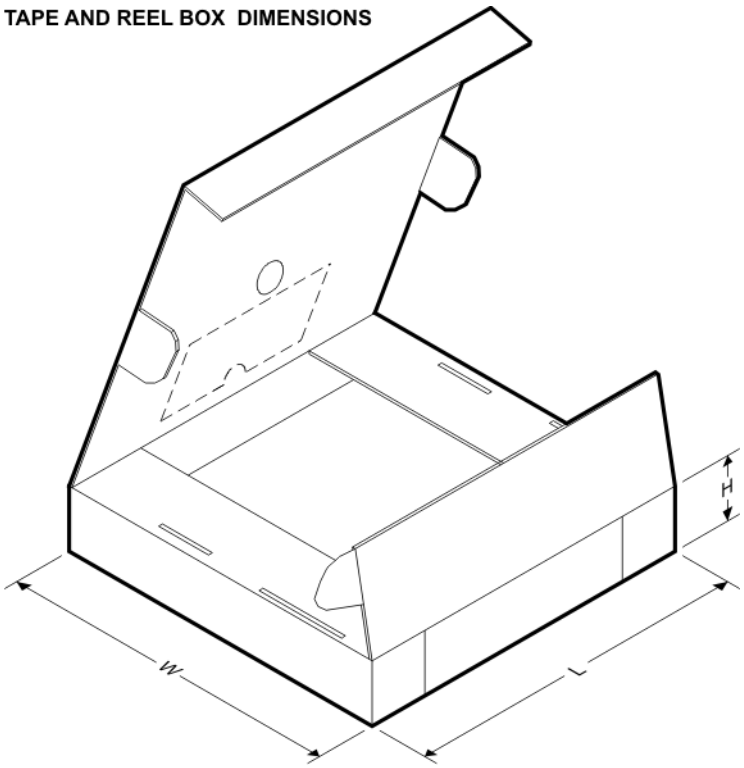
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

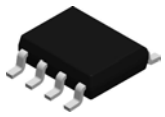
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL3016CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL3016CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL3016IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL3016IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL3016CDR	SOIC	D	8	2500	350.0	350.0	43.0
TL3016CPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TL3016IDR	SOIC	D	8	2500	350.0	350.0	43.0
TL3016IPWR	TSSOP	PW	8	2000	367.0	367.0	35.0

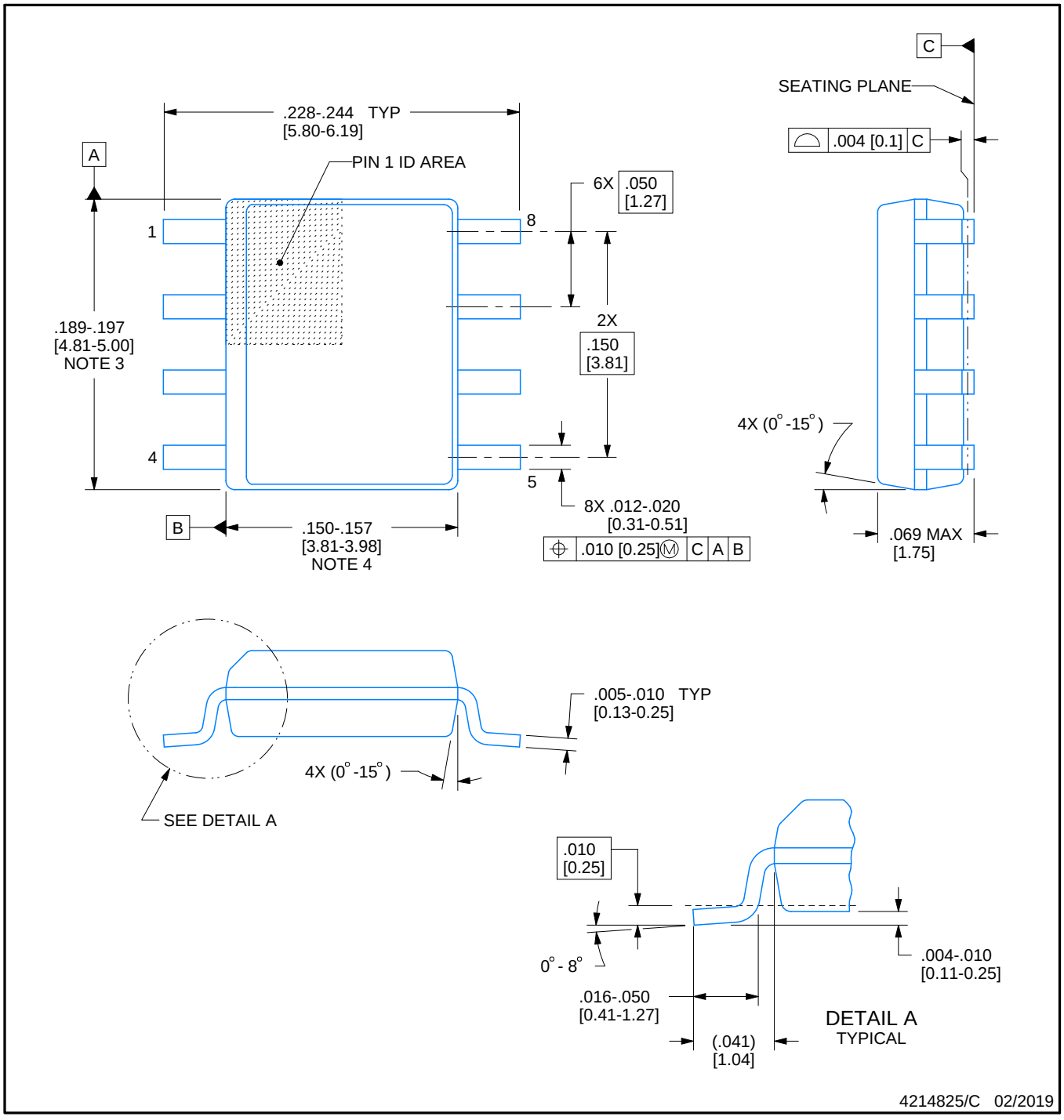


PACKAGE OUTLINE

D0008A

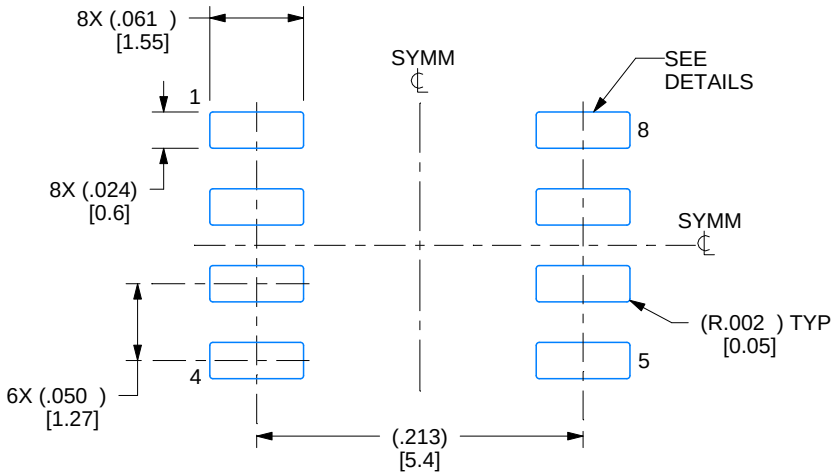
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

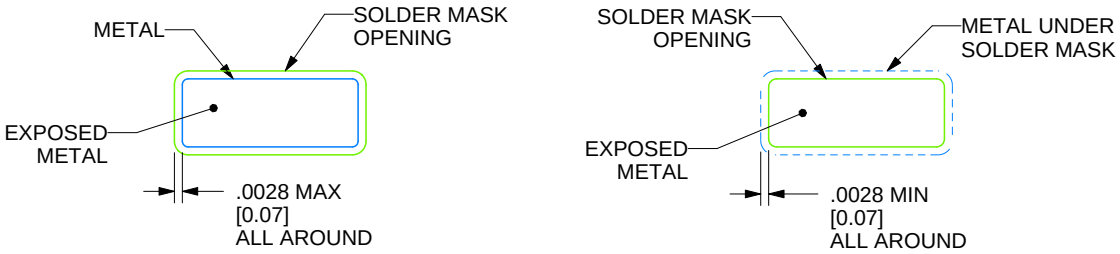


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

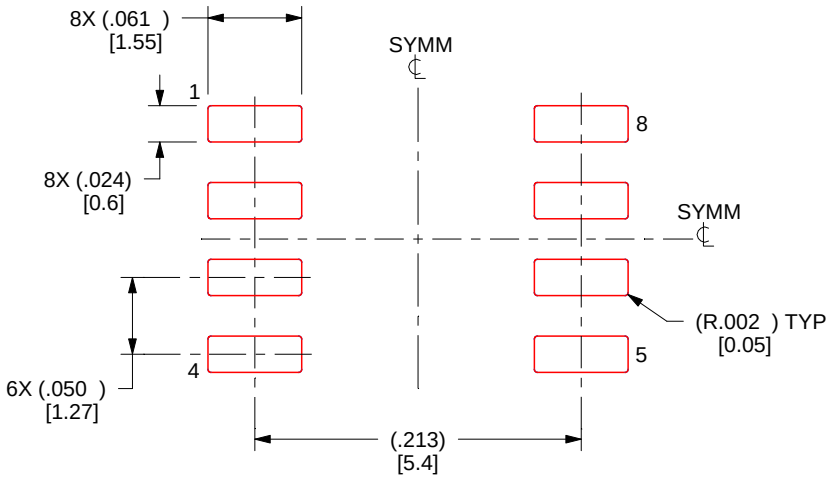
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

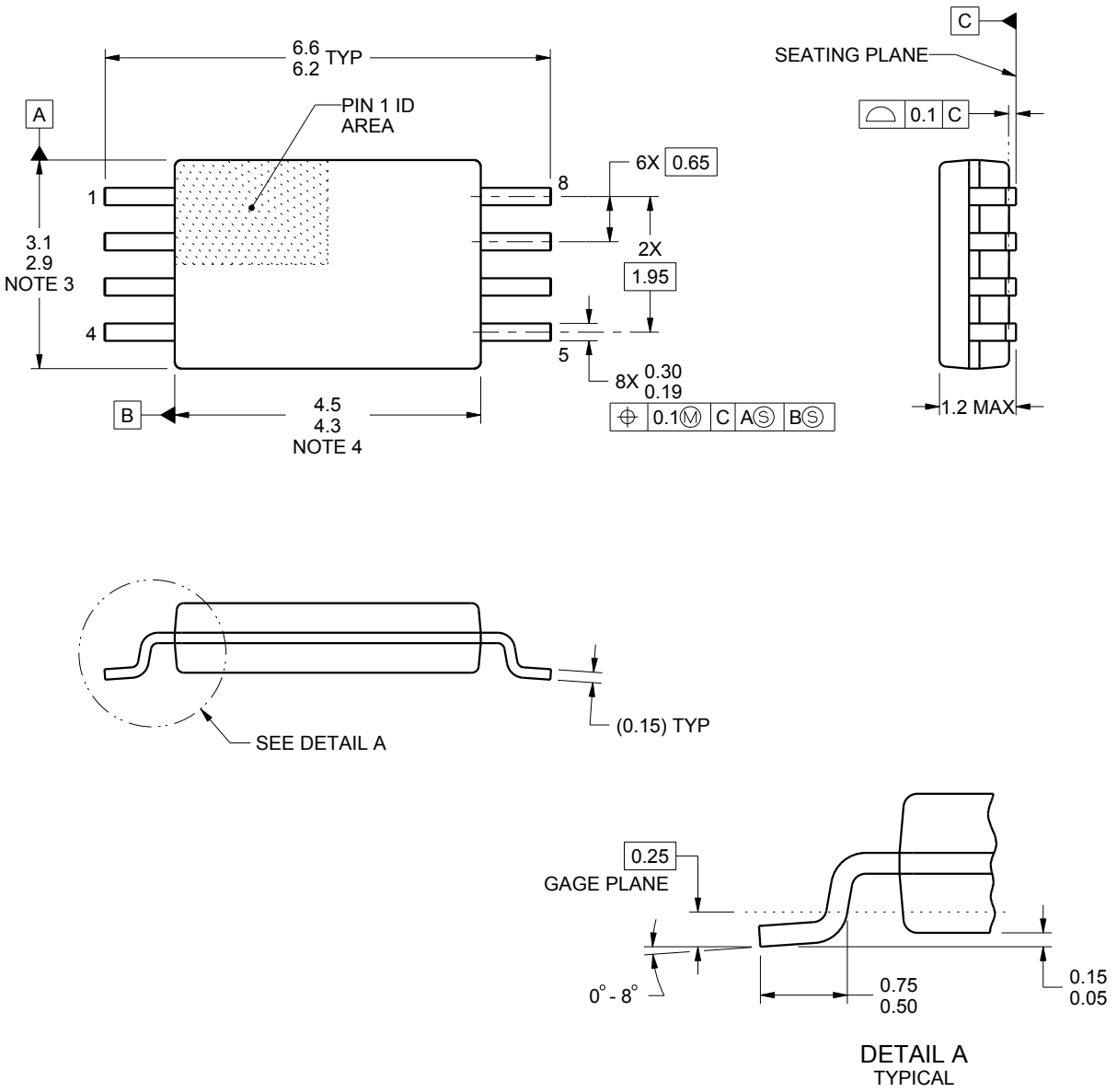
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

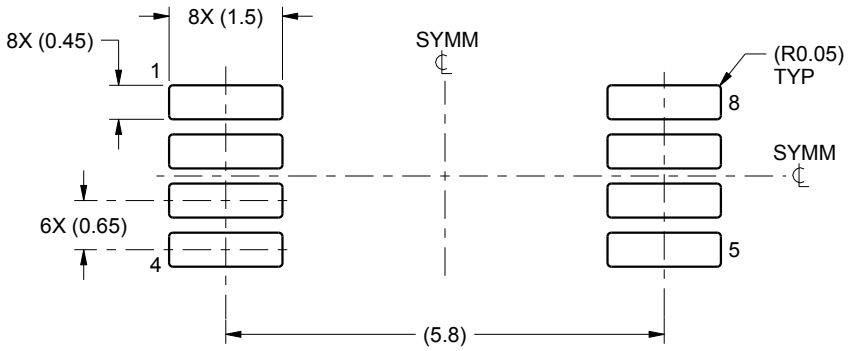
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

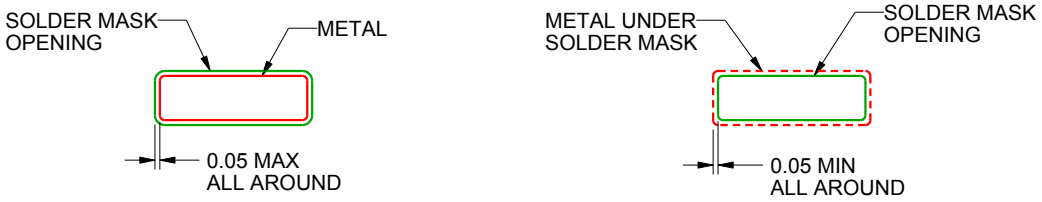


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

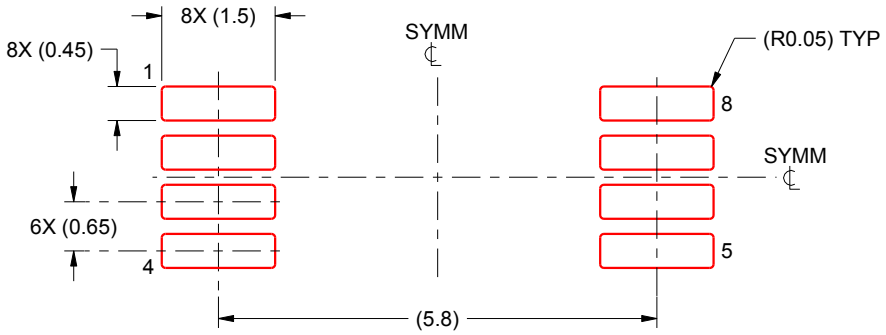


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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