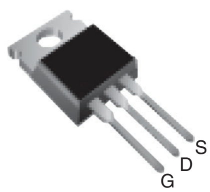
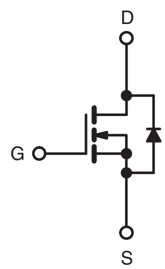
Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	50	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.10
Q_g (Max.) (nC)	17	
Q_{gs} (nC)	9.0	
Q_{gd} (nC)	3.0	
Configuration	Single	

TO-220AB





N-Channel MOSFET

FEATURES

- Extremely Low $R_{DS(on)}$
- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- Excellent Temperature Stability
- Parts Per Million Quality
- Compliant to RoHS Directive 2002/95/EC

Pb Available
RoHS*
COMPLIANT

DESCRIPTION

The technology has expanded its product base to serve the low voltage, very low $R_{DS(on)}$ MOSFET transistor requirements. Vishay's highly efficient geometry and unique processing have been combined to create the lowest on resistance per device performance. In addition to this feature all have documented reliability and parts per million quality!

The transistor also offer all of the well established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, high energy pulse circuits, and in systems that are operated from low voltage batteries, such as automotive, portable equipment, etc.

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRFZ20PbF
	SiHFZ20-E3
SnPb	IRFZ20
	SiHFZ20

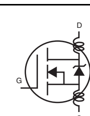
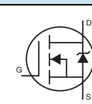
ABSOLUTE MAXIMUM RATINGS					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage[a]			V_{DS}	50	V
Gate-Source Voltage[a]			V_{GS}	± 20	
Continuous Drain Current	V_{GS} at 10 V	T_C = 25 °C	I_D	15	A
		T_C = 100 °C		10	
Pulsed Drain Current[b]			I_{DM}	60	
Single Pulse Avalanche Energy[c]			E_{AS}	5	mJ
Linear Derating Factor (see fig. 16)				0.32	W/°C
Maximum Power Dissipation (see fig. 16)	T_C = 25 °C		P_D	40	W
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300 (0.063" (1.6 mm) from case	

Notes

a. T_J = 25 °C to 150 °C
b. Repeditive rating: Pulse width limited by max. junction temperature. See transient temperature impedance curve (see fig. 11).
c. Starting T_J = 25 °C, L = 0.07 mH, R_g = 25 Ω, I_{AS} = 12 A

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Typical Socket Mount, Junction-to-Ambient	R_{thJA}	-	80	°C/W
Case-to-Sink, Mounting Surface Flat, Smooth, and Greased	R_{thCS}	1.0	-	
Junction-to-Case	R_{thJC}	-	3.12	

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	50	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} > Max. Rating, V_{GS} = 0 V	-	-	250	µA
		V_{DS} = Max. Rating x 0.8, V_{GS} = 0 V, T_C = 125 °C	-	-	1000	
On-State Drain Current	$I_{D(on)}$	V_{GS} = 10 V; V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max.	-	-	15	A
Drain-Source On-State Resistance[b]	$R_{DS(on)}$	V_{GS} = 10 V; I_D = 10 A	-	0.080	0.10	Ω
Forward Transconductance[b]	g_{fs}	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 9.0 A	5.0	6.0	-	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 11	-	560	860	pF
Output Capacitance	C_{oss}		-	250	350	
Reverse Transfer Capacitance	C_{rss}		-	60	100	
Total Gate Charge	Q_g	V_{GS} = 10 V; I_D = 20 A, V_{DS} = 0.8 max. rating, see fig. 18 for test circuit (Gate charge is essentially independent of operating temperature)	-	12	17	nC
Gate-Source Charge	Q_{gs}		-	9.0	-	
Gate-Drain Charge	Q_{gd}		-	3.0	-	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 25 V, I_D = 9.0 A, Z_0 = 50 Ω, see fig. 5[b]	-	15	30	ns
Rise Time	t_r		-	45	90	
Turn-Off Delay Time	$t_{d(off)}$		-	20	40	
Fall Time	t_f		-	15	30	
Internal Drain Inductance	L_D	Modified MOSFET symbol showing the internal device inductances 	-	3.5	-	nH
Internal Source Inductance	L_S		-	4.5	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction rectifier 	-	-	15	A
Pulsed Diode Forward Current[a]	I_{SM}		-	-	60	
Body Diode Voltage[b]	V_{SD}	T_C = 25 °C, I_S = 15 A, V_{GS} = 0 V	-	-	1.5	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 150 °C, I_F = 15 A, dI_F/dt = 100 A/µs	-	100	-	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	0.4	-	µC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes
a. Repeditive rating: Pulse width limited by max. junction temperature. See transient temperature impedance curve (see fig. 5).
b. Pulse test: Pulse width ≤ 300 µs; duty cycle ≤ 2 %.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

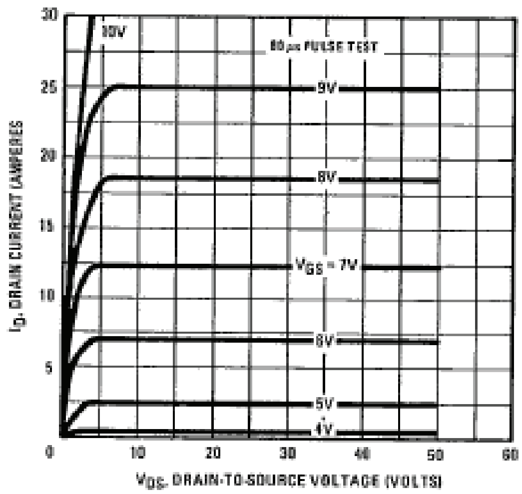


Fig. 1 - Typical Output Characteristics

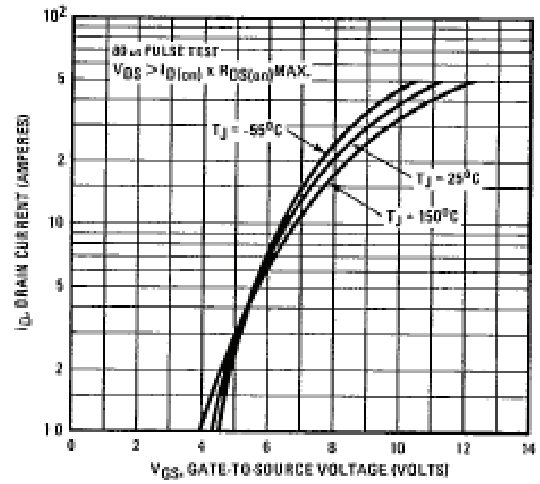


Fig. 3 - Typical Transfer Characteristics

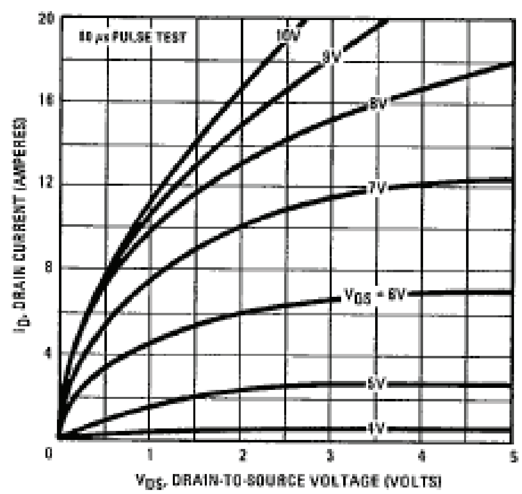


Fig. 2 - Typical Saturation Characteristics

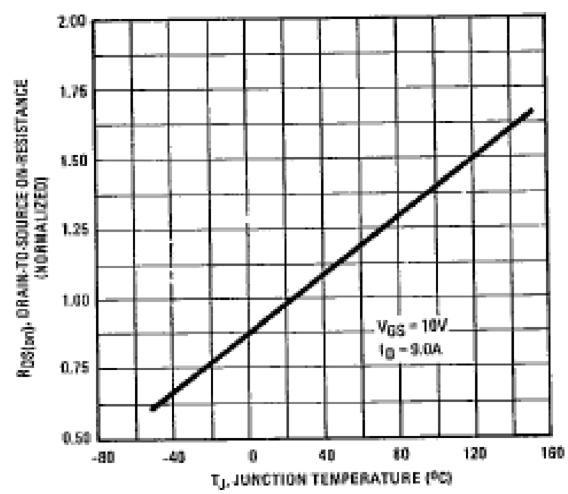


Fig. 4 - Normalized On-Resistance vs. Temperature

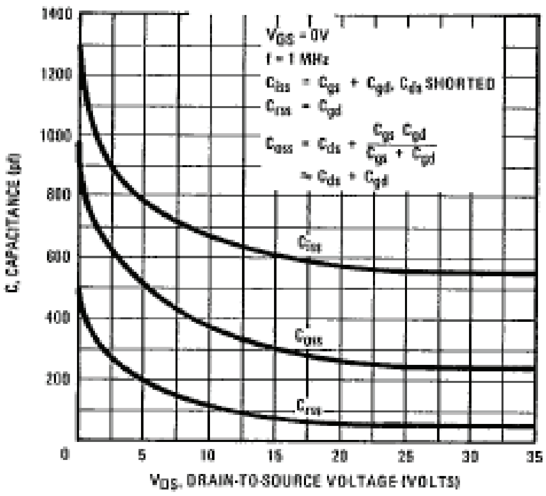


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

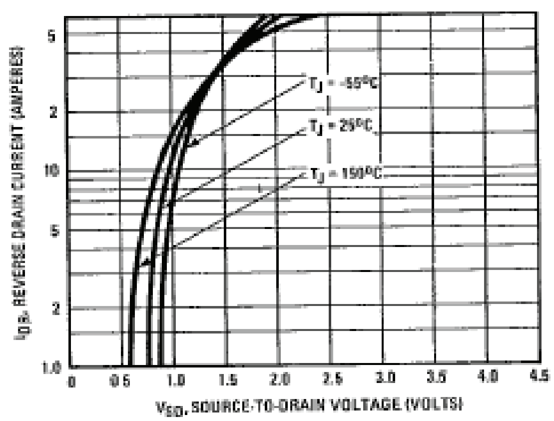


Fig. 7 - Typical Source-Drain Diode Forward Voltage

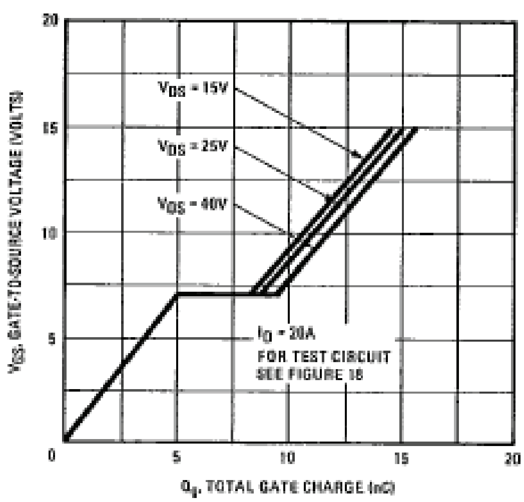


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

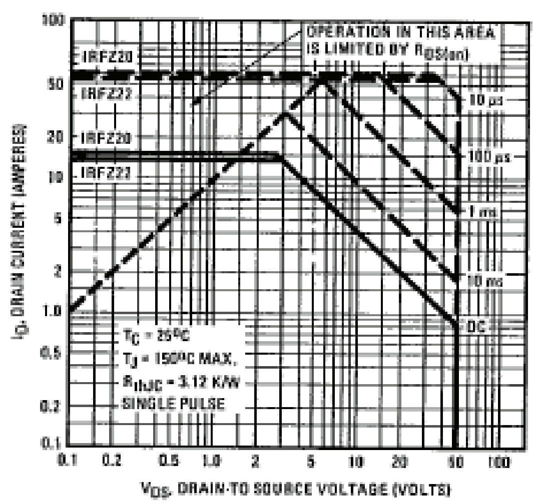


Fig. 8 - Maximum Safe Operating Area

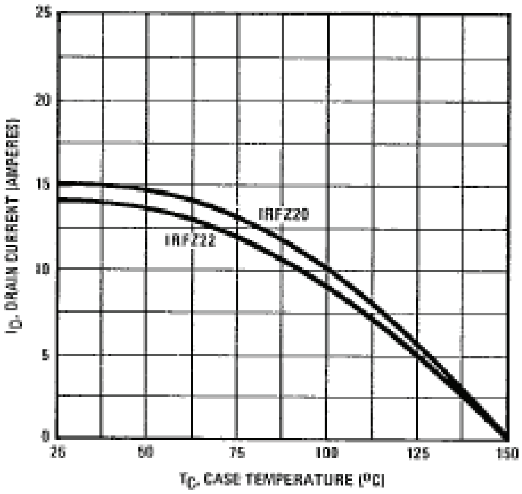


Fig. 9 - Maximum Drain Current vs. Case Temperature

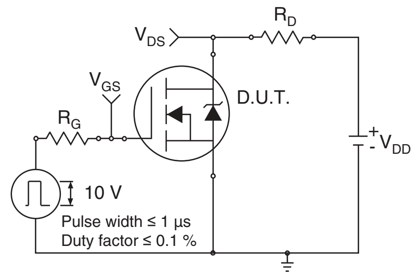


Fig. 10a - Switching Time Test Circuit

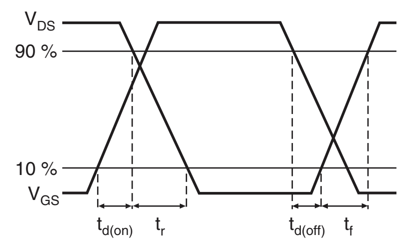


Fig. 10b - Switching Time Waveforms

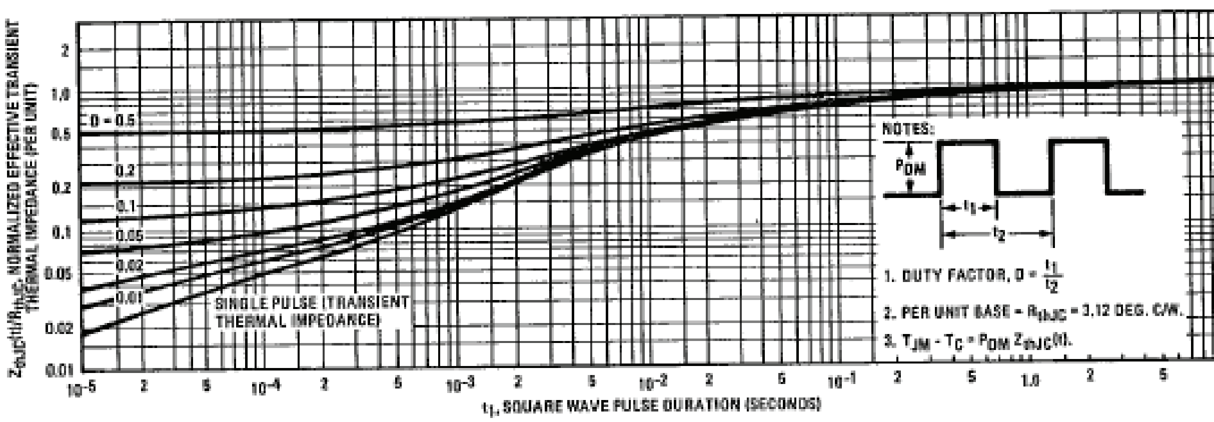


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case vs. Pulse Duration

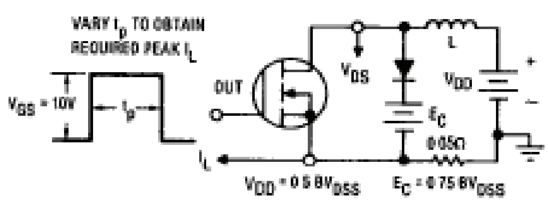


Fig. 12a - Clamped Inductive Test Circuit

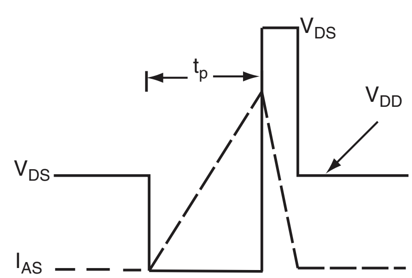


Fig. 12b - Unclamped Inductive Waveforms

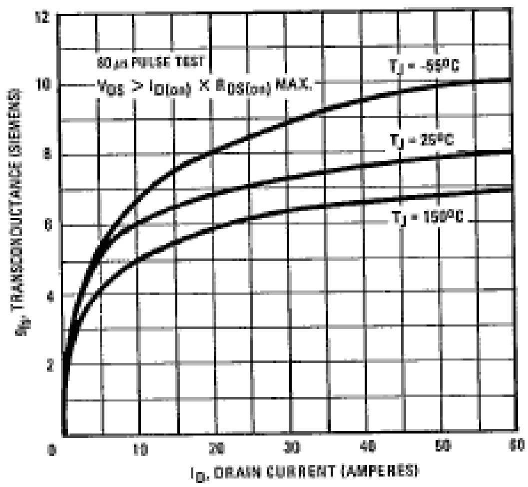


Fig. 13 - Typical Transconductance vs. Drain Current

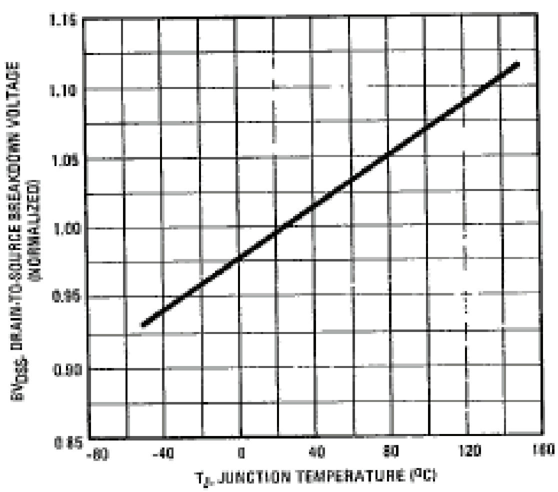


Fig. 14 - Breakdown Voltage vs. Temperature

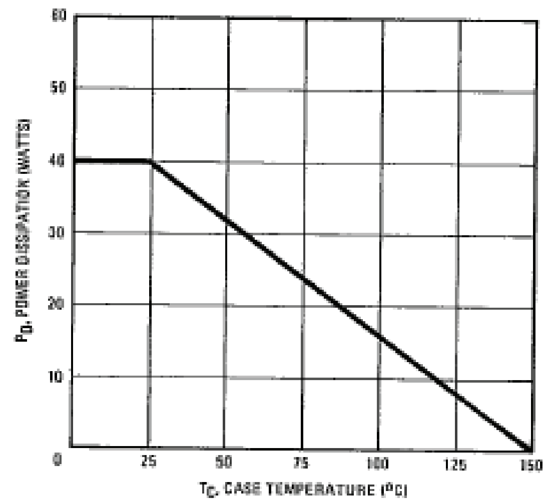


Fig. 16 - Power vs. Temperature Derating Curve

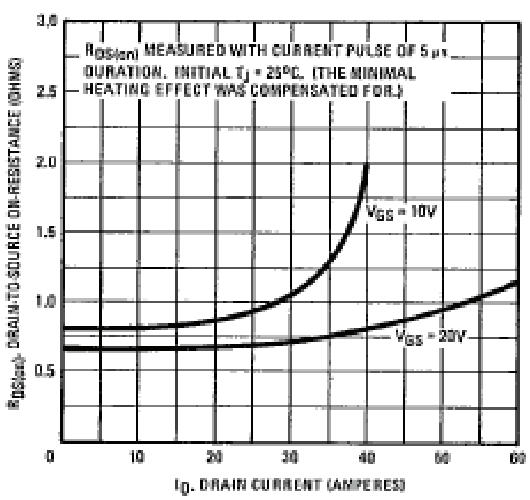


Fig. 15 - Typical On-Resistance vs. Drain Current

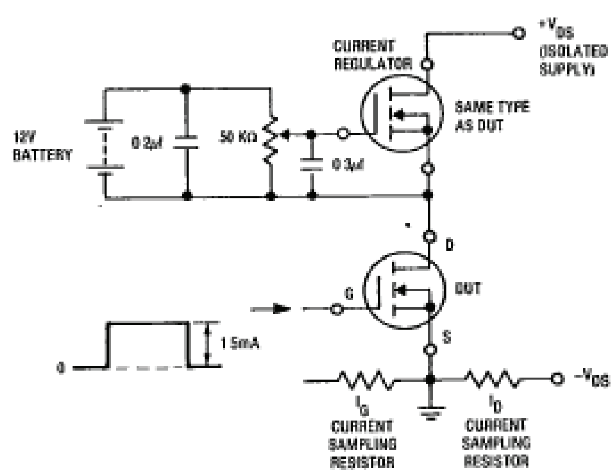
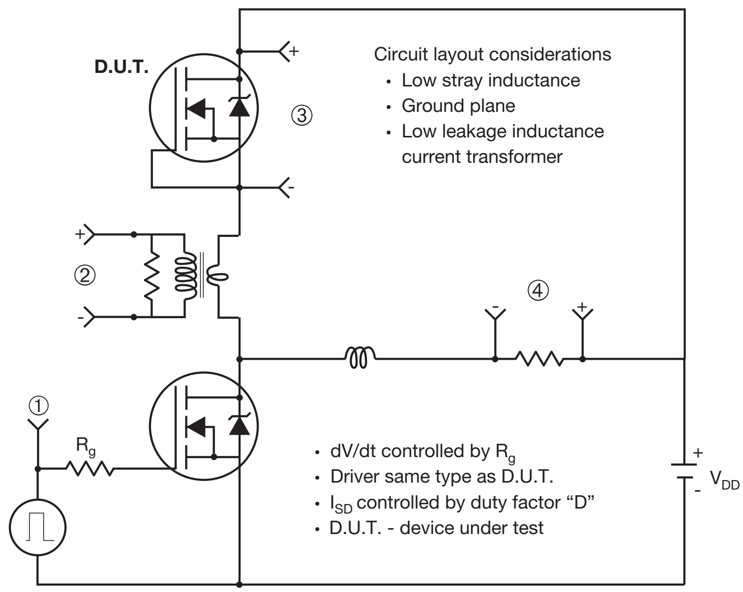
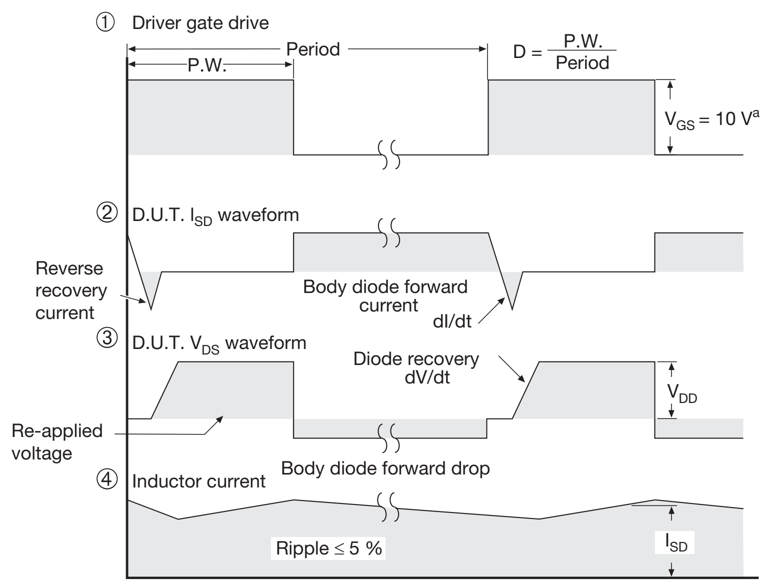


Fig. 17 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit





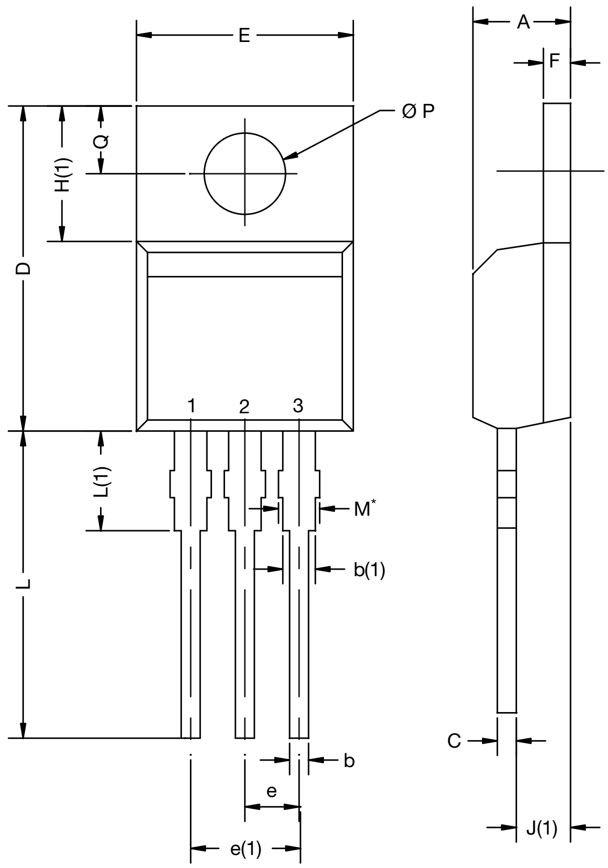
Note

a. V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?91340.

TO-220-1

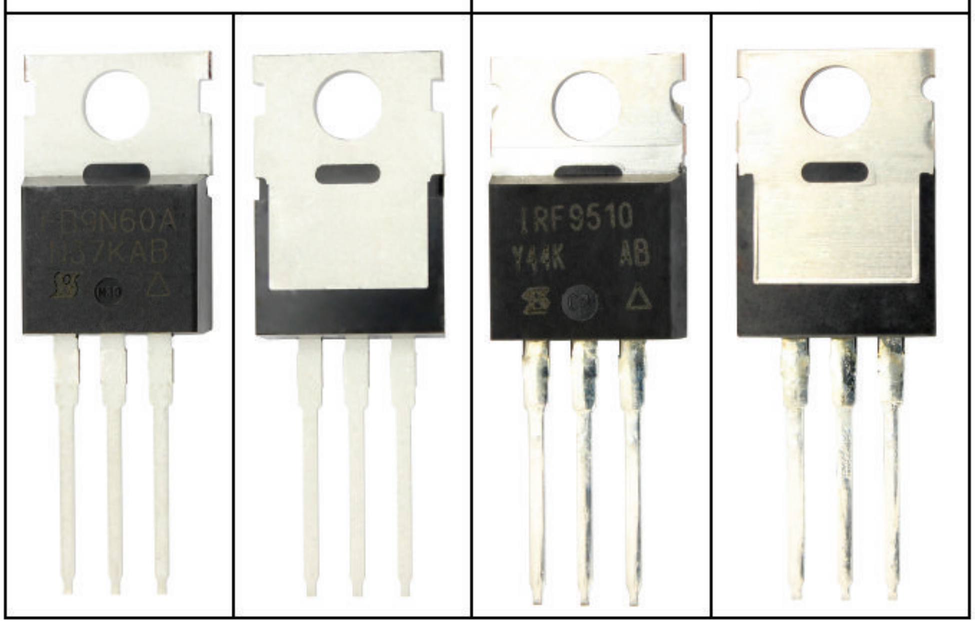


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
c	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
E	9.96	10.52	0.392	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
Ø P	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118
ECN: X15-0364-Rev. C, 14-Dec-15 DWG: 6031				

Note

- M* = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM

Package Picture	
ASE	Xi'an



For technical questions, contact: hvm@vishay.com

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