

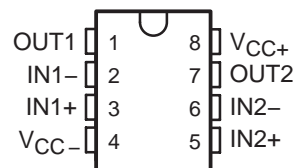
# TL3414A

## DUAL HIGH-OUTPUT-CURRENT OPERATIONAL AMPLIFIER

SLOS453A – DECEMBER 2004 – REVISED JANUARY 2005

- Single/Dual Power-Supply Operation
- High Output Current . . . 70 mA,  $V_{CC+} = 5\text{ V}$
- Wide Operating Voltage . . . 3 V to 15 V (Single Supply)
- Ideal for Headphone Drivers

D (SOIC), P (PDIP), OR PW (TSSOP) PACKAGE  
(TOP VIEW)



### description/ordering information

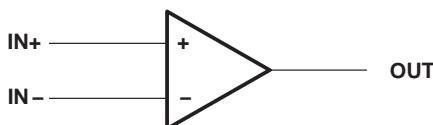
The TL3414A device is a dual operational amplifier that can be operated with single or dual power supplies. In addition to high gain and high output voltage swing, it is capable of driving a 70-mA load, making it ideally suited for simple, low-cost audio-amplifier applications, such as headphone amplifiers in DVD and CDRW applications.

### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP (P)	Tube of 50	TL3414AIP	TL3414AIP
	SOIC (D)	Tube of 75	TL3414AID	Z3414A
		Reel of 2500	TL3414AIDR	
	TSSOP (PW)	Tube of 150	TL3414AIPW	Z3414A
		Reel of 2000	TL3414AIPWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

### symbol (each amplifier)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

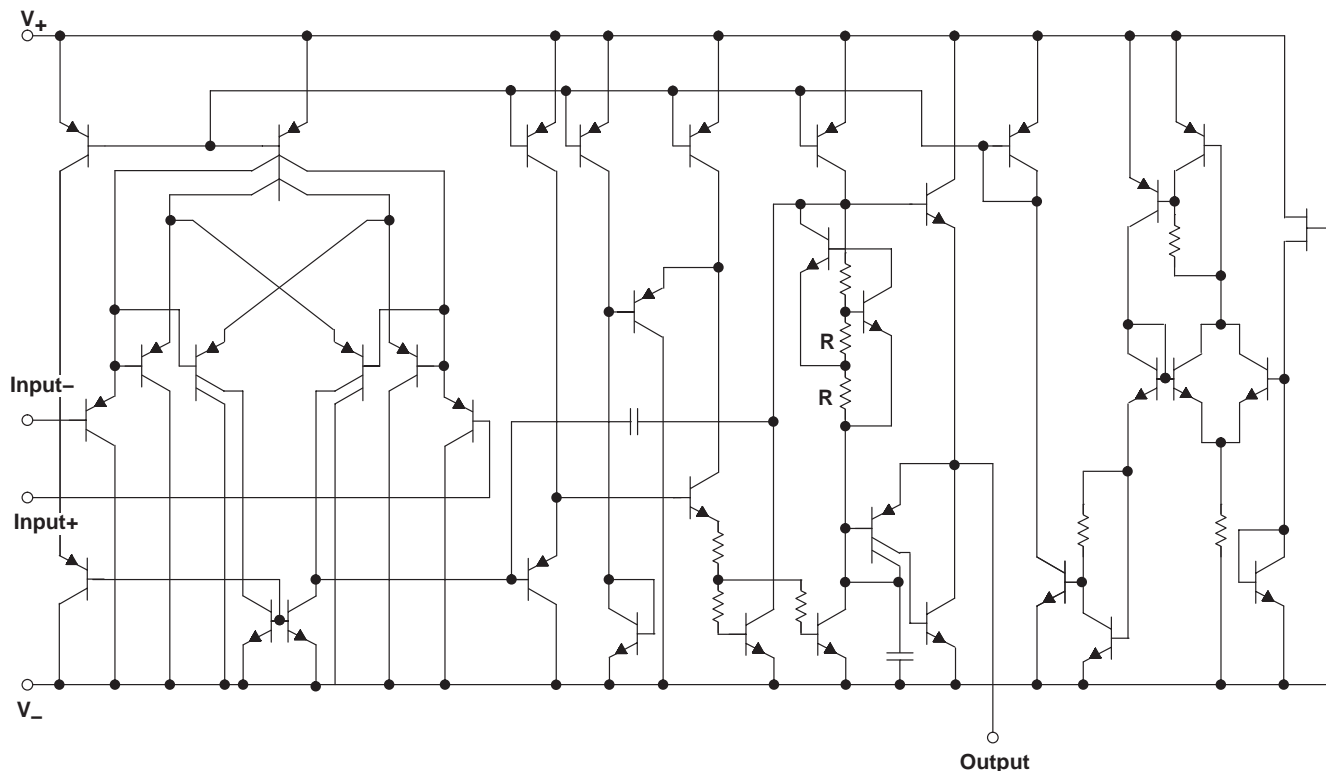
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# TL3414A DUAL HIGH-OUTPUT-CURRENT OPERATIONAL AMPLIFIER

SLOS453A – DECEMBER 2004 – REVISED JANUARY 2005

## simplified schematic



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC+}$ (single supply)	15 V
Supply voltage, $V_{CC-}$ (single supply)	0 V
Supply voltage, $V_{CC+}$ (dual supply)	7.5 V
Supply voltage, $V_{CC-}$ (dual supply)	-7.5 V
Supply voltage, ( $V_{CC-}$ to $V_{CC+}$ )	15 V
Input voltage, either input (see Note 1)	$V_{CC-}$ or $V_{CC+}$
Input current (see Note 2)	$\pm 10$ mA
Duration of output short circuit (see Note 3)	Unlimited
Package thermal impedance, $\theta_{JA}$ (see Notes 4 and 5): D package	97°C/W
P package	85°C/W
PW package	149°C/W
Operating virtual junction temperature, $T_J$	150°C
Storage temperature range, $T_{stg}$	-40°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The magnitude of the input voltage must never exceed the magnitude of the supply voltage.
  2. Excessive input current will flow if a differential input voltage in excess of approximately 0.6 V is applied between the inputs, unless some limiting resistance is used.
  3. The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.
  4. Maximum power dissipation is a function of  $T_J(\max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\max) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can impact reliability.
  5. The package thermal impedance is calculated in accordance with JESD 51-7.



# TL3414A

## DUAL HIGH-OUTPUT-CURRENT OPERATIONAL AMPLIFIER

SLOS453A – DECEMBER 2004 – REVISED JANUARY 2005

### recommended operating conditions

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage (single supply)	3	15	V
$V_{CC+}$	Supply voltage (dual supply)	1.5	7.5	V
$V_{CC-}$	Supply voltage (dual supply)	-1.5	-7.5	V
$V_{ID}$	Differential input voltage		15	V
$V_I$	Input voltage	-0.3	15	V
$T_A$	Operating free-air temperature range	-40	85	°C

### DC electrical characteristics, $V_{CC+} = 5\text{ V}$ , $V_{CC-} = 0\text{ V}$ , $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$V_{IO}$	Input offset voltage $R_S = 0\ \Omega$		2	5	mV	
$I_{IO}$	Input offset current		15	100	nA	
$I_{IB}$	Input bias current		300	600	nA	
$A_{VD}$	Large-signal differential voltage amplification $R_L = 2\text{ k}\Omega$		77	100	dB	
$V_{ICR}$	Common-mode input voltage range		$V_{CC+} - 2\text{ V}$		V	
$V_{OM}$	Output voltage swing $R_L > 2\text{ k}\Omega$ , $V_{CC+} = 5\text{ V}$		3.5		V	
		$I_O = 70\text{ mA}$ , $V_{CC+} = 5\text{ V}$	3.2			
CMRR	Common-mode rejection ratio		70	79	dB	
$k_{SVR}^\dagger$	Supply-voltage rejection ratio		80	90	dB	
$I_{CC}$	Supply current (all amplifiers) $R_L = \text{open circuit (full temperature range)}$		3	4	6	mA

† Measured with  $V_{CC\pm}$  differentially and simultaneously varied from 5 V to 8.6 V

### AC electrical characteristics, $V_{CC+} = 5\text{ V}$ , $V_{CC-} = 0\text{ V}$ , $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP	UNIT
SR	Slew rate at unity gain	0.83	V/ $\mu\text{s}$
GBW	Gain bandwidth product	1.1	MHz
$V_n$	Equivalent input noise voltage $f = 1\text{ kHz}$	18	nV/ $\sqrt{\text{Hz}}$

### DC electrical characteristics, $V_{CC+} = 8.6\text{ V}$ , $V_{CC-} = 0\text{ V}$ , $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$V_{IO}$	Input offset voltage $R_S = 0\ \Omega$		2	5	mV	
$I_{IO}$	Input offset current		15	100	nA	
$I_{IB}$	Input bias current		300	600	nA	
$A_{VD}$	Large-signal differential voltage amplification $R_L = 2\text{ k}\Omega$		88	105	dB	
$V_{ICR}$	Common-mode input voltage range		$V_{CC+} - 2\text{ V}$		V	
$V_{OM}$	Output voltage swing $R_L > 2\text{ k}\Omega$ , $V_{CC+} = 8.6\text{ V}$		7		V	
		$I_O = 70\text{ mA}$ , $V_{CC+} = 8.6\text{ V}$	6.7			
CMRR	Common-mode rejection ratio		80	90	dB	
$k_{SVR}^\dagger$	Supply-voltage rejection ratio		80	90	dB	
$I_{CC}$	Supply current (all amplifiers) $R_L = \text{open circuit (full temperature range)}$		3	4	6	mA

† Measured with  $V_{CC\pm}$  differentially and simultaneously varied from 5 V to 8.6 V



# TL3414A

## DUAL HIGH-OUTPUT-CURRENT OPERATIONAL AMPLIFIER

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AC electrical characteristics,  $V_{CC+} = 8.6\text{ V}$ ,  $V_{CC-} = 0\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
SR	Slew rate at unity gain		1.3	V/ $\mu\text{s}$
GBW	Gain bandwidth product		2	MHz
$V_n$	Equivalent input noise voltage	$f = 1\text{ kHz}$	18	$\text{nV}/\sqrt{\text{Hz}}$

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL3414AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z3414A	<a href="#">Samples</a>
TL3414AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z3414A	<a href="#">Samples</a>
TL3414AIDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z3414A	<a href="#">Samples</a>
TL3414AIPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z3414A	<a href="#">Samples</a>
TL3414AIPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z3414A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL3414AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL3414AIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL3414AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TL3414AIPWR	TSSOP	PW	8	2000	367.0	367.0	35.0





D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW0008A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

# EXAMPLE BOARD LAYOUT

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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