CY7C026A

16K × 16 Dual-Port Static RAM

Features

- True dual-ported memory cells that allow simultaneous access of the same memory location
- 16K × 16 organization (CY7C026A)
- 0.35 micron CMOS for optimum speed and power
- High speed access: 15, and 20 ns
- Low operating power
- Active: I_{CC} = 180 mA (typical)
- Standby: I_{SB3} = 0.05 mA (typical)
- Fully asynchronous operation
- Automatic power-down
- Expandable data bus to 32 bits or more using Master/Slave chip select when using more than one device
- On-chip arbitration logic
- Semaphores included to permit software handshaking between ports
- $\overline{INT}$ flags for port-to-port communication
- Separate upper-byte and lower-byte control
- Pin select for Master or Slave
- Commercial and Industrial temperature ranges
- Available in 100-pin thin quad plastic flatpack (TQFP)
- Pb-free packages available

Functional Description

The CY7C026A is a low power CMOS 16K × 16 dual-port static RAM. Various arbitration schemes are included on the devices to handle situations when multiple processors access the same piece of data. Two ports are provided, permitting independent, asynchronous access for reads and writes to any location in memory. The device can be utilized as standalone 16-bit dual-port static RAM or multiple devices can be combined to function as a 32-bit or wider master/slave dual-port static RAM. An M/$\overline{S}$ pin is provided for implementing 32-bit or wider memory applications without the need for separate master and slave devices or additional discrete logic. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: Chip Enable ($\overline{CE}$), Read or Write Enable (R/$\overline{W}$), and Output Enable ($\overline{OE}$). Two flags are provided on each port ($\overline{BUSY}$ and $\overline{INT}$). $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. The Interrupt flag ($\overline{INT}$) permits communication between ports or systems by means of a mail box. The semaphores are used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power down feature is controlled independently on each port by the chip enable pin.

The CY7C026A is available in 100-pin thin quad plastic flatpack (TQFP) packages.

For a complete list of related documentation, click here.

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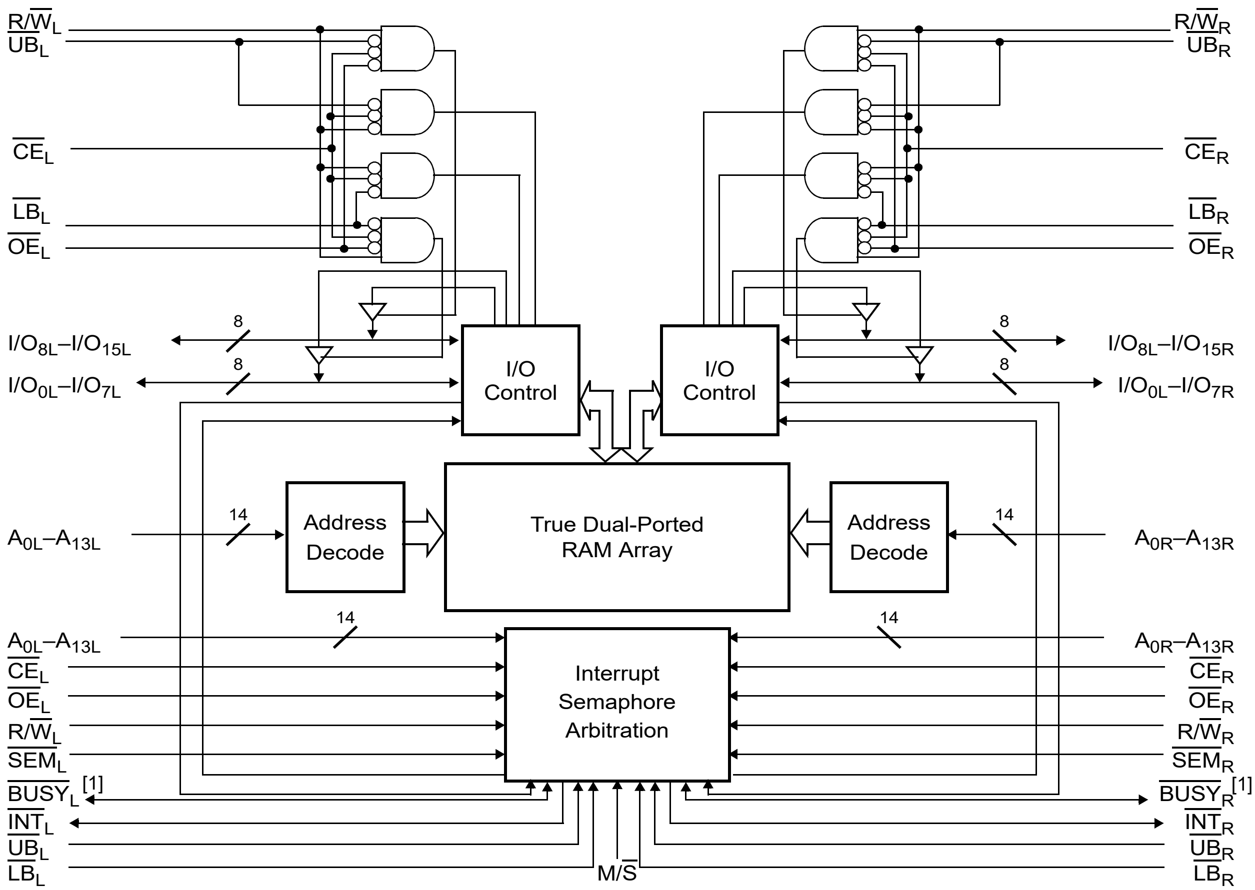
Logic Block Diagram

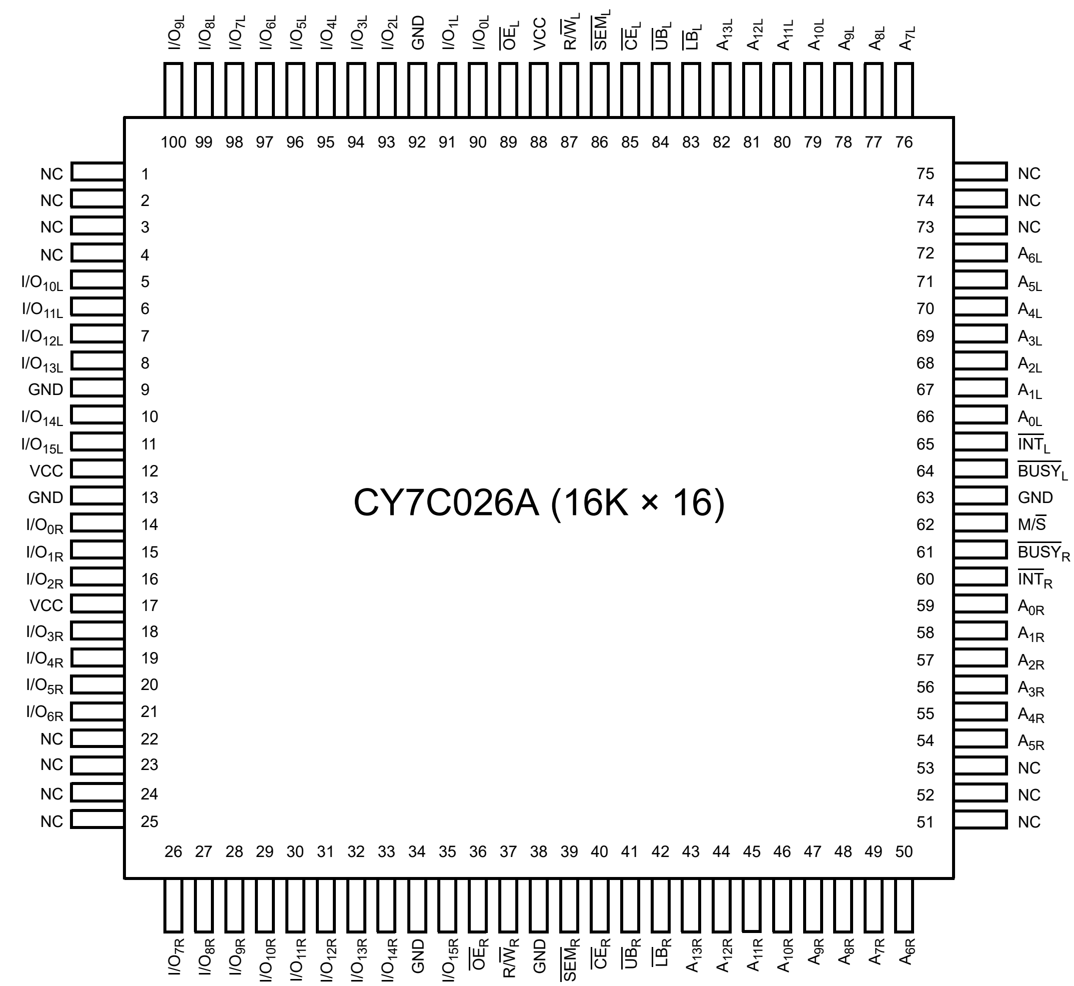


Note
1. BUSY is an output in master mode and an input in slave mode.

Contents

Pin Configurations

Figure 1. 100-pin TQFP pinout (Top View)



Pin Definitions

Left Port	Right Port	Description
$\overline{CE}_L$	$\overline{CE}_R$	Chip enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write enable
$\overline{OE}_L$	$\overline{OE}_R$	Output enable
A_{0L}–A_{13L}	A_{0R}–A_{13R}	Address
I/O_{0L}–I/O_{15L}	I/O_{0R}–I/O_{15R}	Data bus input/output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore enable
$\overline{UB}_L$	$\overline{UB}_R$	Upper byte select (I/O_8–I/O_{15} for × 16 devices)
$\overline{LB}_L$	$\overline{LB}_R$	Lower byte select (I/O_0–I/O_7 for × 16 devices)
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy flag
$M/\overline{S}$		Master or slave select
V_{CC}		Power
GND		Ground
NC		No connect

Selection Guide

Parameter	CY7C026A -15	CY7C026A -20	Unit
Maximum access time	15	20	ns
Typical operating current	190	180	mA
Typical standby current for I_{SB1} (Both ports TTL level)	50	45	mA
Typical standby current for I_{SB3} (Both ports CMOS level)	0.05	0.05	mA

Architecture

The CY7C026A consists of an array of 16K words of 16 bits each of dual-port RAM cells, I/O and address lines, and control signals (CE, OE, R/W). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a BUSY pin is provided on each port. Two Interrupt (INT) pins can be utilized for port-to-port communication. Two Semaphore (SEM) control pins are used for allocating shared resources. With the M/S pin, the devices can function as a master (BUSY pins are outputs) or as a slave (BUSY pins are inputs). The devices also have an automatic power down feature controlled by CE. Each port is provided with its own Output Enable control (OE), which allows data to be read from the device.

Functional Overview

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/W to either the R/W pin (see Figure 6 on page 15) or the CE pin (see Figure 7 on page 15). Required inputs for non-contention operations are summarized in Table 1.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must occur before the data is read on the output; otherwise the data read is not deterministic. Data is valid on the port t_{DDD} after the data is presented on the other port.

Table 1. Non-Contending Read/Write

Inputs						Outputs		Operation
CE	R/W	OE	UB	LB	SEM	$I/O_8–I/O_{15}$	$I/O_0–I/O_7$	
H	X	X	X	X	H	High Z	High Z	Deselected: Power-down
X	X	X	H	H	H	High Z	High Z	Deselected: Power-down
L	L	X	L	H	H	Data in	High Z	Write to upper byte only
L	L	X	H	L	H	High Z	Data in	Write to lower byte only
L	L	X	L	L	H	Data in	Data in	Write to both bytes
L	H	L	L	H	H	Data out	High Z	Read upper byte only
L	H	L	H	L	H	High Z	Data out	Read lower byte only
L	H	L	L	L	H	Data out	Data out	Read both bytes
X	X	H	X	X	X	High Z	High Z	Outputs disabled
H	H	L	X	X	L	Data out	Data out	Read data in semaphore flag
H	H	L	H	H	L	Data out	Data out	Read data in semaphore flag
H	_/¯	X	X	X	L	Data in	Data in	Write D_{IN0} into semaphore flag
H	_/¯	X	H	H	L	Data in	Data in	Write D_{IN0} into semaphore flag
L	X	X	L	X	L			Not allowed
L	X	X	X	L	L			Not allowed

Read Operation

When reading the device, the user must assert both the OE and CE pins. Data is available t_{ACE} after CE or t_{DOE} after OE is asserted. If the user wishes to access a semaphore flag, then the SEM pin must be asserted instead of the CE pin, and OE must also be asserted.

Interrupts

The upper two memory locations may be used for message passing. The highest memory location (3FFF) is the mailbox for the right port and the second highest memory location (3FFE) is the mailbox for the left port. When one port writes to the other port's mailbox, an interrupt is generated to the owner. The interrupt is reset when the owner reads the contents of the mailbox. The message is user defined.

Each port can read the other port's mailbox without resetting the interrupt. The active state of the busy signal (to a port) prevents the port from setting the interrupt to the winning port. Also, an active busy to a port prevents that port from reading its own mailbox and, thus, resetting the interrupt to it.

If an application does not require message passing, do not connect the interrupt pin to the processor's interrupt request input pin.

The operation of the interrupts and their interaction with Busy are summarized in Table 2.

Table 2. Interrupt Operation Example (Assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = HIGH)

Function	Left Port					Right Port				
	$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A_{0L–13L}$	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A_{0R–13R}$	$\overline{INT}_R$
Set right $\overline{INT}_R$ flag	L	L	X	3FFF	X	X	X	X	X	L[2]
Reset right $\overline{INT}_R$ flag	X	X	X	X	X	X	L	L	3FFF	H[3]
Set left $\overline{INT}_L$ flag	X	X	X	X	L[3]	L	L	X	3FFE	X
Reset left $\overline{INT}_L$ flag	X	L	L	3FFE	H[2]	X	X	X	X	X

Busy

The CY7C026A provides on-chip arbitration to resolve simultaneous memory location access (contention). If both ports' $\overline{CE}$s are asserted and an address match occurs within t_{PS} of each other, the busy logic determines which port has access. If t_{PS} is violated, one port definitely gains permission to the location, but it is not predictable which port gets that permission. $\overline{BUSY}$ is asserted t_{BLA} after an address match or t_{BLC} after $\overline{CE}$ is taken LOW.

Master/Slave

A M/$\overline{S}$ pin is provided to expand the word width by configuring the device as either a master or a slave. The $\overline{BUSY}$ output of the master is connected to the $\overline{BUSY}$ input of the slave. This allows the device to interface to a master device with no external components. Writing to slave devices must be delayed until after the $\overline{BUSY}$ input has settled (t_{BLC} or t_{BLA}), otherwise, the slave chip may begin a write cycle during a contention situation. When tied HIGH, the M/$\overline{S}$ pin allows the device to be used as a master and, therefore, the $\overline{BUSY}$ line is an output. $\overline{BUSY}$ can then be used to send the arbitration outcome to a slave.

Notes
2. If $\overline{BUSY}_R$ = L, then no change.
3. If $\overline{BUSY}_L$ = L, then no change.

Semaphore Operation

The CY7C026A provides eight semaphore latches, which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a zero to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, $\overline{SEM}$ or $\overline{OE}$ must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value is available t_{SWRD} + t_{DOE} after the rising edge of the semaphore write. If the left port was successful (reads a zero), it assumes control of the shared resource, otherwise (reads a one) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a one), the left side succeeds in gaining control of the semaphore. If the left side no longer requires the semaphore, a one is written to cancel its request.

Semaphores are accessed by asserting $\overline{SEM}$ LOW. The $\overline{SEM}$ pin functions as a chip select for the semaphore latches ($\overline{CE}$ must remain HIGH during $\overline{SEM}$ LOW). $A_{0–2}$ represents the semaphore address. $\overline{OE}$ and R/$\overline{W}$ are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O_0 is used. If a zero is written to the left port of an available semaphore, a one appears at the same semaphore address on the right port. That semaphore can now only be modified by the side showing zero (the left port in this case). If the left port now relinquishes control by writing a one to the semaphore, the semaphore is set to one for both sides. However, if the right port had requested the semaphore (written a zero) while the left port had control, the right port would immediately own the semaphore as soon as the left port released it. Table 3 shows sample semaphore operations.

When reading a semaphore, all sixteen/eighteen data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t_{SPS} of each other, the semaphore is definitely obtained by one side or the other, but there is no guarantee which side controls the semaphore.

Table 3. Semaphore Operation Example

Function	I/O_0–I/O_{15} Left	I/O_0–I/O_{15} Right	Status
No action	1	1	Semaphore free
Left port writes 0 to semaphore	0	1	Left port has semaphore token
Right port writes 0 to semaphore	0	1	No change. Right side has no write access to semaphore
Left port writes 1 to semaphore	1	0	Right port obtains semaphore token
Left port writes 0 to semaphore	1	0	No change. Left port has no write access to semaphore
Right port writes 1 to semaphore	0	1	Left port obtains semaphore token
Left port writes 1 to semaphore	1	1	Semaphore free
Right port writes 0 to semaphore	1	0	Right port has semaphore token
Right port writes 1 to semaphore	1	1	Semaphore free
Left port writes 0 to semaphore	0	1	Left port has semaphore token
Left port writes 1 to semaphore	1	1	Semaphore free

Maximum Ratings

Exceeding maximum ratings [4] may shorten the useful life of the device. User guidelines are not tested.

Storage temperature .... –65 °C to +150 °C

Ambient temperature
with power applied .... –55 °C to +125 °C

Supply voltage to ground potential ....–0.3 V to +7.0 V

DC voltage applied to outputs
in High Z state ....–0.5 V to +7.0 V

DC input voltage [5] ....–0.5 V to + 7.0 V

Output current into outputs (LOW) .... 20 mA

Static discharge voltage .... >2001 V

Latch-up current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to +70 °C	5 V ± 10%
Industrial	–40 °C to +85 °C	5 V ± 10%

Electrical Characteristics

Over the Operating Range

Parameter	Description		CY7C026A						Unit
			-15			-20			
			Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH voltage (V_{CC} = Min., I_{OH} = –4.0 mA)		2.4	–	–	2.4	–	–	V
V_{OL}	Output LOW voltage (V_{CC} = Min., I_{OH} = +4.0 mA)		–		0.4	–		0.4	V
V_{IH}	Input HIGH voltage		2.2		–	2.2		–	V
V_{IL}	Input LOW voltage		–		0.8	–		0.8	V
I_{OZ}	Output leakage current		–10		10	–10		10	µA
I_{CC}	Operating current (V_{CC} = Max, I_{OUT} = 0 mA) outputs disabled	Commercial	–	190	285	–	180	275	mA
		Industrial		215	305		–		mA
I_{SB1}	Standby current (Both ports TTL level) $\overline{CE}_L$ & $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}	Commercial		50	70		45	65	mA
		Industrial		65	95		–		mA
I_{SB2}	Standby current (One port TTL level) $\overline{CE}_L$ | $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}	Commercial		120	180		110	160	mA
		Industrial		135	205		–		mA
I_{SB3}	Standby current (Both port CMOS level) $\overline{CE}_L$ & $\overline{CE}_R \geq V_{CC}$–0.2 V, f = 0	Commercial		0.05	0.5		0.05	0.5	mA
		Industrial		0.05	0.5		–		mA
I_{SB4}	Standby current (One port CMOS level) $\overline{CE}_L$ | $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}[6]	Commercial		110	160		100	140	mA
		Industrial		125	175		–		mA

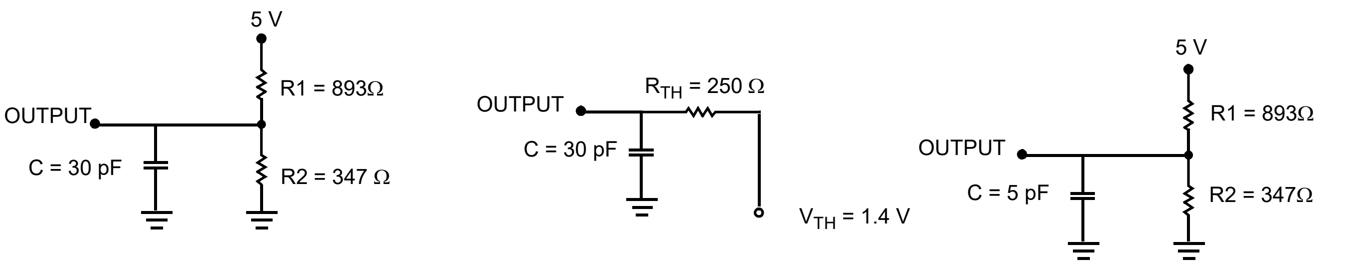
Notes
4. The voltage on any input or I/O pin cannot exceed the power pin during power up.
5. Pulse width < 20 ns.
6. $f_{MAX} = 1/t_{RC}$ = All inputs cycling at f = $1/t_{RC}$ (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.

Capacitance

Parameter [7]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 5.0 V	10	pF
C_{OUT}	Output capacitance		10	pF

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms

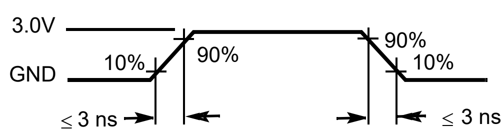


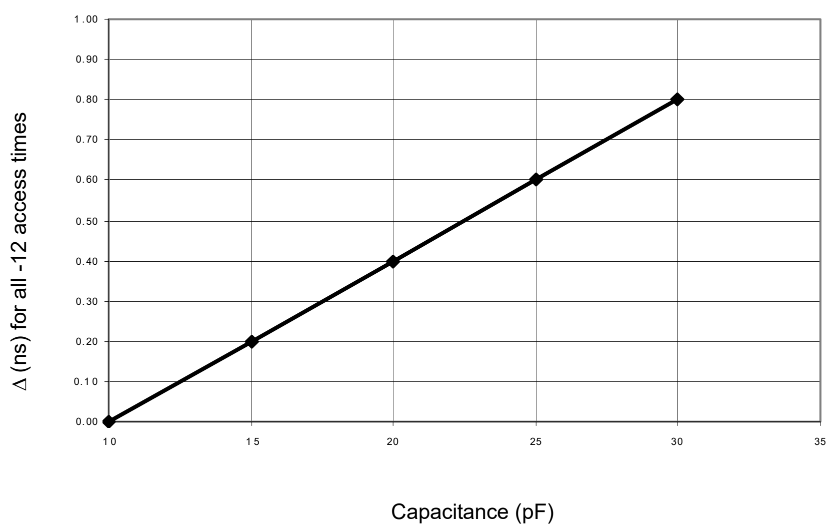
(a) Normal Load (Load 1)

(b) Thévenin Equivalent (Load 1)

(c) Three-State Delay (Load 2)
(Used for t_{LZ}, t_{HZ}, t_{HZWE}, & t_{LZWE} including scope and jig)

ALL INPUT PULSES





Load Derating Curve

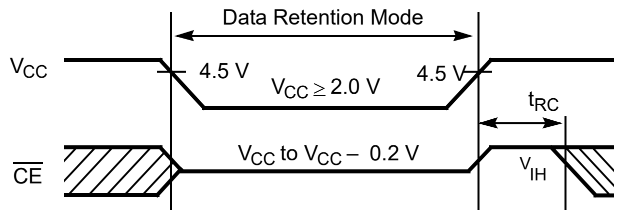
Note
7. Tested initially and after any design or process changes that may affect these parameters.

Data Retention Mode

The CY7C026A is designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules ensure data retention:

1. Chip Enable ($\overline{CE}$) must be held HIGH during data retention, within V_{CC} to V_{CC} – 0.2 V.
2. $\overline{CE}$ must be kept between V_{CC} – 0.2 V and 70% of V_{CC} during the power up and power down transitions.
3. The RAM can begin operation > t_{RC} after V_{CC} reaches the minimum operating voltage (4.5 V).

Timing



Parameter	Test Conditions [8]	Max	Unit
ICC_{DR1}	At VCC_{DR} = 2 V	1.5	mA

Note
8. $\overline{CE}$ = V_{CC}, V_{in} = GND to V_{CC}, T_A = 25 °C. This parameter is guaranteed but not tested.

Switching Characteristics

Over the Operating Range

Parameter [9]	Description	CY7C026A				Unit
		-15		-20		
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	15	–	20	–	ns
t_{AA}	Address to data valid	–	15	–	20	ns
t_{OHA}	Output hold from address change	3	–	3	–	ns
t_{ACE}[10]	$\overline{CE}$ LOW to data valid	–	15	–	20	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	10	–	12	ns
t_{LZOE}[11, 12, 13]	$\overline{OE}$ LOW to Low Z	3	–	3	–	ns
t_{HZOE}[11, 12, 13]	$\overline{OE}$ HIGH to High Z	–	10	–	12	ns
t_{LZCE}[11, 12, 13]	$\overline{CE}$ LOW to Low Z	3	–	3	–	ns
t_{HZCE}[11, 12, 13]	$\overline{CE}$ HIGH to High Z	–	10	–	12	ns
t_{PU}[13]	$\overline{CE}$ LOW to Power-up	0	–	0	–	ns
t_{PD}[13]	$\overline{CE}$ HIGH to Power-down	–	15	–	20	ns
t_{ABE}[10]	Byte enable access time	–	15	–	20	ns
Write Cycle						
t_{WC}	Write cycle time	15	–	20	–	ns
t_{SCE}[10]	$\overline{CE}$ LOW to write end	12	–	15	–	ns
t_{AW}	Address valid to write end	12	–	15	–	ns
t_{HA}	Address hold From write end	0	–	0	–	ns
t_{SA}[10]	Address setup to write start	0	–	0	–	ns
t_{PWE}	Write pulse width	12	–	15	–	ns
t_{SD}	Data setup to write end	10	–	15	–	ns
t_{HD}[14]	Data hold from write end	0	–	0	–	ns
t_{HZWE}[12, 13]	R/$\overline{W}$ LOW to High Z	–	10	–	12	ns
t_{LZWE}[12, 13]	R/$\overline{W}$ HIGH to Low Z	3	–	3	–	ns
t_{WDD}[15]	Write pulse to data delay	–	30	–	45	ns
t_{DDD}[15]	Write data valid to read data valid	–	25	–	30	ns

Notes

9. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OI}/I_{OH} and 30 pF load capacitance.
10. To access RAM, $\overline{CE}$ = L, $\overline{SEM}$ = H. To access semaphore, $\overline{CE}$ = H and $\overline{SEM}$ = L. Either condition must be valid for the entire t_{SCE} time.
11. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
12. Test conditions used are Load 2.
13. This parameter is guaranteed but not tested.
14. For 15 ns industrial parts t_{HD} minimum is 0.5 ns.
15. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Figure 10 on page 17.

Switching Characteristics (continued)

Over the Operating Range

Parameter [9]	Description	CY7C026A				Unit
		-15		-20		
		Min	Max	Min	Max	
Busy Timing[16]						
t_{BLA}	$\overline{BUSY}$ LOW from address match	–	15	–	20	ns
t_{BHA}	$\overline{BUSY}$ HIGH from address mismatch	–	15	–	20	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW	–	15		20	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH	–	15	–	17	ns
t_{PS}	Port setup for priority	5	–	5	–	ns
t_{WB}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ (Slave)	0	–	0	–	ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH (Slave)	13	–	15	–	ns
t_{BDD}[17]	$\overline{BUSY}$ HIGH to data valid	–	15	–	20	ns
Interrupt Timing[16]						
t_{INS}	$\overline{INT}$ set time	–	15	–	20	ns
t_{INR}	$\overline{INT}$ reset time	–	15	–	20	ns
Semaphore Timing						
t_{SOP}	SEM flag update pulse ($\overline{OE}$ or $\overline{SEM}$)	10	–	10	–	ns
t_{SWRD}	SEM flag write to read time	5	–	5	–	ns
t_{SPS}	SEM flag contention window	5	–	5	–	ns
t_{SAA}	SEM address access time	–	15	–	20	ns

Notes
16. Test conditions used are Load 2.
17. t_{BDD} is a calculated parameter and is the greater of $t_{WDD}–t_{PWE}$ (actual) or $t_{DDD}–t_{SD}$ (actual).

Switching Waveforms

Figure 3. Read Cycle No. 1 (Either Port Address Access) [18, 19, 20]

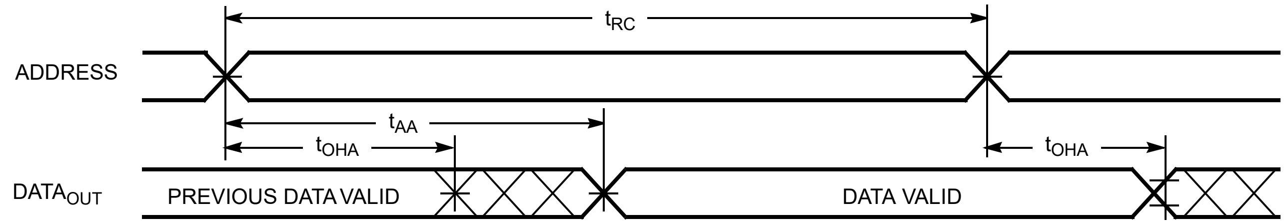


Figure 4. Read Cycle No. 2 (Either Port $\overline{CE}/\overline{OE}$ Access) [18, 21, 22]

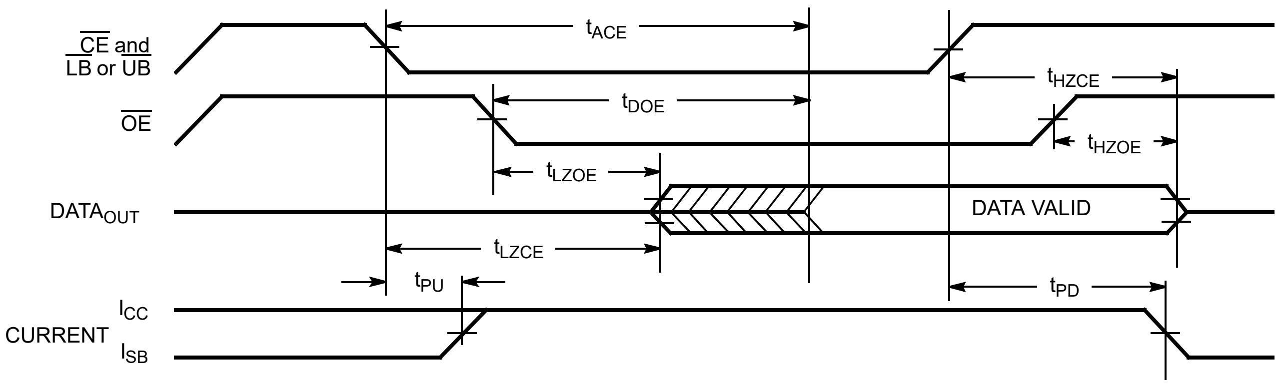
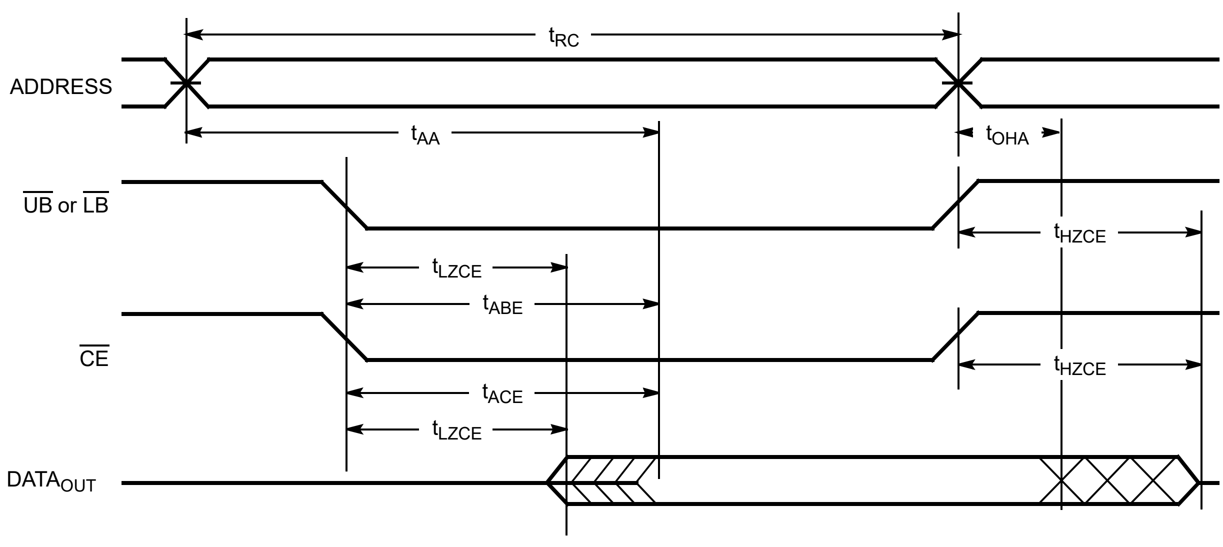


Figure 5. Read Cycle No. 3 (Either Port) [18, 20, 21, 22]



Notes

18. R/$\overline{W}$ is HIGH for read cycles.
19. Device is continuously selected $\overline{CE}$ = V_{IL} and $\overline{UB}$ or $\overline{LB}$ = V_{IL}. This waveform cannot be used for semaphore reads.
20. $\overline{OE}$ = V_{IL}.
21. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
22. To access RAM, $\overline{CE}$ = V_{IL}, $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH}, $\overline{SEM}$ = V_{IL}.

Switching Waveforms (continued)

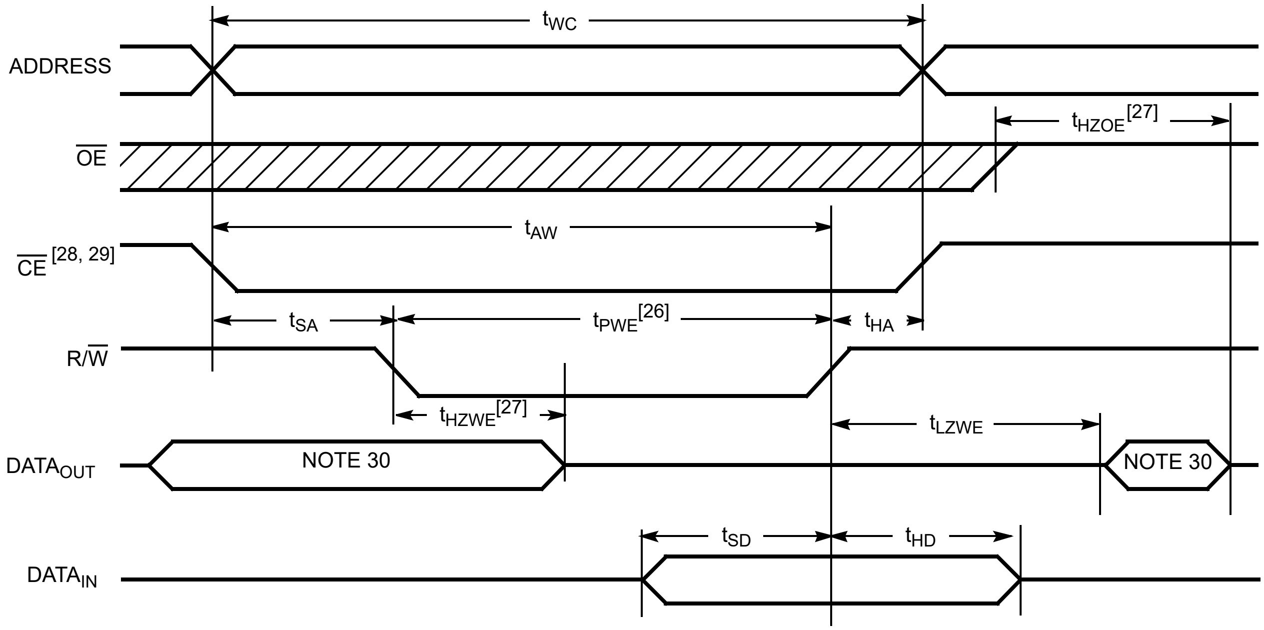


Figure 6. Write Cycle No. 1 (R/$\overline{\text{W}}$ Controlled Timing) [23, 24, 25, 26]

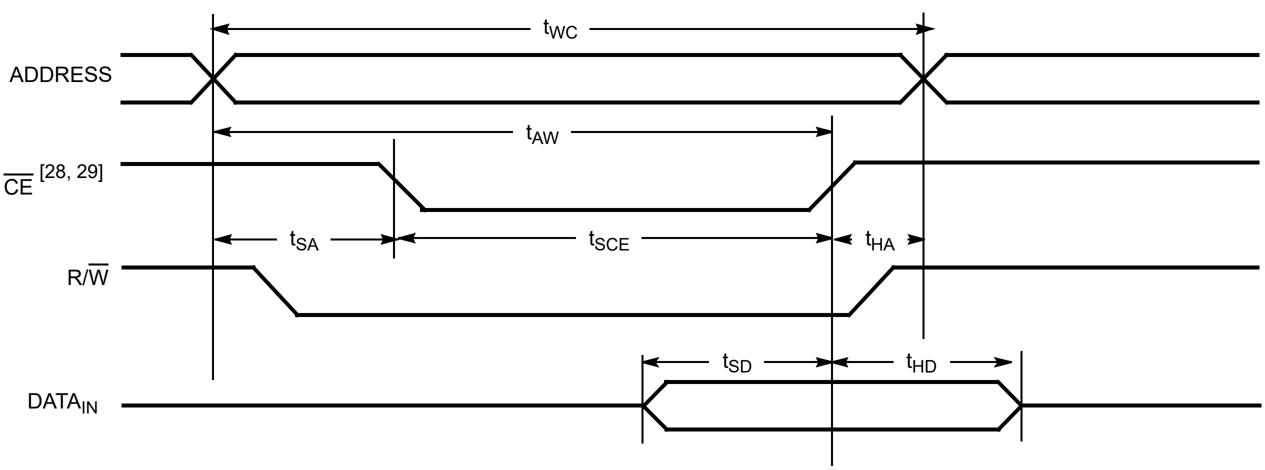


Figure 7. Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled Timing) [23, 24, 25, 31]

Notes

23. R/$\overline{\text{W}}$ must be HIGH during all address transitions.
24. A write occurs during the overlap (t_{SCE} or t_{PWE}) of a LOW $\overline{\text{CE}}$ or $\overline{\text{SEM}}$ and a LOW $\overline{\text{UB}}$ or $\overline{\text{LB}}$.
25. t_{HA} is measured from the earlier of $\overline{\text{CE}}$ or R/$\overline{\text{W}}$ or ($\overline{\text{SEM}}$ or R/$\overline{\text{W}}$) going HIGH at the end of write cycle.
26. If $\overline{\text{OE}}$ is LOW during a R/$\overline{\text{W}}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or (t_{HZWE} + t_{SD}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If $\overline{\text{OE}}$ is HIGH during an R/$\overline{\text{W}}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.
27. Transition is measured ±500 mV from steady state with a 5 pF load (including scope and jig). This parameter is sampled and not 100% tested.
28. To access RAM, $\overline{\text{CE}}$ = V_{IL}, $\overline{\text{SEM}}$ = V_{IH}.
29. To access upper byte, $\overline{\text{CE}}$ = V_{IL}, $\overline{\text{UB}}$ = V_{IL}, $\overline{\text{SEM}}$ = V_{IH}.
    To access lower byte, $\overline{\text{CE}}$ = V_{IL}, $\overline{\text{LB}}$ = V_{IL}, $\overline{\text{SEM}}$ = V_{IH}.
30. During this period, the I/O pins are in the output state, and input signals must not be applied.
31. If the $\overline{\text{CE}}$ or $\overline{\text{SEM}}$ LOW transition occurs simultaneously with or after the R/$\overline{\text{W}}$ LOW transition, the outputs remain in the high impedance state.

Switching Waveforms (continued)

Figure 8. Semaphore Read After Write Timing, Either Side [32]

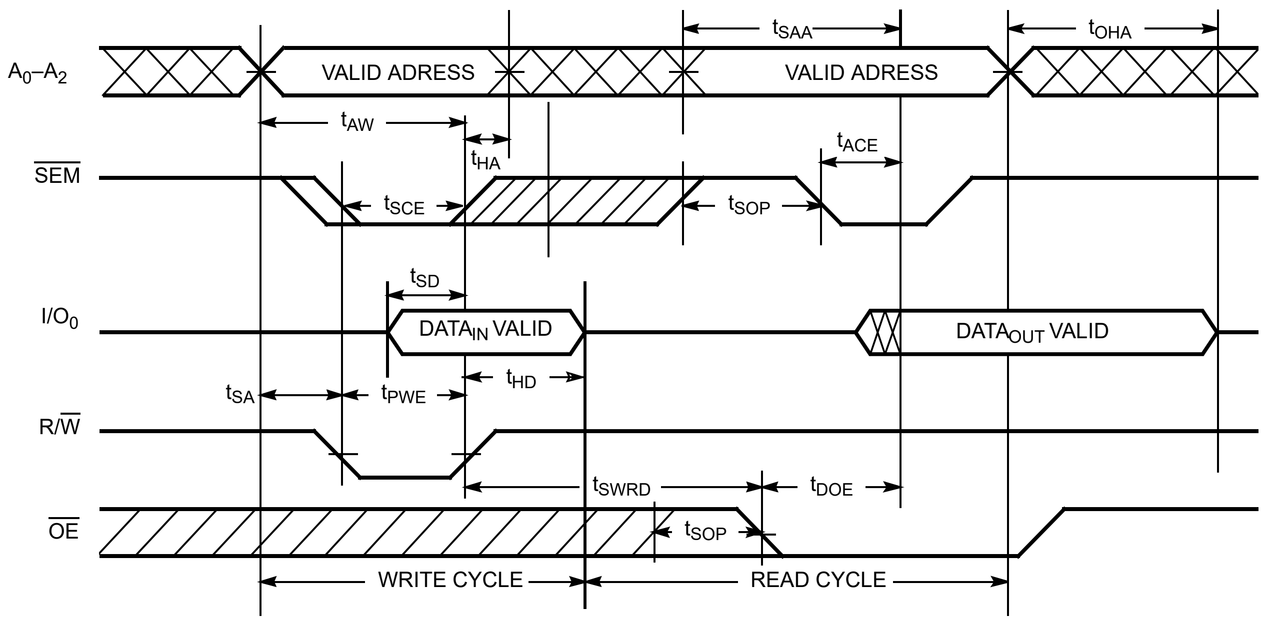
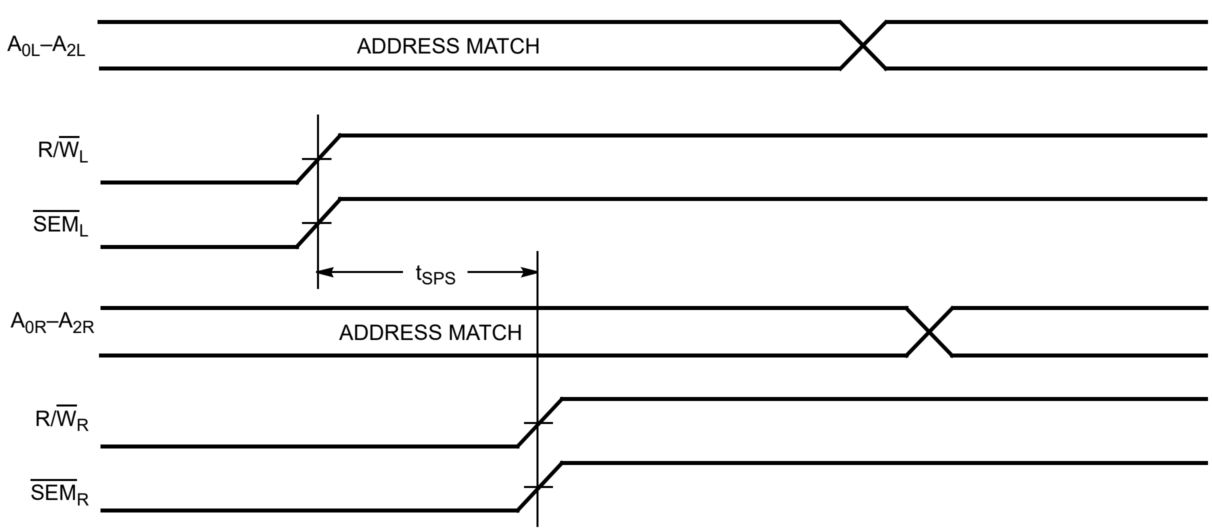


Figure 9. Timing Diagram of Semaphore Contention [33, 34, 35]



Notes

32. $\overline{CE}$ = HIGH for the duration of the above timing (both write and read cycle).
33. $I/O_{0R} = I/O_{0L}$ = LOW (request semaphore); $\overline{CE}_R = \overline{CE}_L$ = HIGH.
34. Semaphores are reset (available to both ports) at cycle start.
35. If t_{SPS} is violated, the semaphore is definitely obtained by one side or the other, but which side gets the semaphore is unpredictable.

Switching Waveforms (continued)

Figure 10. Timing Diagram of Read with $\overline{BUSY}$ (M/$\overline{S}$ = HIGH) [36]

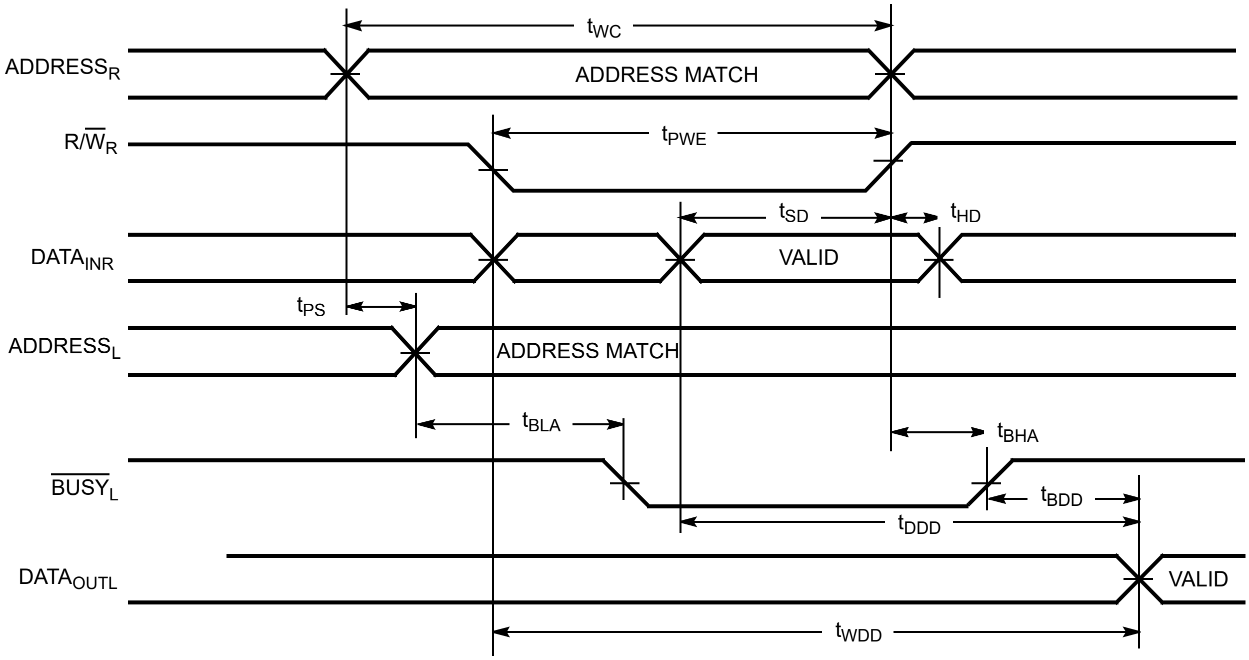
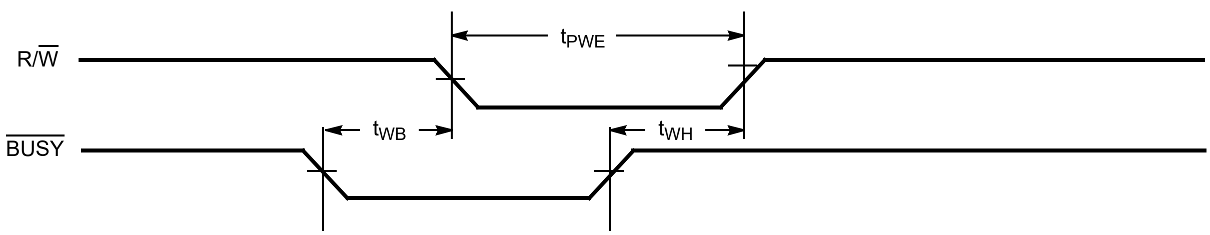


Figure 11. Write Timing with Busy Input (M/$\overline{S}$ = LOW)

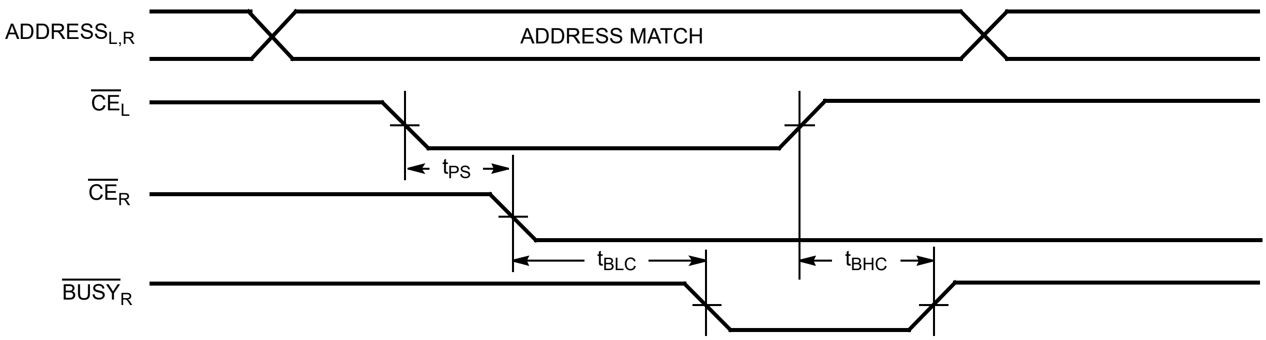


Note
36. $\overline{CE}_L = \overline{CE}_R$ = LOW.

Switching Waveforms (continued)

Figure 12. Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration) [37]

$\overline{CE}_L$ Valid First:



$\overline{CE}_R$ Valid First:

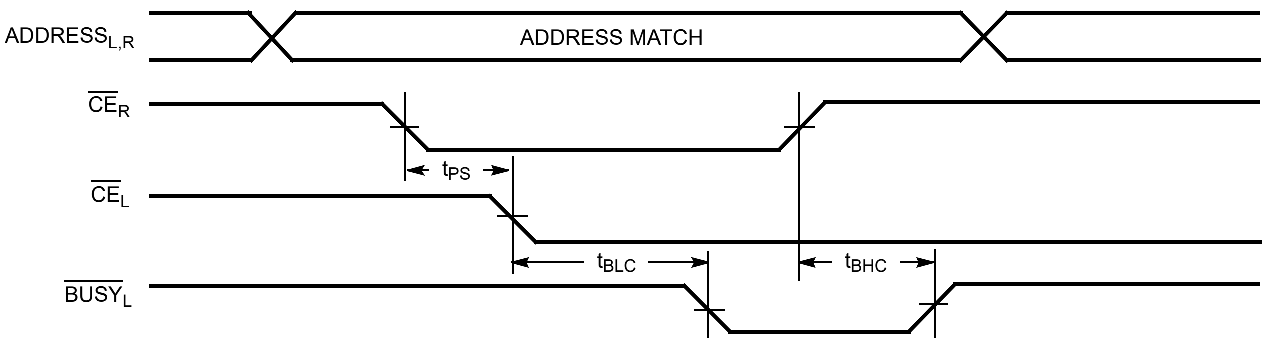
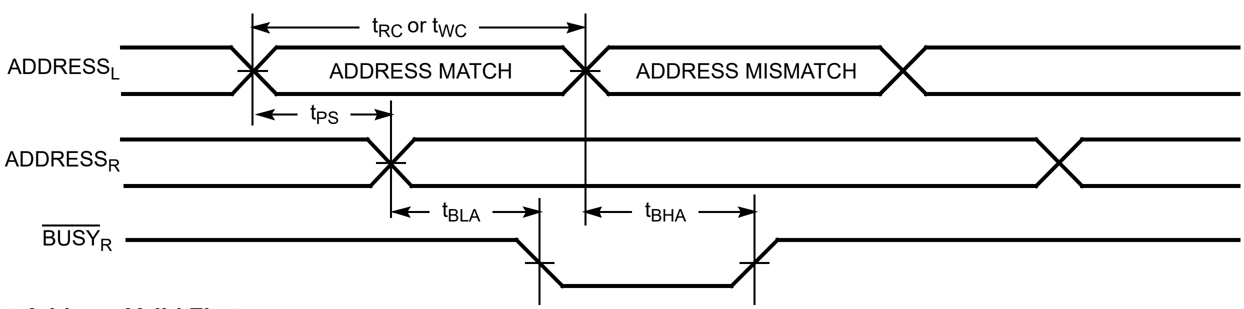
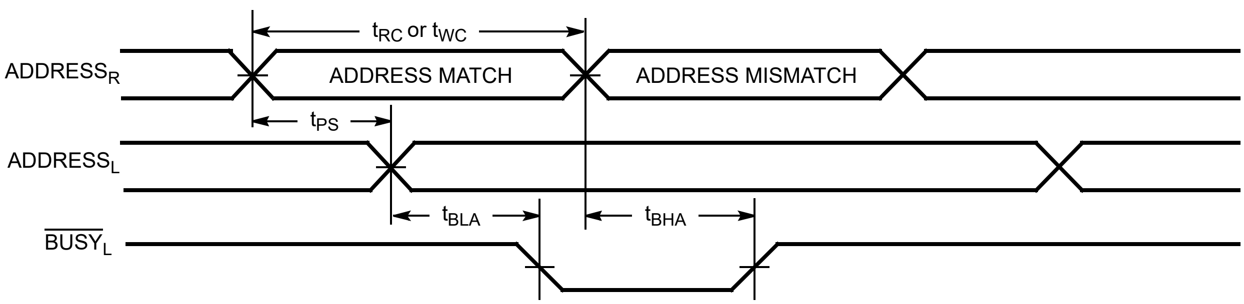


Figure 13. Busy Timing Diagram No. 2 (Address Arbitration) [37]

Left Address Valid First:



Right Address Valid First:

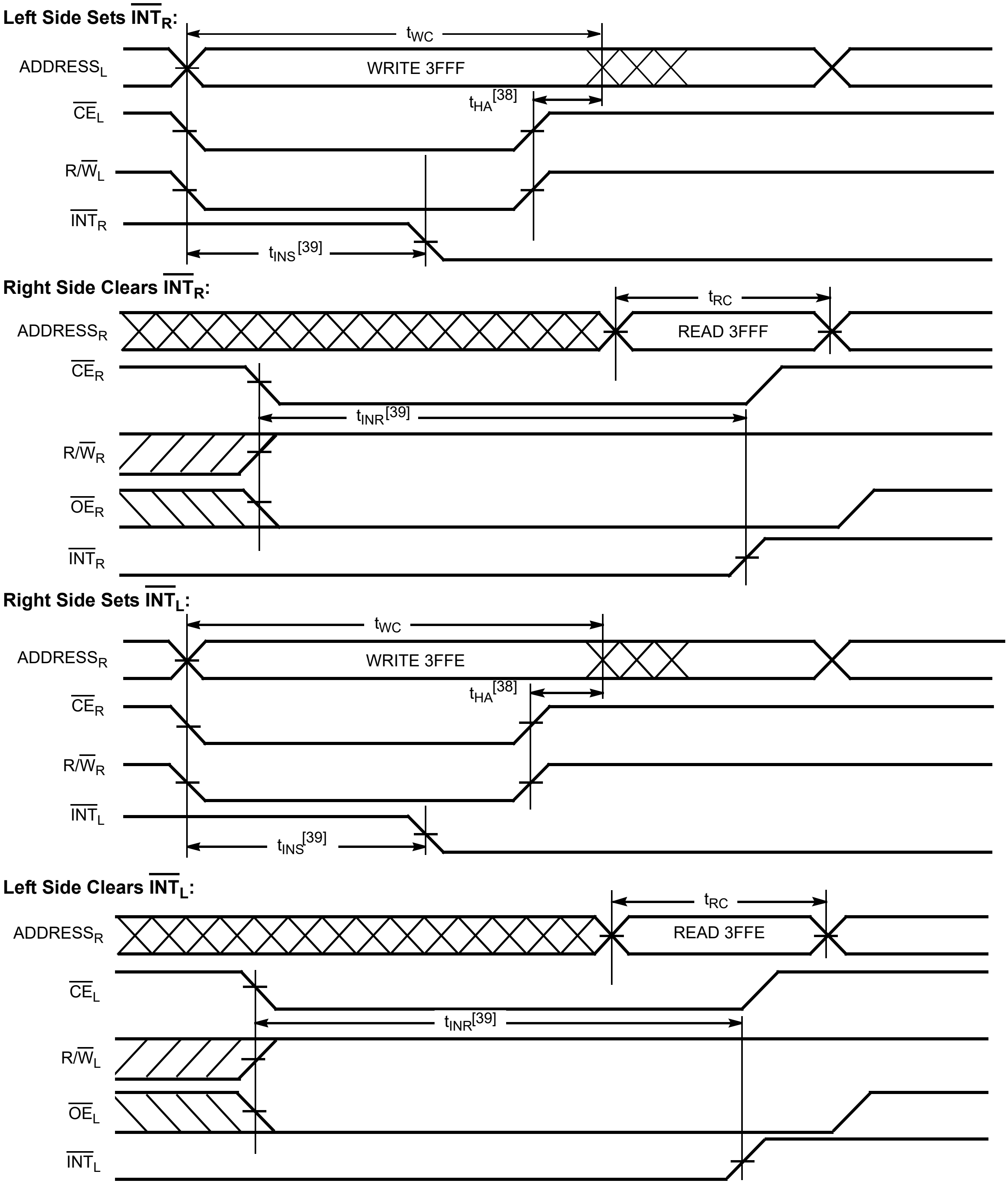


Note

37. If t_{PS} is violated, the busy signal is asserted on one side or the other, but there is no guarantee to which side $\overline{BUSY}$ is asserted.

Switching Waveforms (continued)

Figure 14. Interrupt Timing Diagrams



Notes

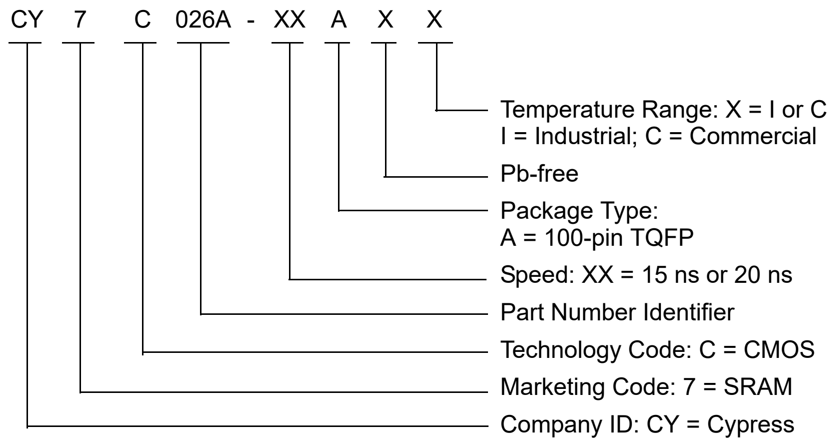
38. t_{HA} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is deasserted first.
39. t_{INS} or t_{INR} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is asserted last.

Ordering Information

16K × 16 Asynchronous Dual-Port SRAM

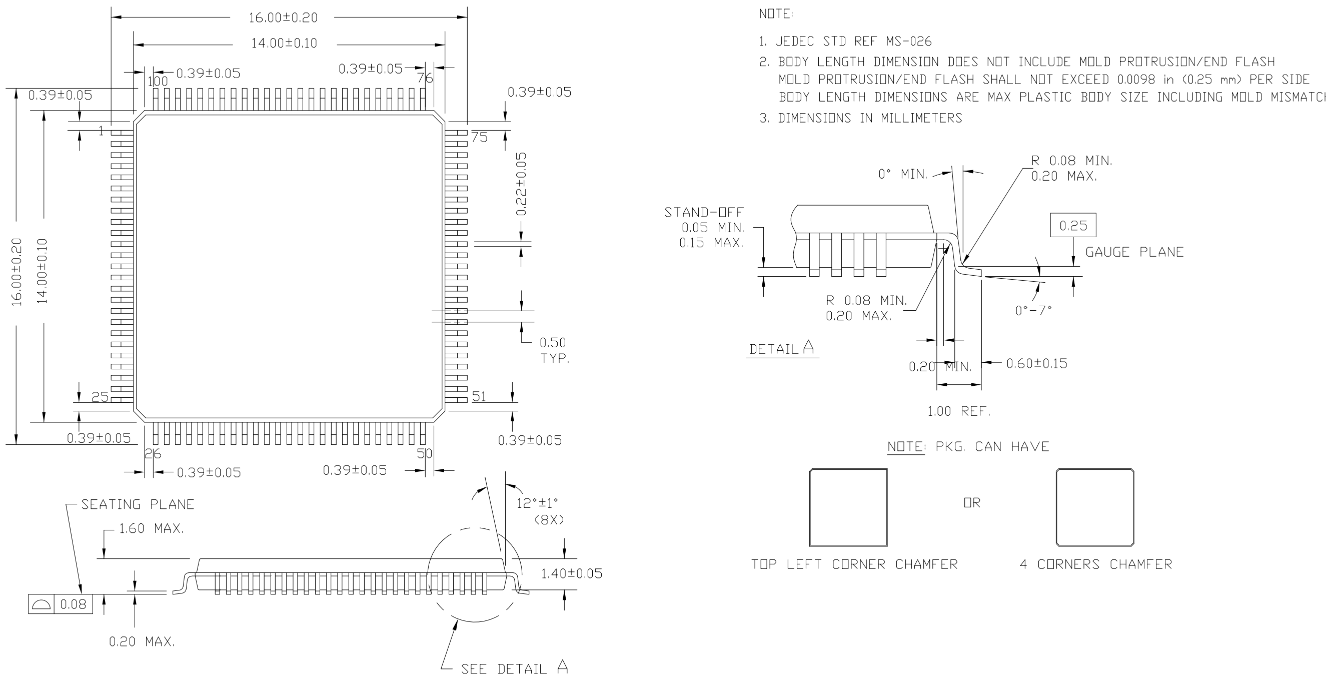
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C026A-15AXI	A100	100-pin TQFP (Pb-free)	Industrial
20	CY7C026A-20AXC	A100	100-pin TQFP (Pb-free)	Commercial

Ordering Code Definitions



Package Diagram

Figure 15. 100-pin TQFP (14 × 14 × 1.4 mm) Package Outline, 51-85048



51-85048 *K

Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
SRAM	Static Random Access Memory
TQFP	Thin Quad Flat Pack

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mV	millivolt
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C026A, 16K × 16 Dual-Port Static RAM
Document Number: 38-06046

Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	110198	SZV	09/29/2001	Changed from Spec number: 38-00832 to 38-06046
*A	122296	RBI	12/27/2002	Updated Maximum Ratings: Added Note 4 and referred the same note in maximum ratings.
*B	237621	YDT	06/25/2004	Updated Features: Removed “Pin-compatible and functionally equivalent to IDT70261”.
*C	393454	YIM	09/07/2005	Added Pb-free Logo. Updated Ordering Information: Updated part numbers.
*D	2623540	VKN / PYRS	12/17/2008	Added CY7C026B part related information in all instances across the document. Updated Ordering Information: Updated part numbers.
*E	2896038	RAME	03/19/2010	Updated Ordering Information: Updated part numbers. Updated Package Diagram: spec 51-85048 – Changed revision from *C to *D.
*F	3081925	ADMU	11/10/2010	Changed title from “CY7C026A/026B, CY7C036A 16K × 16/18 Dual-Port Static RAM” to “CY7C026A, 16K × 16 Dual-Port Static RAM”. Removed CY7C026B and CY7C036A part related information in all instances across the document. Removed 12 ns speed bin related information in all instances across the document. Updated Ordering Information: No change in part numbers. Added Ordering Code Definitions. Added Acronyms and Units of Measure. Updated to new template. Completing Sunset Review.
*G	3403652	ADMU	10/14/2011	Updated Ordering Information: Updated part numbers. Updated Package Diagram: spec 51-85048 – Changed revision from *D to *E. Completing Sunset Review.
*H	3799343	SMCH	10/31/2012	Updated Logic Block Diagram (No change in diagram, removed the notes “I/O_8–I/O_{15} for × 16 devices.” and “I/O_0–I/O_7 for × 16 devices.” and their references in Logic Block Diagram). Updated Functional Overview (Updated Write Operation (Updated Table 1 (Replaced “X” with “H” for $\overline{CE}$ inputs of “Read data in semaphore flag” and “Write D_{IN0} into semaphore flag” operations))). Updated Switching Characteristics (Updated Note 10 (Removed “$\overline{UB}$ = L”)). Updated Switching Waveforms (Updated Note 22 (Removed “$\overline{UB}$ or $\overline{LB}$ = V_{IL}”), updated Figure 9 (Replaced “MATCH” with “ADDRESS MATCH”), updated Figure 10 (Replaced “MATCH” with “ADDRESS MATCH”)). Updated Package Diagram: spec 51-85048 – Changed revision from *E to *G. Completing Sunset Review.
*I	4580622	SMCH	11/26/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Updated Package Diagram: spec 51-85048 – Changed revision from *G to *I.

Document History Page (continued)

Document Title: CY7C026A, 16K × 16 Dual-Port Static RAM Document Number: 38-06046				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*J	5018928	NILE	11/18/2015	Updated Package Diagram: spec 51-85048 – Changed revision from *I to *J. Updated to new template. Completing Sunset Review.
*K	5995408	NILE	11/14/2018	Updated Package Diagram: spec 51-85048 – Changed revision from *J to *K. Updated to new template. Completing Sunset Review.

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