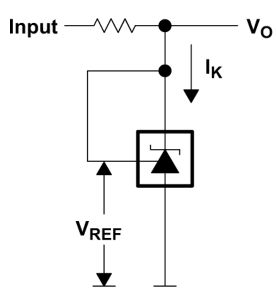
TLV431x Low-Voltage Adjustable Precision Shunt Regulator

1 Features

- Low-voltage operation, V_{REF} = 1.24V
- Adjustable output voltage, V_O = V_{REF} to 6V
- Reference voltage tolerances at 25°C
  - 0.5% for TLV431B
  - 1% for TLV431A
  - 1.5% for TLV431
- Typical temperature drift
  - 4mV (0°C to 70°C)
  - 6mV (–40°C to 85°C)
  - 11mV (–40°C to 125°C)
- Low operational cathode current, 80μA typical
- 0.25Ω typical output impedance
- Ultra-small SC-70 package offers 40% smaller footprint than SOT-23-3
- See TLVH431 and TLVH432 for:
  - Wider V_{KA} (1.24V to 18 V) and I_K (80mA)
  - Additional SOT-89 package
  - Multiple pinouts for SOT-23-3 and SOT-89 packages
- On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. on all other products, production processing does not necessarily include testing of all parameters.

2 Applications

- Adjustable voltage and current referencing
- Secondary side regulation in flyback SMPSs
- Zener replacement
- Voltage monitoring
- Comparator with integrated reference



Simplified Schematic

3 Description

The TLV431 device is a low-voltage 3-terminal adjustable voltage reference with specified thermal stability over applicable industrial and commercial temperature ranges. Output voltage can be set to any value between V_{REF} (1.24V) and 6V with two external resistors (see the *Parameter Measurement Information* section). These devices operate from a lower voltage (1.24V) than the widely used TL431 and TL1431 shunt-regulator references.

When used with an optocoupler, the TLV431 device is an ideal voltage reference in isolated feedback circuits for 3V to 3.3V switching-mode power supplies. These devices have a typical output impedance of 0.25Ω. Active output circuitry provides a very sharp turnon characteristic, making them excellent replacements for low-voltage Zener diodes in many applications, including on-board regulation and adjustable power supplies.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TLV431	DBZ (SOT-23, 3)	2.92mm × 2.37mm
	DBV (SOT-23, 5)	2.90mm × 2.8mm
	LP (TO-92, 3)	5.2mm × 3.68mm
	PK (SOT-89, 3)	4.5mm × 4.095mm
TLV431A	DBV (SOT-23, 5)	2.90mm × 2.8mm
	DBZ (SOT-23, 3)	2.92mm × 2.37mm
	PK (SOT-89, 3)	4.5mm × 4.095mm
	LP (TO-92, 3)	5.2mm × 3.68mm
	D (SOIC, 8)	4.9mm × 6mm
TLV431B	DBV (SOT-23, 5)	2.90mm × 2.8mm
	DBZ (SOT-23, 3)	2.92mm × 2.37mm
	PK (SOT-89, 3)	4.5mm × 4.095mm
	LP (TO-92, 3)	5.2mm × 3.68mm
	DCK (SOT-SC70, 6)	2mm × 1.5mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable

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4 Pin Configuration and Functions

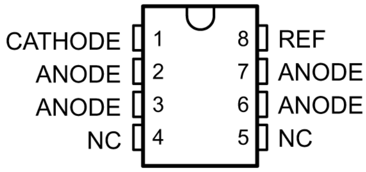
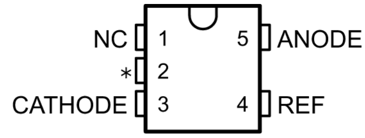


Figure 4-1. D (SOIC) Package (Top View)



NC − No internal connection

* Pin 2 is attached to Substrate and must be connected to ANODE or left open.

Figure 4-2. DBV (SOT-23-5) Package (Top View)

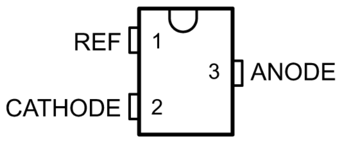


Figure 4-3. DBZ (SOT-23-3) Package (Top View)

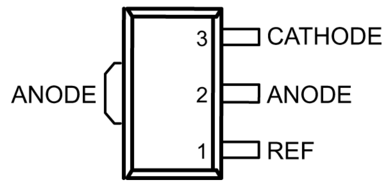


Figure 4-4. PK (SOT-89) Package (Top View)

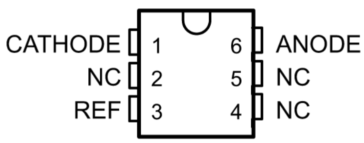


Figure 4-5. DCK (SC-70) Package (Top View)

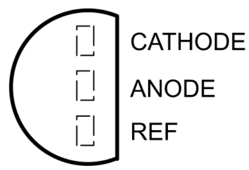


Figure 4-6. LP (TO-92/TO-226) Package (Top View)

Table 4-1. Pin Functions

PIN							TYPE	DESCRIPTION
NAME	DBZ	DBV	PK	D	LP	DCK		
CATHODE	2	3	3	1	1	1	I/O	Shunt Current/Voltage input
REF	1	4	1	8	3	3	I	Threshold relative to common anode
ANODE	3	5	2	2, 3, 6, 7	2	6	O	Common pin, normally connected to ground
NC	—	1	—	4, 5	—	2, 4, 5	I	No Internal Connection
*	—	2	—	—	—	—	I	Substrate Connection

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
V_{KA}	Cathode voltage[(2)]		7	V
I_K	Continuous cathode current	–20	20	mA
I_{ref}	Reference current	–0.05	3	mA
	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage values are with respect to the anode terminal, unless otherwise noted.

5.2 ESD Ratings

PARAMETER		DEFINITION	VALUE	UNIT
V(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{KA}	Cathode voltage		V_{REF}	6	V
I_K	Cathode current		0.1	15	mA
T_A	Operating free-air temperature	TLV431_C	0	70	°C
		TLV431_I	–40	85	
		TLV431_Q	–40	125	

5.4 Thermal Information

THERMAL METRIC[(1)]		TLV431x						UNIT
		DCK	D	PK	DBV	DBZ	LP	
		6 PINS	8 PINS	3 PINS	5 PINS	3 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	87	97	52	206	206	140	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	259	39	9	131	76	55	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

5.5 Electrical Characteristics for TLV431

at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TLV431 MIN	TLV431 TYP	TLV431 MAX	UNIT
V_{REF}	Reference voltage	$V_{KA} = V_{REF}$, I_K=10mA	T_A = 25°C		1.222	1.24	1.258	V
			T_A = full range(1) (see Figure 6-1)	TLV431C	1.21		1.27	
				TLV431I	1.202		1.278	
				TLV431Q	1.194		1.286	
$V_{REF(dev)}$	V_{REF} deviation over full temperature range(2)	$V_{KA} = V_{REF}$, I_K = 10mA(1) (see Figure 6-1)		TLV431C		4	12	mV
				TLV431I		6	20	
				TLV431Q		11	31	
$\frac{\Delta V_{REF}}{\Delta V_{KA}}$	Ratio of V_{REF} change in cathode voltage change	$V_{KA} = V_{REF}$ to 6V, I_K = 10mA (see Figure 6-2)				-1.5	-2.7	mV/V
I_{ref}	Reference terminal current	I_K = 10mA, R1 = 10kΩ, R2 = open (see Figure 6-2)				0.15	0.5	µA
$I_{ref(dev)}$	I_{ref} deviation over full temperature range(2)	I_K = 10mA, R1 =10kΩ, R2 = open(1) (see Figure 6-2)		TLV431C		0.05	0.3	µA
				TLV431I		0.1	0.4	
				TLV431Q		0.15	0.5	
$I_{K(min)}$	Minimum cathode current for regulation	$V_{KA} = V_{REF}$ (see Figure 6-1)		TLV431C/I		55	80	µA
				TLV431Q		55	100	
$I_{K(off)}$	Off-state cathode current	V_{REF} = 0, V_{KA} = 6V (see Figure 6-3)				0.001	0.1	µA
$\lvert z_{KA} \rvert$	Dynamic impedance(3)	$V_{KA} = V_{REF}$, f ≤ 1kHz, I_K = 0.1mA to 15mA (see Figure 6-1)				0.25	0.4	Ω

(1) Full temperature ranges are –40°C to 125°C for TLV431Q, –40°C to 85°C for TLV431I, and 0°C to 70°C for TLV431C.

(2) The deviation parameters $V_{REF(dev)}$ and $I_{ref(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage, αV_{REF}, is defined as:

$$\left|\alpha V_{REF}\right|\left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{REF(dev)}}{V_{REF}\left(T_A = 25°C\right)}\right) \times 10^6}{\Delta T_A}$$

where ΔT_A is the rated operating free-air temperature range of the device. αV_{REF} can be positive or negative, depending on whether minimum V_{REF} or maximum V_{REF}, respectively, occurs at the lower temperature.

(3) The dynamic impedance is defined as $\left|z_{ka}\right| = \frac{\Delta V_{KA}}{\Delta I_K}$. When the device is operating with two external resistors (see Figure 6-2), the total dynamic impedance of the circuit is defined as: $\left|z_{ka}\right|' = \frac{\Delta V}{\Delta I} \approx \left|z_{ka}\right| \times \left(1 + \frac{R1}{R2}\right)$

5.6 Electrical Characteristics for TLV431A

at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TLV431A MIN	TLV431A TYP	TLV431A MAX	UNIT
V_{REF}	Reference voltage	$V_{KA} = V_{REF}$, I_K = 10mA	T_A = 25°C		1.228	1.24	1.252	V
			T_A = full range[(1)] (see Figure 6-1)	TLV431AC	1.221		1.259	
				TLV431AI	1.215		1.265	
				TLV431AQ	1.209		1.271	
$V_{REF(dev)}$	V_{REF} deviation over full temperature range[(2)]	$V_{KA} = V_{REF}$, I_K = 10mA[(1)] (see Figure 6-1)		TLV431AC		4	12	mV
				TLV431AI		6	20	
				TLV431AQ		11	31	
$\frac{\Delta V_{REF}}{\Delta V_{KA}}$	Ratio of V_{REF} change in cathode voltage change	$V_{KA} = V_{REF}$ to 6V, I_K = 10mA (see Figure 6-2)				-1.5	-2.7	mV/V
I_{ref}	Reference terminal current	I_K = 10mA, R1 = 10kΩ, R2 = open (see Figure 6-2)				0.15	0.5	µA
$I_{ref(dev)}$	I_{ref} deviation over full temperature range[(2)]	I_K = 10mA, R1 = 10kΩ, R2 = open[(1)] (see Figure 6-2)		TLV431AC		0.05	0.3	µA
				TLV431AI		0.1	0.4	
				TLV431AQ		0.15	0.5	
$I_{K(min)}$	Minimum cathode current for regulation	$V_{KA} = V_{REF}$ (see Figure 6-1)		TLV431AC/AI		55	80	µA
				TLV431AQ		55	100	
$I_{K(off)}$	Off-state cathode current	V_{REF} = 0, V_{KA} = 6V (see Figure 6-3)				0.001	0.1	µA
$\lvert z_{KA}\rvert$	Dynamic impedance [(3)]	$V_{KA} = V_{REF}$, f ≤ 1kHz, I_K = 0.1mA to 15mA (see Figure 6-1)				0.25	0.4	Ω

(1) Full temperature ranges are –40°C to 125°C for TLV431Q, –40°C to 85°C for TLV431I, and 0°C to 70°C for TLV431C.

(2) The deviation parameters $V_{REF(dev)}$ and $I_{ref(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage, αV_{REF}, is defined as:

$$\left|\alpha V_{REF}\right|\left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{REF(dev)}}{V_{REF}\left(T_A = 25°C\right)}\right)\times 10^6}{\Delta T_A}$$

where ΔT_A is the rated operating free-air temperature range of the device. αV_{REF} can be positive or negative, depending on whether minimum V_{REF} or maximum V_{REF}, respectively, occurs at the lower temperature.

(3) The dynamic impedance is defined as $\left|z_{ka}\right| = \frac{\Delta V_{KA}}{\Delta I_K}$. When the device is operating with two external resistors (see Figure 6-2), the total dynamic impedance of the circuit is defined as: $\left|z_{ka}\right|' = \frac{\Delta V}{\Delta I} \approx \left|z_{ka}\right| \times \left(1 + \frac{R1}{R2}\right)$

5.7 Electrical Characteristics for TLV431B

at 25°C free-air temperature (unless otherwise noted)

<table>
<tr><th colspan="2" rowspan="2">PARAMETER</th><th colspan="3" rowspan="2">TEST CONDITIONS</th><th colspan="3">TLV431B</th><th rowspan="2">UNIT</th></tr>
<tr><th>MIN</th><th>TYP</th><th>MAX</th></tr>
<tr><td rowspan="4">V_{REF}</td><td rowspan="4">Reference voltage</td><td rowspan="4">$V_{KA} = V_{REF}$, I_K=10mA</td><td colspan="2">T_A = 25°C</td><td>1.234</td><td>1.24</td><td>1.246</td><td rowspan="4">V</td></tr>
<tr><td rowspan="3">T_A = full range[(1)] (see Figure 6-1)</td><td>TLV431BC</td><td>1.227</td><td></td><td>1.253</td></tr>
<tr><td>TLV431BI</td><td>1.224</td><td></td><td>1.259</td></tr>
<tr><td>TLV431BQ</td><td>1.221</td><td></td><td>1.265</td></tr>
<tr><td rowspan="3">$V_{REF(dev)}$</td><td rowspan="3">V_{REF} deviation over full temperature range[(2)]</td><td colspan="2" rowspan="3">$V_{KA} = V_{REF}$, I_K = 10mA[(1)] (see Figure 6-1)</td><td>TLV431BC</td><td></td><td>4</td><td>12</td><td rowspan="3">mV</td></tr>
<tr><td>TLV431BI</td><td></td><td>6</td><td>20</td></tr>
<tr><td>TLV431BQ</td><td></td><td>11</td><td>31</td></tr>
<tr><td>$\frac{\Delta V_{REF}}{\Delta V_{KA}}$</td><td>Ratio of V_{REF} change in cathode voltage change</td><td colspan="3">$V_{KA} = V_{REF}$ to 6V, I_K = 10mA (see Figure 6-2)</td><td></td><td>-1.5</td><td>-2.7</td><td>mV/V</td></tr>
<tr><td>I_{ref}</td><td>Reference terminal current</td><td colspan="3">I_K = 10mA, R1 = 10kΩ, R2 = open (see Figure 6-2)</td><td></td><td>0.1</td><td>0.5</td><td>µA</td></tr>
<tr><td rowspan="3">$I_{ref(dev)}$</td><td rowspan="3">I_{ref} deviation over full temperature range[(2)]</td><td colspan="2" rowspan="3">I_K = 10mA, R1 =10kΩ, R2 = open[(3)] (see Figure 6-2)</td><td>TLV431BC</td><td></td><td>0.05</td><td>0.3</td><td rowspan="3">µA</td></tr>
<tr><td>TLV431BI</td><td></td><td>0.1</td><td>0.4</td></tr>
<tr><td>TLV431BQ</td><td></td><td>0.15</td><td>0.5</td></tr>
<tr><td>$I_{K(min)}$</td><td>Minimum cathode current for regulation</td><td colspan="3">$V_{KA} = V_{REF}$ (see Figure 6-1)</td><td></td><td>55</td><td>100</td><td>µA</td></tr>
<tr><td>$I_{K(off)}$</td><td>Off-state cathode current</td><td colspan="3">V_{REF} = 0, V_{KA} = 6V (see Figure 6-3)</td><td></td><td>0.001</td><td>0.1</td><td>µA</td></tr>
<tr><td>$|z_{KA}|$</td><td>Dynamic impedance[(4)]</td><td colspan="3">$V_{KA} = V_{REF}$, f ≤ 1kHz, I_K = 0.1mA to 15mA (see Figure 6-1)</td><td></td><td>0.25</td><td>0.4</td><td>Ω</td></tr>
</table>

(1) Full temperature ranges are –40°C to 125°C for TLV431Q, –40°C to 85°C for TLV431I, and 0°C to 70°C for TLV431C.

(2) The deviation parameters VREF(dev) and Iref(dev) are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full-range temperature coefficient of the reference input voltage, αV_{REF}, is defined as:

$$\left|\alpha V_{REF}\right|\left(\frac{ppm}{°C}\right)=\frac{\left(\frac{V_{REF(dev)}}{V_{REF}\left(T_A = 25°C\right)}\right)\times 10^6}{\Delta T_A}$$

where ΔT_A is the rated operating free-air temperature range of the device. αV_{REF} can be positive or negative, depending on whether minimum V_{REF} or maximum V_{REF}, respectively, occurs at the lower temperature.

(3) Full temperature ranges are –40°C to 125°C for TLV431Q, –40°C to 85°C for TLV431I, and 0°C to 70°C for TLV431C.

(4) dynamic impedance is defined as $|z_{ka}| = \frac{\Delta V_{KA}}{\Delta I_K}$. When the device is operating with two external resistors (see Figure 6-2), the total dynamic impedance of the circuit is defined as: $|z_{ka}|' = \frac{\Delta V}{\Delta I} \approx |z_{ka}| \times \left(1+\frac{R1}{R2}\right)$

5.8 Typical Characteristics

Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.

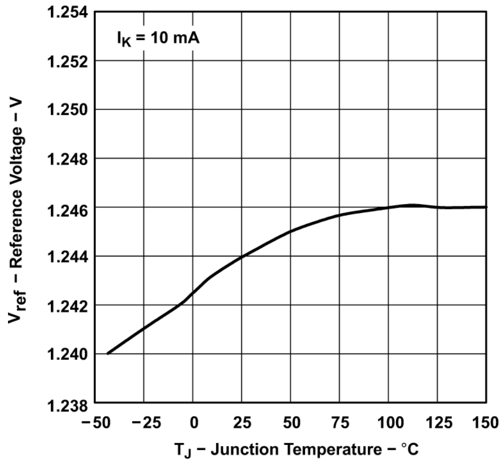


Figure 5-1. Reference Voltage vs Junction Temperature

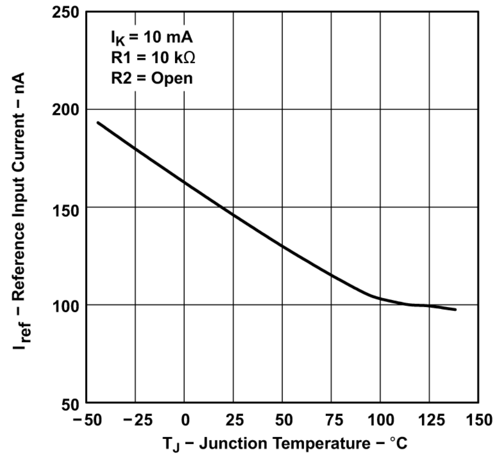


Figure 5-2. Reference Input Current vs Junction Temperature (for TLV431 and TLV431A)

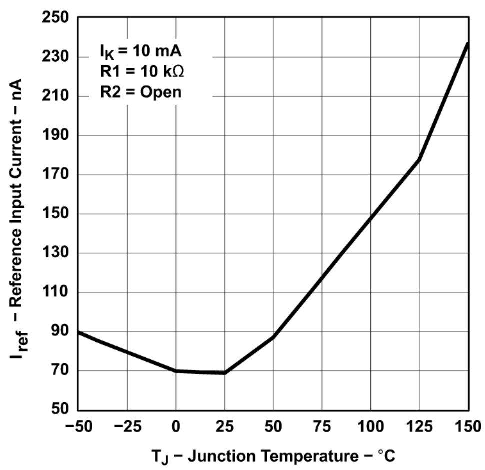


Figure 5-3. Reference Input Current vs Junction Temperature (for TLV431B)

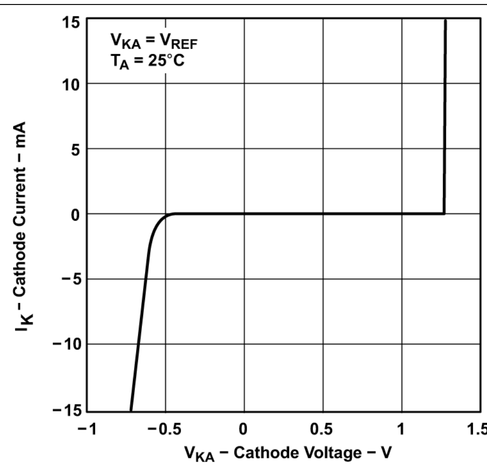


Figure 5-4. Cathode Current vs Cathode Voltage

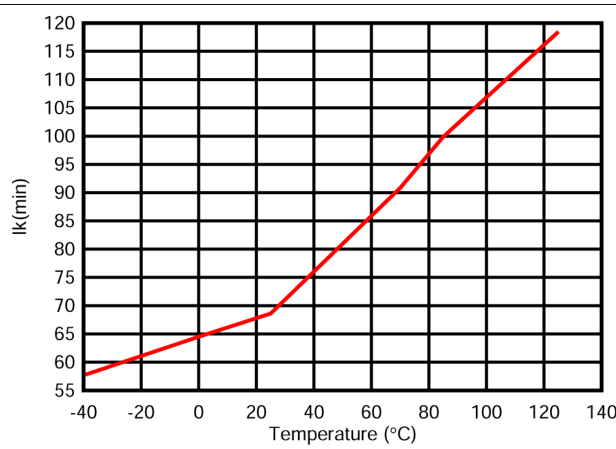


Figure 5-5. Minimum Cathode Current vs Temperature

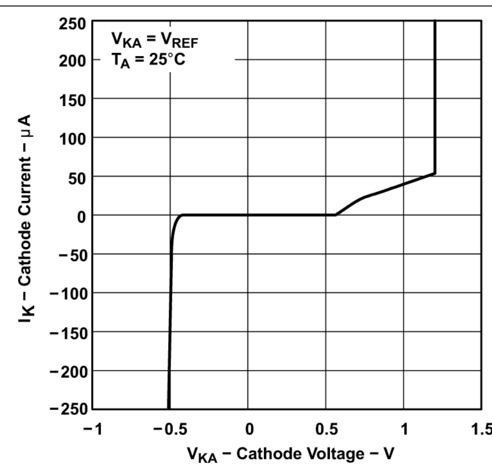


Figure 5-6. Cathode Current vs Cathode Voltage

5.8 Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.

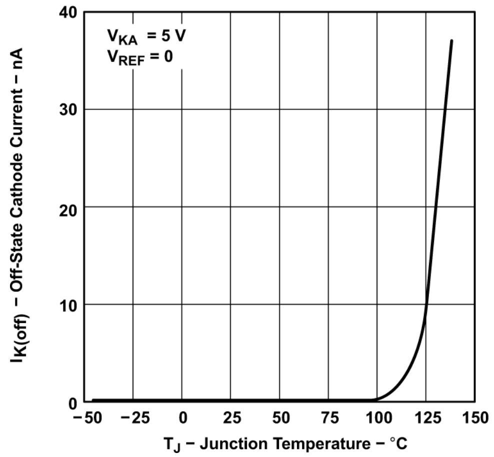


Figure 5-7. Off-State Cathode Current vs Junction Temperature (for TLV431 and TLV431A)

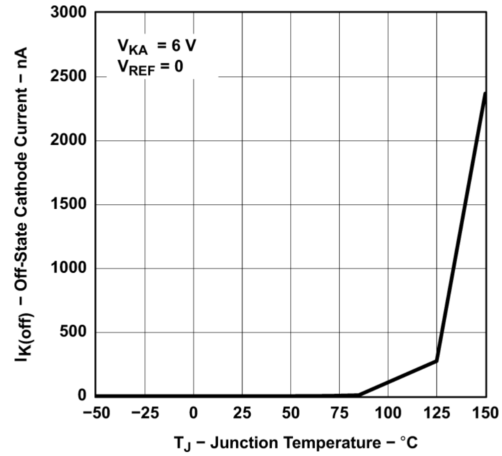


Figure 5-8. Off-State Cathode Current vs Junction Temperature (for TLV431B)

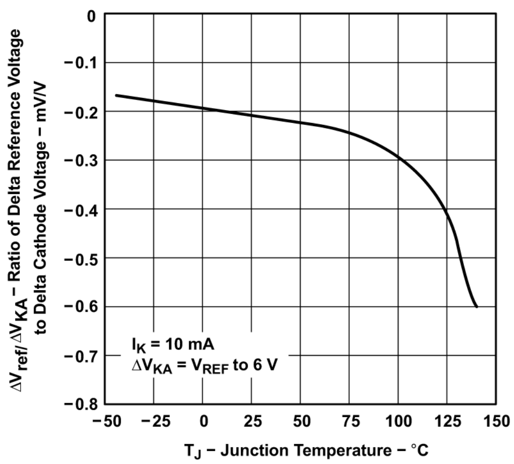


Figure 5-9. Ratio of Delta Reference Voltage to Delta Cathode Voltage vs Junction Temperature (for TLV431 and TLV431A)

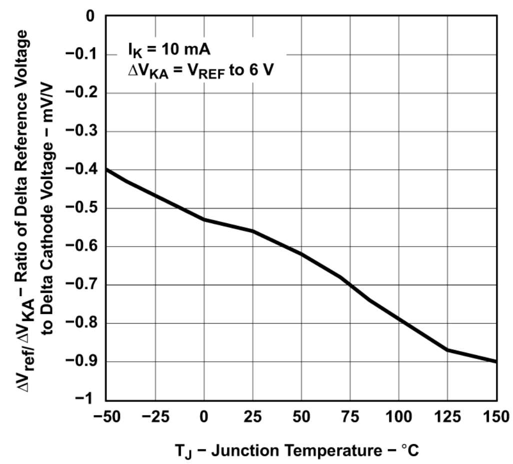


Figure 5-10. Ratio of Delta Reference Voltage to Delta Cathode Voltage vs Junction Temperature (for TLV431B)

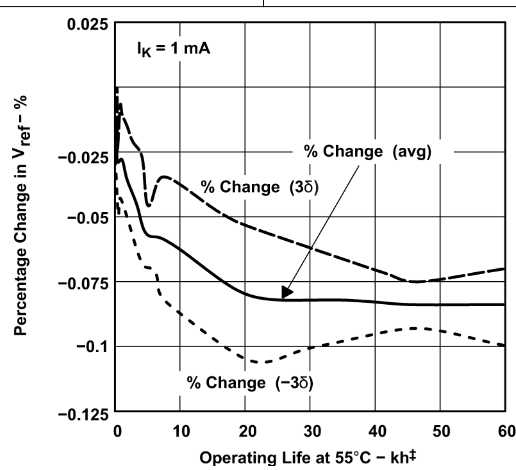


Figure 5-11. Percentage Change in v_{REF} vs Operating Life at 55°C

5.8 Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.

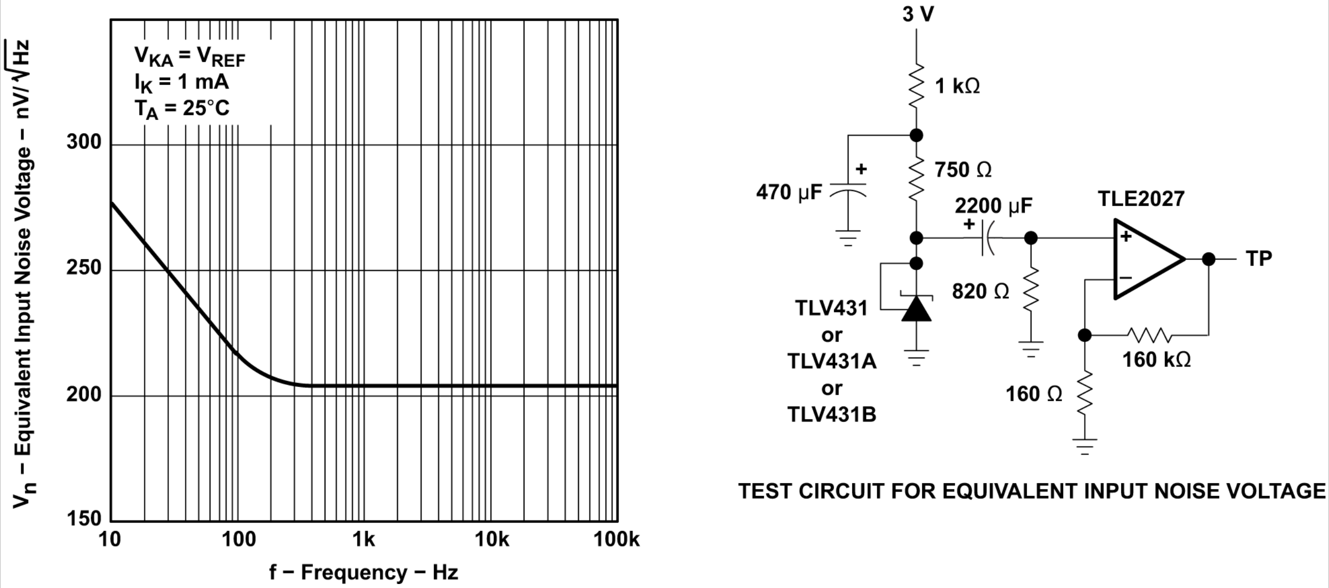


Figure 5-12. Equivalent Input Noise Voltage

5.8 Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.

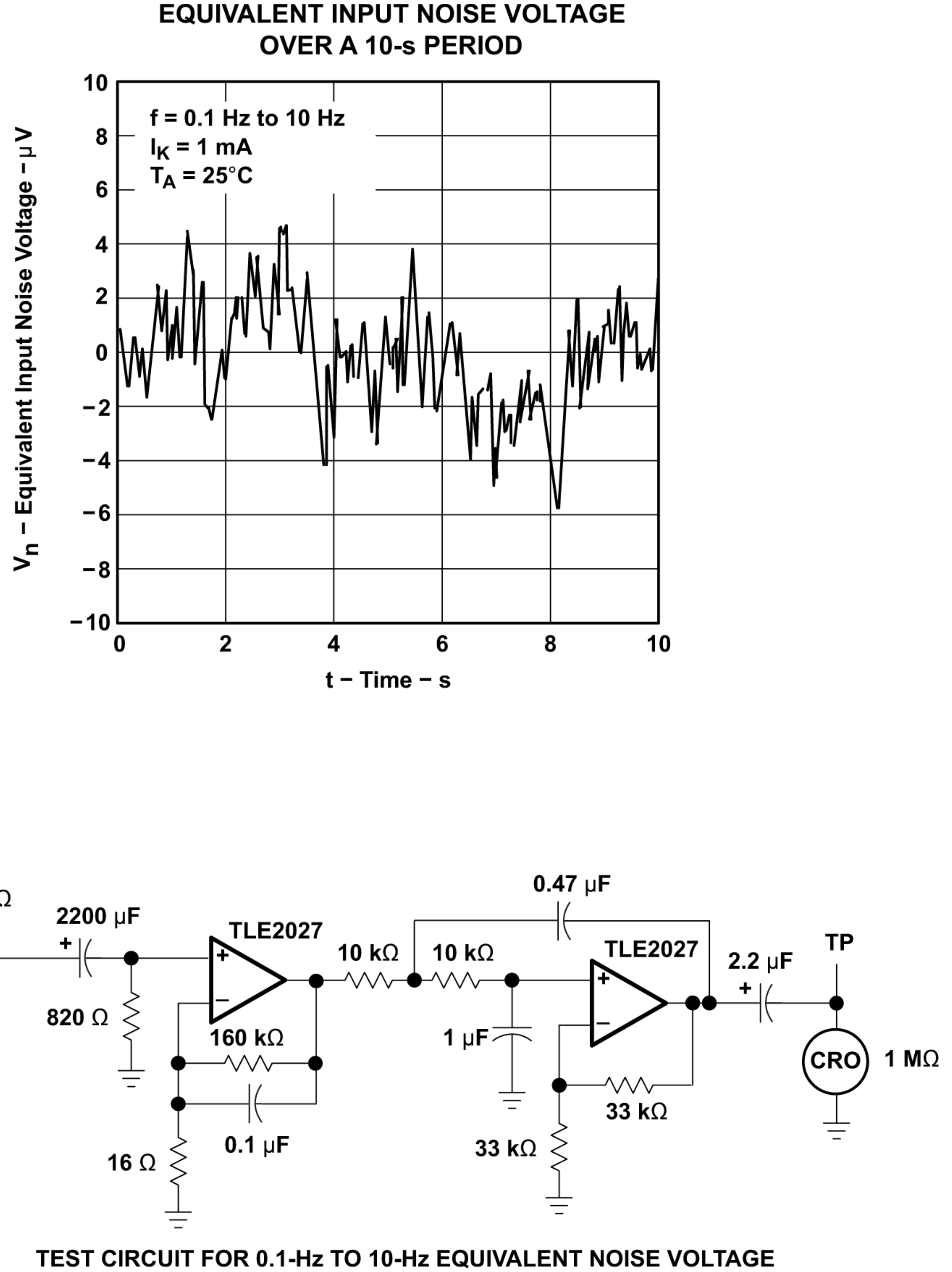


Figure 5-13. Equivalent Noise Voltage over a 10S Period

5.8 Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.

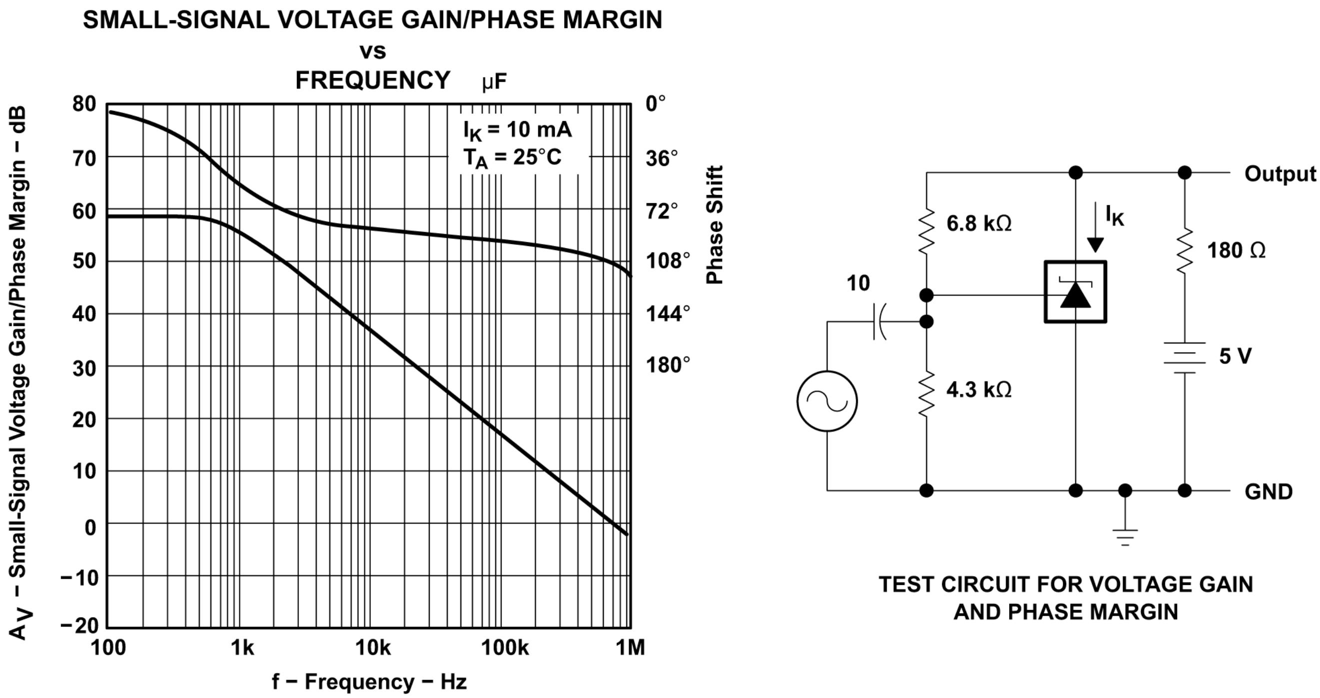


Figure 5-14. Voltage Gain and Phase Margin

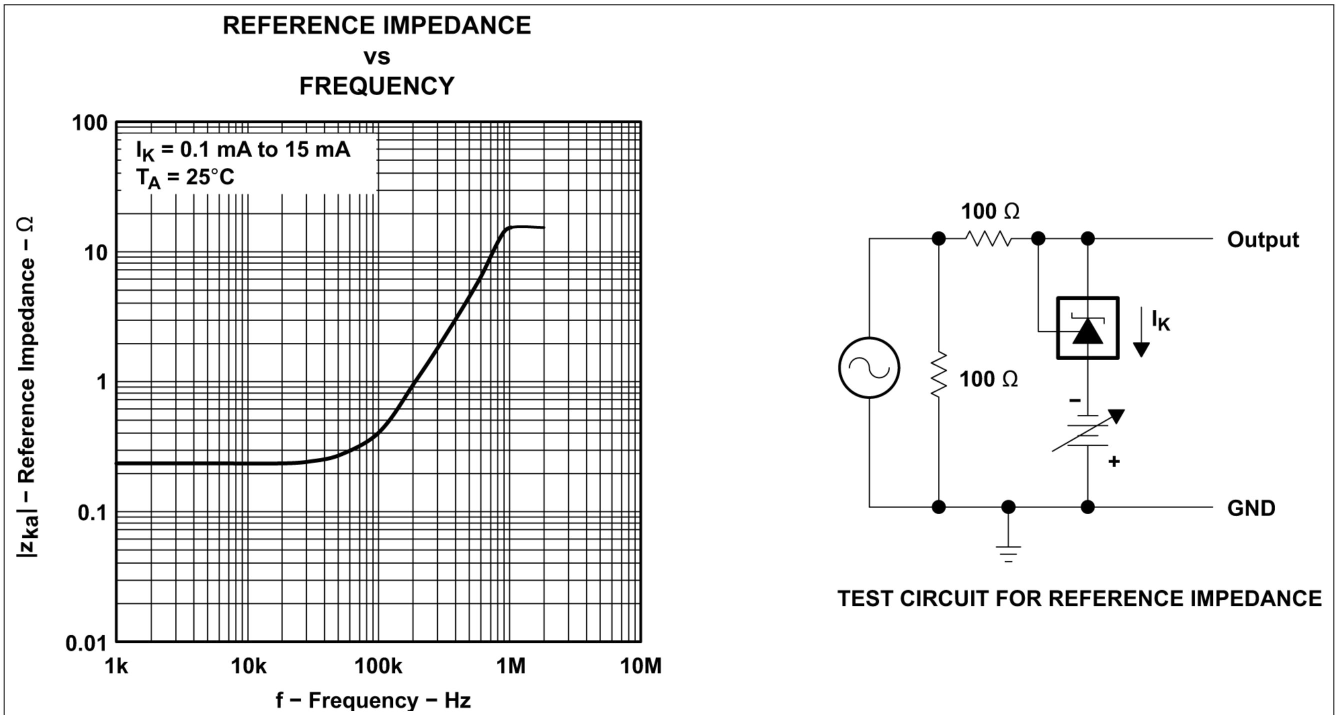


Figure 5-15. Reference Impedance vs Frequency

5.8 Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.

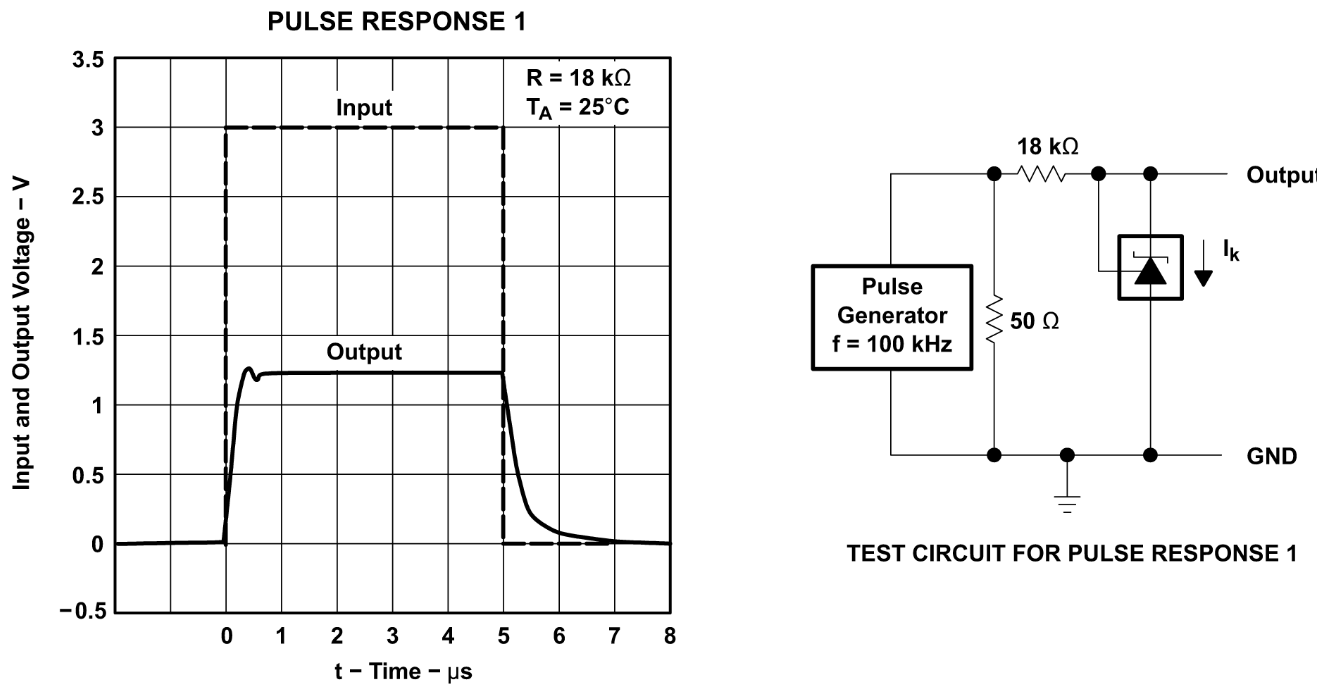


Figure 5-16. Pulse Response 1

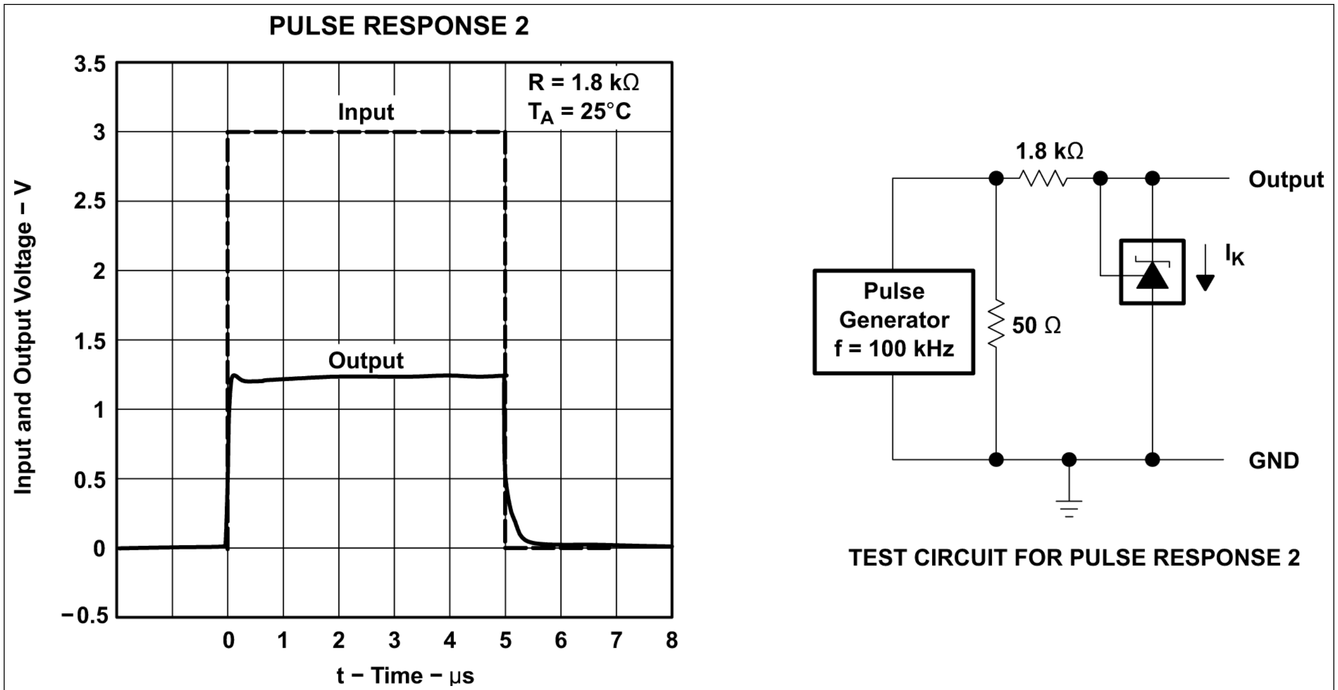
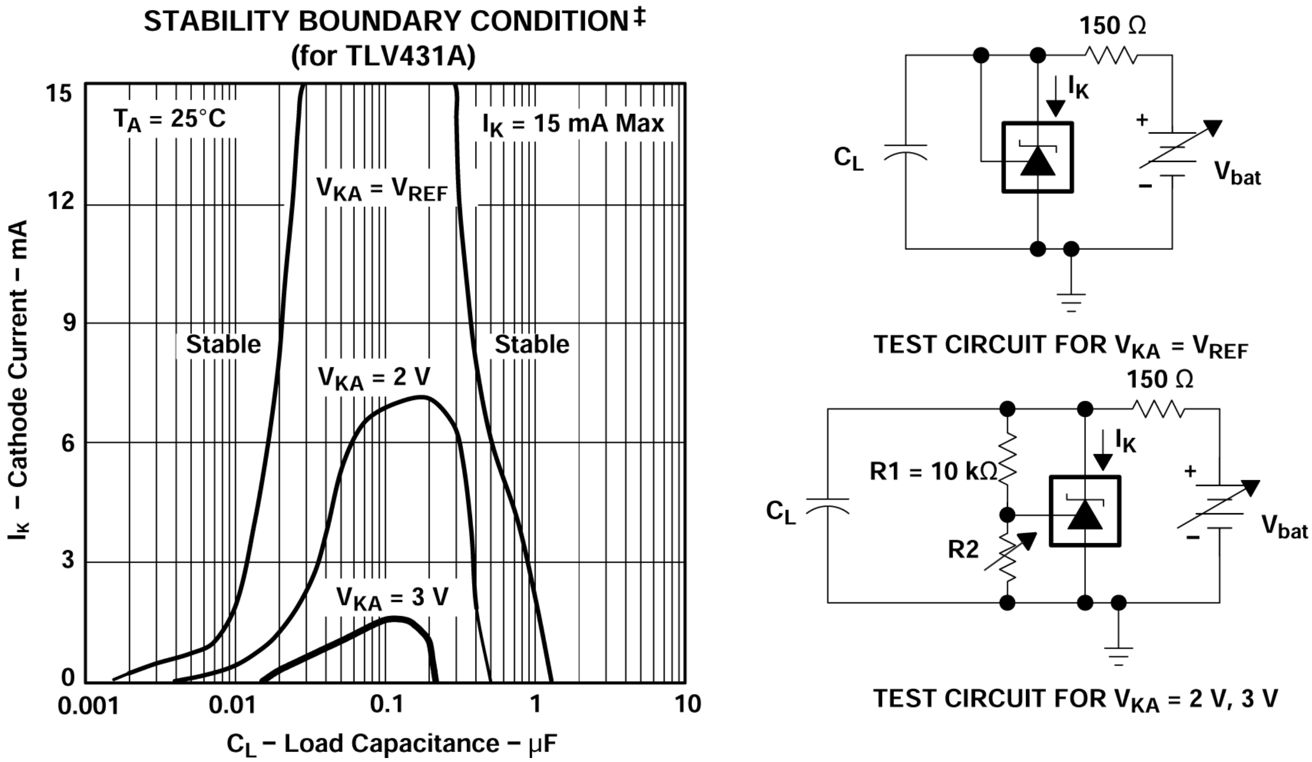


Figure 5-17. Pulse Response 2

5.8 Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.



‡The areas under the curves represent conditions that can cause the device to oscillate. For V_{KA} = 2V and 3V curves, R2 and V_{bat} were adjusted to establish the initial V_{KA} and I_K conditions with C_L = 0. V_{bat} and C_L then were adjusted to determine the ranges of stability.

Figure 5-18. Stability Boundary Conditions

5.8 Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.

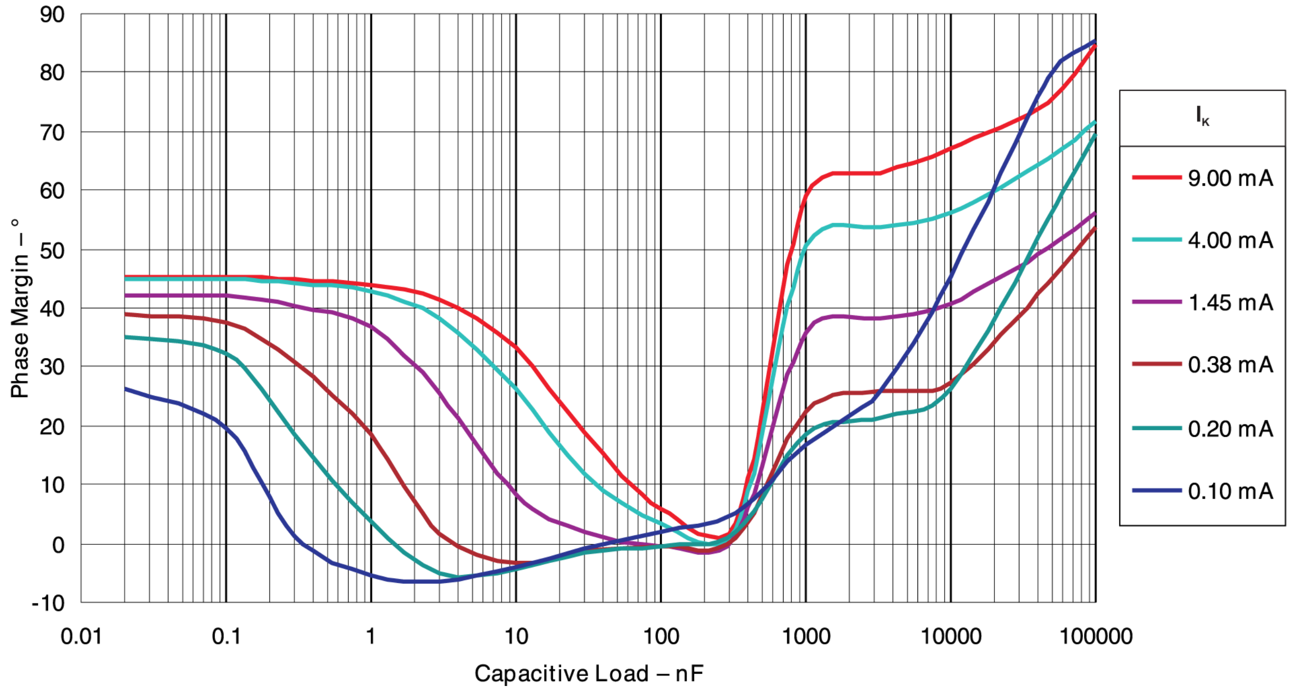


Figure 5-19. Phase Margin vs Capacitive Load v_{KA} = V_{REF} (1.25V), T_A= 25°C

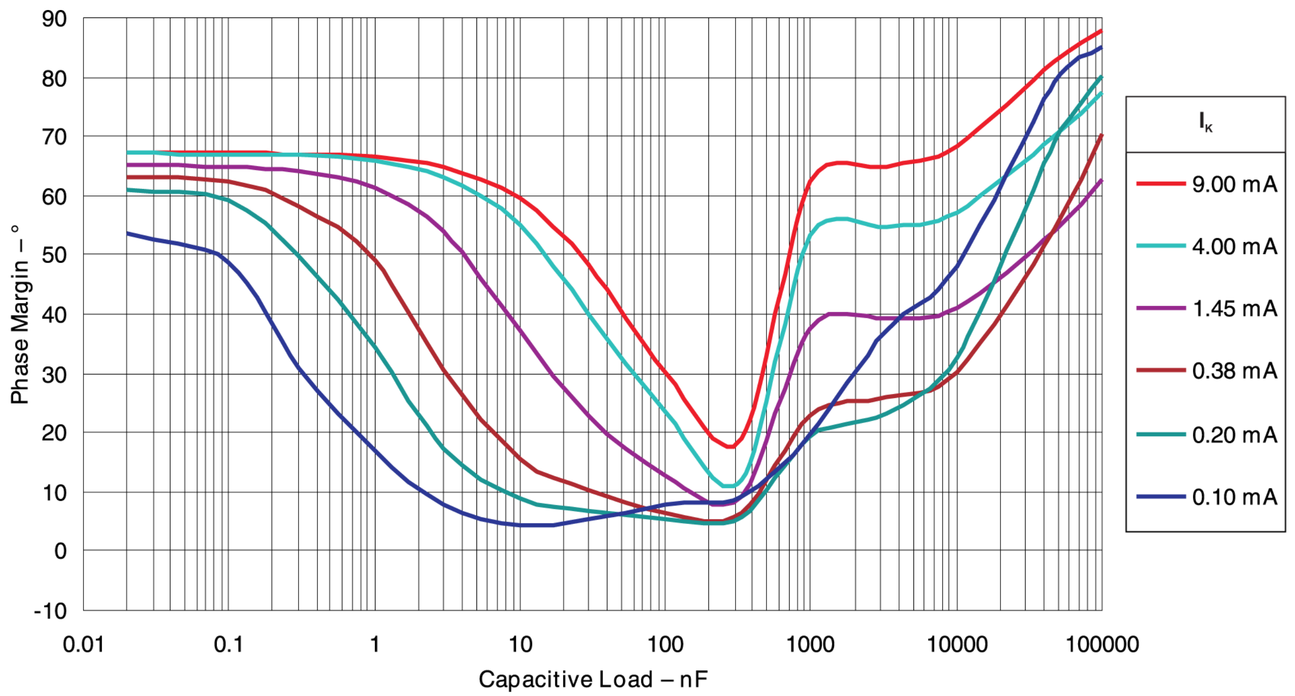


Figure 5-20. Phase Margin vs Capacitive Load v_{KA} = 2.50V, T_A= 25°C

5.8 Typical Characteristics (continued)

Operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* table are not implied.

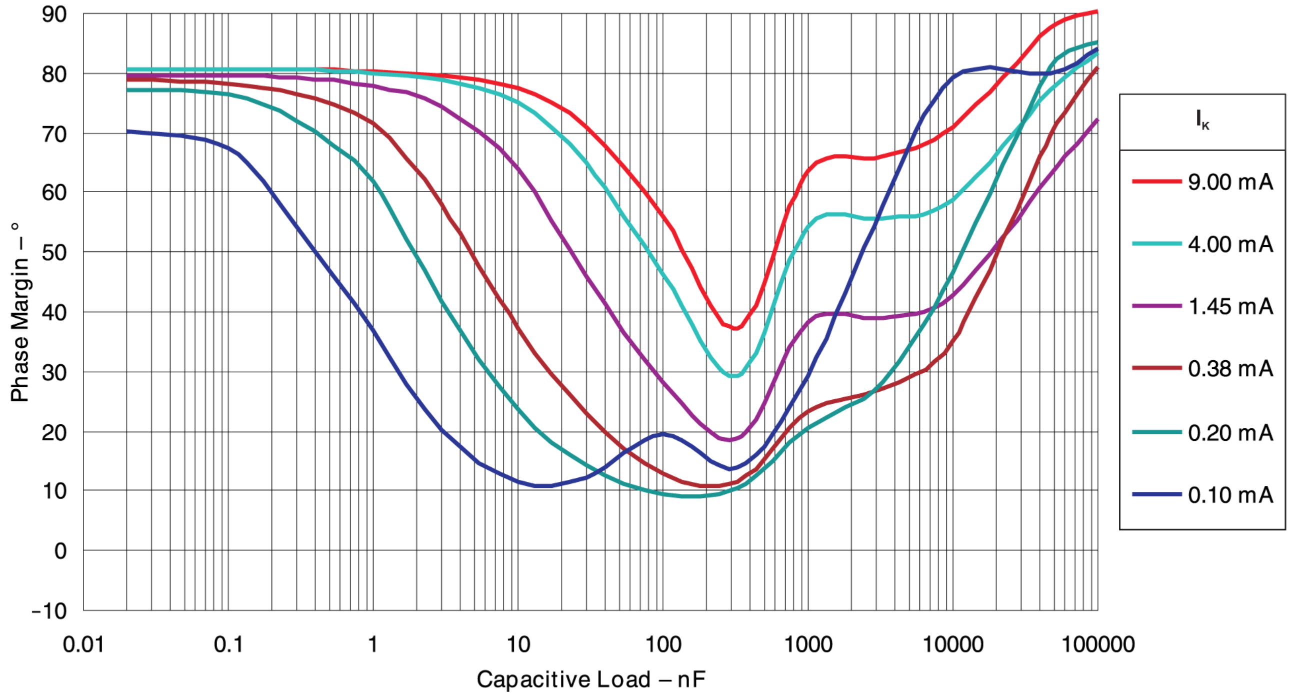


Figure 5-21. Phase Margin vs Capacitive Load v_{KA} = 5.00V, T_A= 25°C

6 Parameter Measurement Information

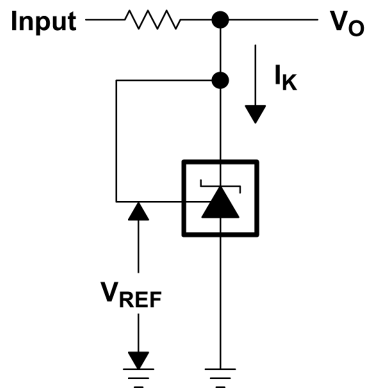


Figure 6-1. Test Circuit for $v_{KA} = V_{REF}$, $V_O = V_{KA} = V_{REF}$

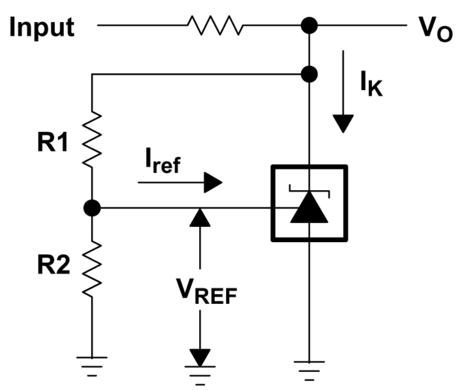


Figure 6-2. Test Circuit for $v_{KA} > V_{REF}$, $V_O = V_{KA} = V_{REF} \times (1 + R1/R2) + I_{ref} \times R1$

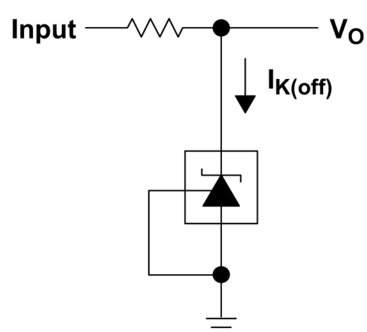


Figure 6-3. Test Circuit for $I_{K(off)}$

7 Detailed Description

7.1 Overview

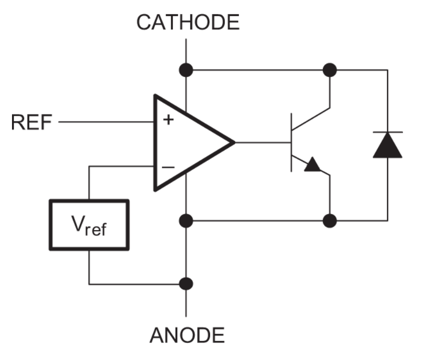
TLV431 is a low power counterpart to TL431, having lower reference voltage (1.24V vs 2.5 V) for lower voltage adjustability and lower minimum cathode current ($I_{k(min)}$= 100µA vs 1mA). Like TL431, TLV431 is used in conjunction with it's key components to behave as a single voltage reference, error amplifier, voltage clamp, or comparator with integrated reference.

TLV431 can be operated and adjusted to cathode voltages from 1.24V to 6V, making this part optimum for a wide range of end equipments in industrial, auto, telecom, and computing. For this device to behave as a shunt regulator or error amplifier, > 100µA (I_{min}(max)) must be supplied in to the cathode pin. Under this condition, feedback can be applied from the Cathode and Ref pins to create a replica of the internal reference voltage.

Various reference voltage options can be purchased with initial tolerances (at 25°C) of 0.5%, 1%, and 1.5%. These reference options are denoted by B (0.5%), A (1.0%), and blank (1.5%) after the TLV431.

The TLV431xC devices are characterized for operation from 0°C to 70°C, the TLV431xI devices are characterized for operation from –40°C to 85°C, and the TLV431xQ devices are characterized for operation from –40°C to 125°C.

7.2 Functional Block Diagram



7.3 Feature Description

TLV431 consists of an internal reference and amplifier that outputs a sink current base on the difference between the reference pin and the virtual internal pin. The sink current is produced by an internal darlington pair.

When operated with enough voltage headroom (≥ 1.24V) and cathode current (Ika), TLV431 forces the reference pin to 1.24V. However, the reference pin can not be left floating, as it requires I_{ref} ≥ 0.5µA (see the *Functional Block Diagram*). This is because the reference pin is driven into an NPN, which requires a base current to operate properly.

When feedback is applied from the Cathode and Reference pins, TLV431 behaves as a Zener diode, regulating to a constant voltage dependent on current being supplied into the cathode. This is due to the internal amplifier and reference entering the proper operating regions. The same amount of current required in the above feedback situation must be applied to this device in open-loop, servo, or error-amplifying implementations for it to be in the proper linear region giving TLV431 enough gain.

Unlike many linear regulators, TLV431 is internally compensated to be stable without an output capacitor between the cathode and anode. However, if it is desired to use an output capacitor Figure 5-19 can be used as a guide to assist in choosing the correct capacitor to maintain stability.

7.4 Device Functional Modes

7.4.1 Open Loop (Comparator)

When the cathode/output voltage or current of TLV431 is not being fed back to the reference/input pin in any form, this device is operating in open loop. With proper cathode current (Ika) applied to this device, TLV431 will have the characteristics shown in Figure 5-6. With such high gain in this configuration, TLV431 is typically used as a comparator. With the reference integrated makes TLV431 the preferred choice when users are trying to monitor a certain level of a single signal.

7.4.2 Closed Loop

When the cathode/output voltage or current of TLV431 is being fed back to the reference/input pin in any form, this device is operating in closed loop. The majority of applications involving TLV431 use it in this manner to regulate a fixed voltage or current. The feedback enables this device to behave as an error amplifier, computing a portion of the output voltage and adjusting it to maintain the desired regulation. This is done by relating the output voltage back to the reference pin in a manner to make it equal to the internal reference voltage, which can be accomplished through resistive or direct feedback.

8 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

Figure 8-1 shows the TLV431, TLV431A, or TLV431B used in a 3.3V isolated flyback supply. Output voltage V_O can be as low as reference voltage V_{REF} (1.24V ± 1%). The output of the regulator, plus the forward voltage drop of the optocoupler LED (1.24 + 1.4 = 2.64V), determine the minimum voltage that can be regulated in an isolated supply configuration. Regulated voltage as low as 2.7 Vdc is possible in the topology shown in Figure 8-1.

The 431 family of devices are prevalent in these applications, being designers go to choice for secondary side regulation. Due to this prevalence, this section will further go on to explain operation and design in both states of TLV431 that this application will see, open loop (Comparator + Vref) and closed loop (Shunt Regulator).

Further information about system stability and using a TLV431 device for compensation can be found in the application note *Compensation Design With TL431 for UCC28600* (SLUA671).

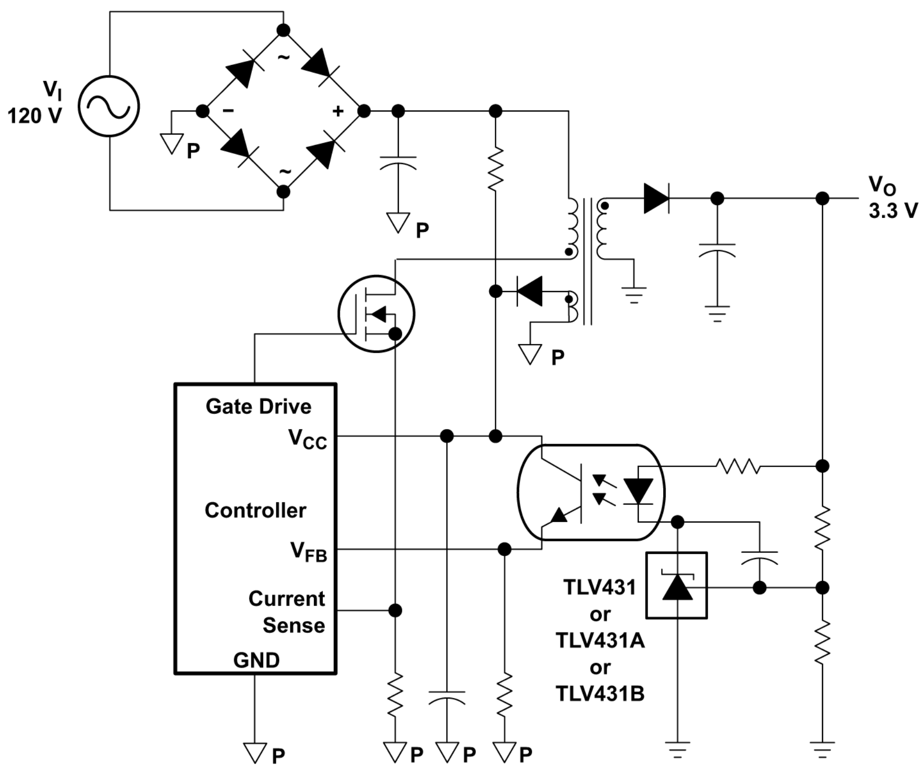


Figure 8-1. Flyback with Isolation Using TLV431, TLV431A, or TLV431B as Voltage Reference and Error Amplifier

8.2 Typical Applications

8.2.1 Comparator with Integrated Reference (Open Loop)

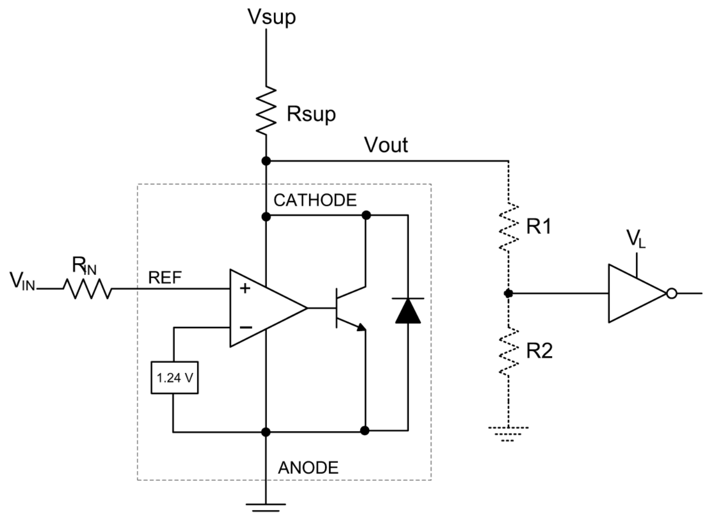


Figure 8-2. Comparator Application Schematic

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 8-1 as the input parameters.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	0V to 5V
Input Resistance	10kΩ
Supply Voltage	5V
Cathode Current (Ik)	500µA
Output Voltage Level	~1V - Vsup
Logic Input Thresholds VIH/VIL	VL

8.2.1.2 Detailed Design Procedure

When using TLV431 as a comparator with reference, determine the following:

- Input voltage range
- Reference voltage accuracy
- Output logic input high and low level thresholds
- Current source resistance

8.2.1.2.1 Basic Operation

In the configuration shown in Figure 8-2 TLV431 will behave as a comparator, comparing the V_{ref} pin voltage to the internal virtual reference voltage. When provided a proper cathode current (I_k), TLV431 will have enough open-loop gain to provide a quick response. With the TLV431's maximum operating current (I_{min}(max)) being 100µA and up to 150µA over temperature, operation below that could result in low gain, leading to a slow response.

8.2.1.2.2 Overdrive

Slow or inaccurate responses can also occur when the reference pin is not provided enough overdrive voltage. This is the amount of voltage that is higher than the internal virtual reference. The internal virtual reference voltage will be within the range of 1.24V ±(0.5%, 1.0%, or 1.5%) depending on which version is being used.

The more overdrive voltage provided, the faster the TLV431 will respond. This can be seen in Figure 8-3 and Figure 8-4 where it displays the output responses to various input voltages.

For applications where TLV431 is being used as a comparator, it is best to set the trip point to greater than the positive expected error (that is, +1.0% for the A version). For fast response, setting the trip point to > 10% of the internal V_{ref} should suffice.

For minimal voltage drop or difference from Vin to the ref pin, TI recommends using an input resistor < 10kΩ to provide I_{ref}.

8.2.1.2.3 Output Voltage and Logic Input Level

For the TLV431 to properly be used as a comparator, the logic output must be readable by the receiving logic device. This is accomplished by knowing the input high and low level threshold voltage levels, typically denoted by V_{IH} and V_{IL}.

As seen in Figure 8-3, TLV431's output low level voltage in open-loop/comparator mode is approximately 1V, which is sufficient for some 3.3V supplied logic. However, this does not work for 2.5V or 1.8V supplied logic. To accommodate this a resistive divider can be tied to the output to attenuate the output voltage to a voltage legible to the receiving low voltage logic device.

TLV431's output high voltage is approximately V_{sup} due to TLV431 being open-collector. If V_{sup} is much higher than the receiving logic's maximum input voltage tolerance, the output must be attenuated to accommodate the outgoing logic's reliability.

When using a resistive divider on the output, be sure to make the sum of the resistive divider (R1 and R2 in Figure 8-2) is much greater than R_{sup} to not interfere with TLV431's ability to pull close to V_{sup} when turning off.

8.2.1.2.3.1 Input Resistance

TLV431 requires an input resistance in this application to source the reference current (I_{ref}) needed from this device to be in the proper operating regions while turning on. The actual voltage seen at the ref pin will be $V_{ref} = V_{in} - I_{ref} \times R_{in}$. Because the I_{ref} can be as high as 0.5µA, TI recommends using a resistance small enough that will mitigate the error that I_{ref} creates from V_{in}.

8.2.1.3 Application Curves

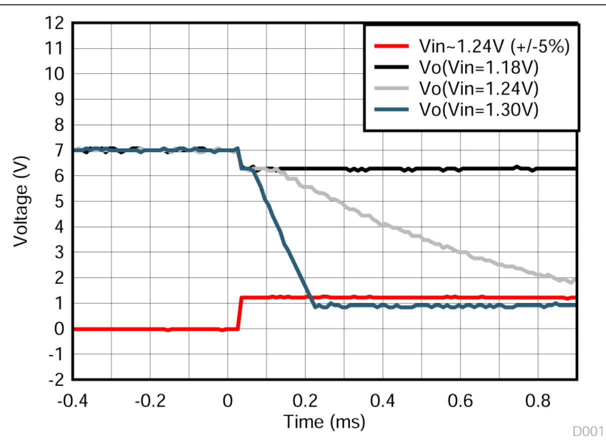


Figure 8-3. Output Response with Small Overdrive Voltages

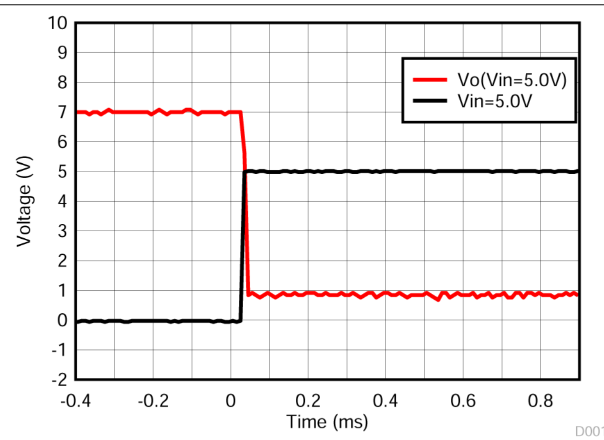


Figure 8-4. Output Response with Large Overdrive Voltage

8.2.2 Shunt Regulator/Reference

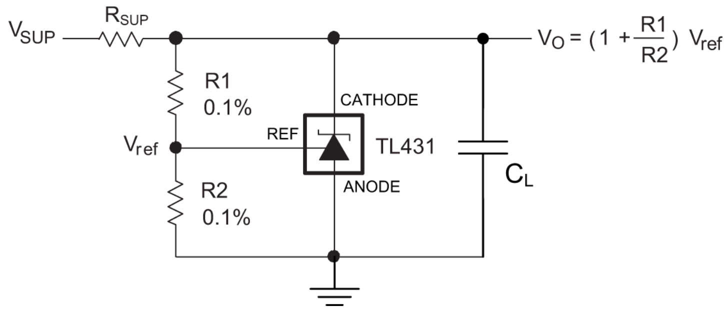


Figure 8-5. Shunt Regulator Schematic

8.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-2 as the input parameters.

Table 8-2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Reference Initial Accuracy	1.0%
Supply Voltage	6V
Cathode Current (Ik)	1mA
Output Voltage Level	1.24V - 6V
Load Capacitance	100pF
Feedback Resistor Values and Accuracy (R1 and R2)	10kΩ

8.2.2.2 Detailed Design Procedure

When using TLV431 as a Shunt Regulator, determine the following:

- Input voltage range
- Temperature range
- Total accuracy
- Cathode current
- Reference initial accuracy
- Output capacitance

8.2.2.2.1 Programming Output/Cathode Voltage

To program the cathode voltage to a regulated voltage a resistive bridge must be shunted between the cathode and anode pins with the mid point tied to the reference pin. This can be seen in Figure 8-5, with R1 and R2 being the resistive bridge. The cathode/output voltage in the shunt regulator configuration can be approximated by the equation shown in Figure 8-5. The cathode voltage can be more accurately determined by taking the cathode current in to account

$V_O = (1 + R1 / R2) \times V_{ref} - I_{ref} \times R1$ (1)

For Equation 1 to be valid, TLV431 must be fully biased so that it has enough open-loop gain to mitigate any gain error. This can be done by meeting the I_{min} spec denoted in *Recommended Operating Conditions* table.

8.2.2.2.2 Total Accuracy

When programming the output above unity gain (Vka = Vref), TLV431 is susceptible to other errors that may effect the overall accuracy beyond V_{ref}. These errors include:

- R1 and R2 accuracies
- $V_{I(dev)}$ – Change in reference voltage over temperature
- $\Delta V_{ref} / \Delta V_{KA}$ – Change in reference voltage to the change in cathode voltage
- $|z_{KA}|$ – Dynamic impedance, causing a change in cathode voltage with cathode current

Worst-case cathode voltage can be determined taking all of the variables in to account. Application note Setting the Shunt Voltage on an Adjustable Shunt Regulator (SLVA445) assists designers in setting the shunt voltage to achieve optimum accuracy for this device.

8.2.2.2.3 Stability

Though TLV431 is stable with no capacitive load, the device that receives the shunt regulator's output voltage could present a capacitive load that is within the TLV431 region of stability, shown in Figure 5-18. Also, designers may use capacitive loads to improve the transient response or for power supply decoupling.

8.2.2.3 Application Curve

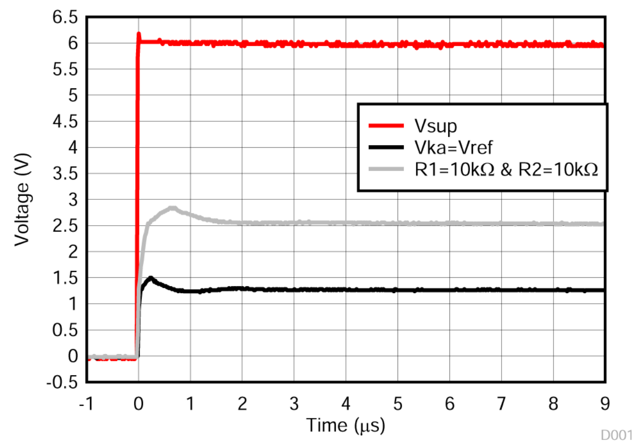


Figure 8-6. TLV431 Start-Up Response

8.3 Power Supply Recommendations

When using TLV431 as a Linear Regulator to supply a load, designers will typically use a bypass capacitor on the output/cathode pin. When doing this, be sure that the capacitance is within the stability criteria shown in Figure 5-18.

To not exceed the maximum cathode current, be sure that the supply voltage is current limited. Also, be sure to limit the current being driven into the Ref pin, as not to exceed the absolute maximum rating.

For applications shunting high currents, pay attention to the cathode and anode trace lengths, adjusting the width of the traces to have the proper current density.

8.4 Layout

8.4.1 Layout Guidelines

Place decoupling capacitors as close to the device as possible. Use appropriate widths for traces when shunting high currents to avoid excessive voltage drops.

8.4.2 Layout Example

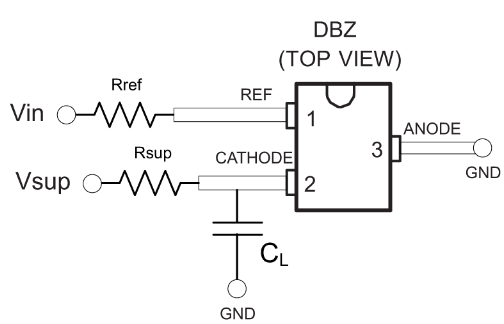


Figure 8-7. DBZ Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Compensation Design With TL431 for UCC28600 (SLUA671)
- Setting the Shunt Voltage on an Adjustable Shunt Regulator (SLVA445)

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision X (May 2018) to Revision Y (March 2024) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document................. 1
- Moved *Simplified Schematic* from *Description* to *Applications* 1
- Updated pinout diagrams... 3
- Updated *Typical Applications Design Requiements* 23

Changes from Revision W (March 2018) to Revision X (May 2018) **Page**

- Changed Figure 5-18 8

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV431ACDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	(YAC6, YACC, YACI, YACN) (YACG, YACL, YACS)	Samples
TLV431ACDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	(YAC6, YACC, YACI) (YACG, YACL, YACS)	Samples
TLV431ACDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(YAC6, YAC8, YACB, YACS) (YAC3, YACS, YACU)	Samples
TLV431ACDBZRG4	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	YAC6 YACS	Samples
TLV431ACLP	ACTIVE	TO-92	LP	3	1000	RoHS & Green	SN	N / A for Pkg Type	0 to 70	V431AC	Samples
TLV431ACLPR	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 70	V431AC	Samples
TLV431AIDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(YAI6, YAIC, YAII, YAIN) (YAIG, YAIL, YAIS)	Samples
TLV431AIDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(YAI6, YAIC, YAII) (YAIG, YAIL, YAIS)	Samples
TLV431AIDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(YAI6, YAI8, YAIB, YAIS) (YAI3, YAIS, YAIU)	Samples
TLV431AIDBZRG4	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	YAI6 YAIS	Samples
TLV431AIDE4	NRND	SOIC	D	8	75	TBD	Call TI	Call TI	-40 to 85		
TLV431AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY431A	Samples
TLV431AIDRE4	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85		

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV431AILPM	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	-40 to 85	V431AI	Samples
TLV431AILPR	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	-40 to 85	V431AI	Samples
TLV431AQPK	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	VA	Samples
TLV431BCDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	(Y3GG, Y3GJ, Y3GU)	Samples
TLV431BCDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	(Y3GG, Y3GJ, Y3GU)	Samples
TLV431BCDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(Y3G3, Y3GS, Y3GU)	Samples
TLV431BCDBZT	ACTIVE	SOT-23	DBZ	3	250	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(Y3GS, Y3GU)	Samples
TLV431BCDBZTG4	ACTIVE	SOT-23	DBZ	3	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	Y3GS	Samples
TLV431BCDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	YEU	Samples
TLV431BCDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	YEU	Samples
TLV431BCLPR	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 70	TV431B	Samples
TLV431BCPK	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 70	VE	Samples
TLV431BIDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(Y3FJ, Y3FU)	Samples
TLV431BIDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(Y3FJ, Y3FU)	Samples
TLV431BIDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(Y3F3, Y3FS, Y3FU)	Samples
TLV431BIDBZRG4	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(Y3F3, Y3FS)	Samples
TLV431BIDBZT	ACTIVE	SOT-23	DBZ	3	250	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(Y3FS, Y3FU)	Samples
TLV431BIDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YFU	Samples
TLV431BIDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YFU	Samples
TLV431BILPR	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	-40 to 85	TY431B	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV431BIPK	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 85	VF	Samples
TLV431BQDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(Y3HJ, Y3HU)	Samples
TLV431BQDBVRE4	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
TLV431BQDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(Y3HJ, Y3HU)	Samples
TLV431BQDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(Y3H3, Y3HS, Y3HU)	Samples
TLV431BQDBZRG4	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	Y3HS	Samples
TLV431BQDBZT	ACTIVE	SOT-23	DBZ	3	250	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(Y3HS, Y3HU)	Samples
TLV431BQDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	YGU	Samples
TLV431BQDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	YGU	Samples
TLV431BQLPR	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	TQ431B	Samples
TLV431BQPK	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	V6	Samples
TLV431CDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	(Y3C6, Y3CI) (Y3CG, Y3CS)	Samples
TLV431CDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	(Y3C6, Y3CI) (Y3CG, Y3CS)	Samples
TLV431CDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(Y3C6, Y3C8, Y3CB, Y3CS) (Y3C3, Y3CS, Y3CU)	Samples
TLV431CLPR	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	0 to 70	V431C	Samples
TLV431IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(Y3I6, Y3II) (Y3IG, Y3IS)	Samples
TLV431IDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(Y3I6, Y3II) (Y3IG, Y3IS)	Samples
TLV431IDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(Y3I6, Y3IB, Y3IS) (Y3IU, Y3IU)	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV431IDBZRG4	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	Y3I6 Y3IS	Samples
TLV431ILPR	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	-40 to 85	V431I	Samples
TLV431QPK	ACTIVE	SOT-89	PK	3	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	VB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV431A, TLV431B :

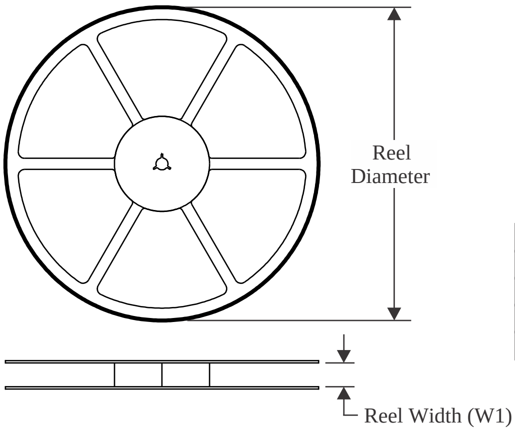
- Automotive : TLV431A-Q1, TLV431B-Q1

NOTE: Qualified Version Definitions:

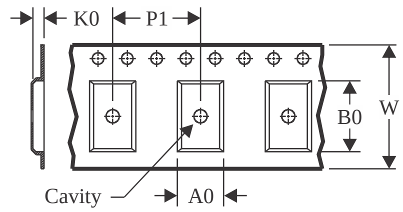
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

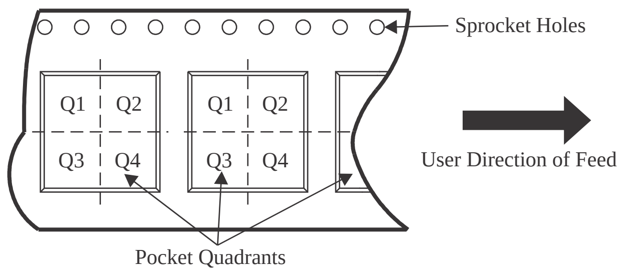


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



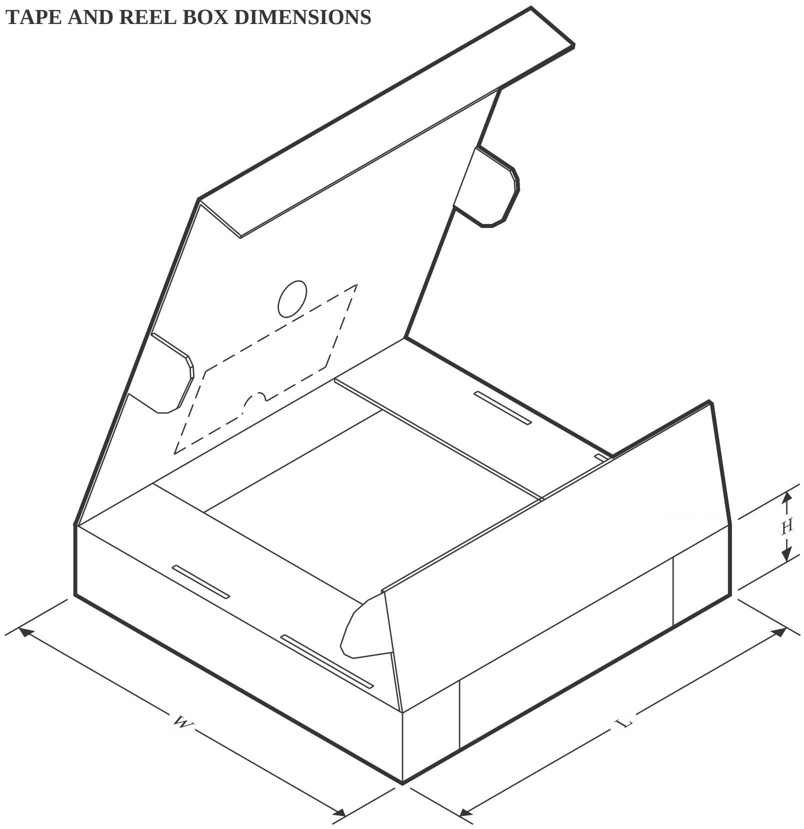
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV431ACDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV431ACDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV431ACDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV431ACDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV431ACDBZR	SOT-23	DBZ	3	3000	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
TLV431ACDBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV431ACDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TLV431ACDBZRG4	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TLV431AIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV431AIDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV431AIDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV431AIDBZR	SOT-23	DBZ	3	3000	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
TLV431AIDBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV431AIDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV431AIDBZRG4	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TLV431AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV431AQPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
TLV431BCDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV431BCDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV431BCDBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV431BCDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV431BCDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TLV431BCDBZR	SOT-23	DBZ	3	3000	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
TLV431BCDBZT	SOT-23	DBZ	3	250	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV431BCDBZTG4	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TLV431BCDCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV431BCDCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV431BCPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
TLV431BIDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV431BIDBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV431BIDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV431BIDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV431BIDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV431BIDBZRG4	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TLV431BIDBZT	SOT-23	DBZ	3	250	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV431BIDCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV431BIDCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV431BIPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
TLV431BQDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV431BQDBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV431BQDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV431BQDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV431BQDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV431BQDBZRG4	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TLV431BQDBZT	SOT-23	DBZ	3	250	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV431BQDCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV431BQDCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TLV431BQPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3
TLV431CDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV431CDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV431CDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV431CDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV431CDBZR	SOT-23	DBZ	3	3000	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
TLV431CDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TLV431CDBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV431CDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV431IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV431IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV431IDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TLV431IDBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV431IDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
TLV431IDBZRG4	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
TLV431QPK	SOT-89	PK	3	1000	180.0	12.4	4.91	4.52	1.9	8.0	12.0	Q3

TAPE AND REEL BOX DIMENSIONS



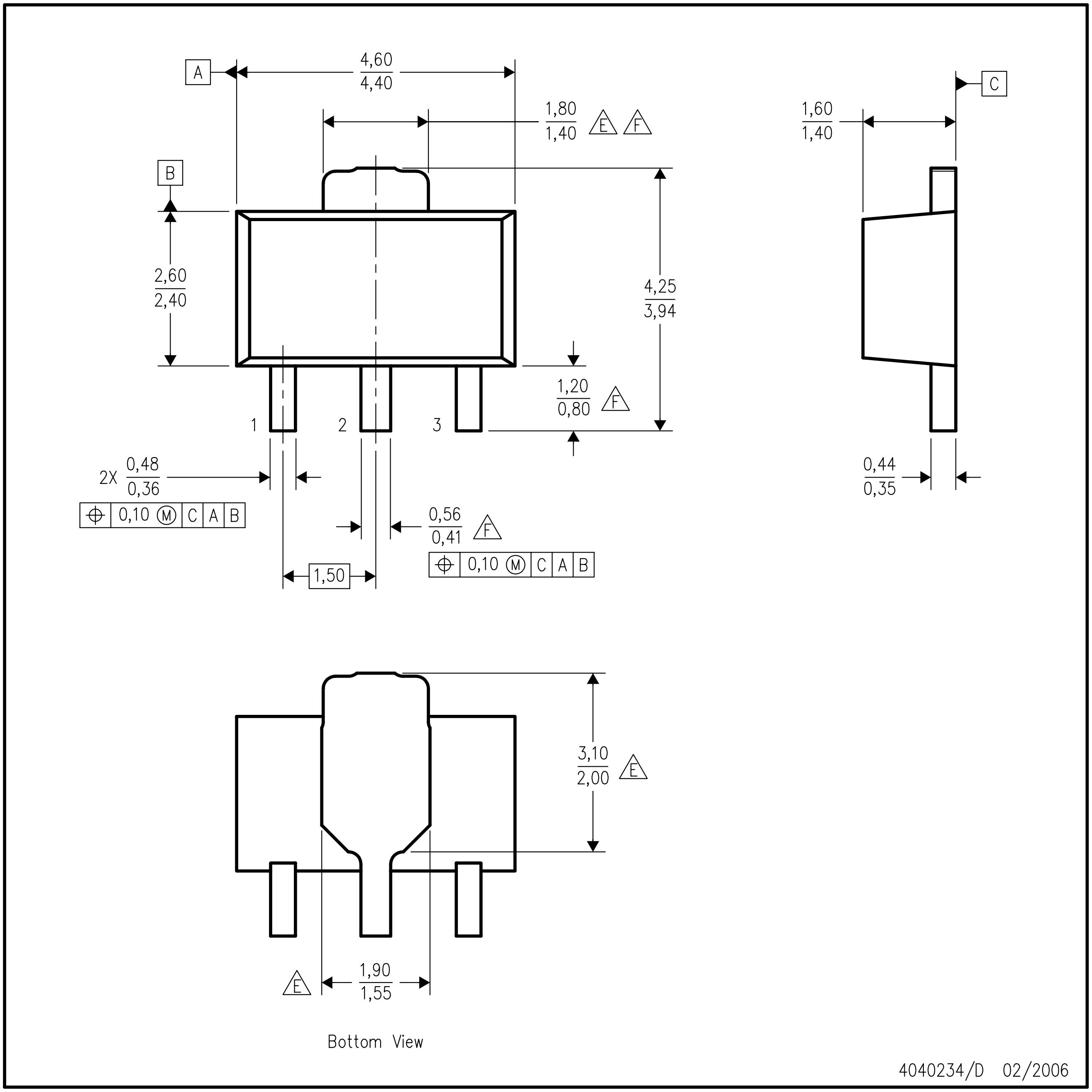
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV431ACDBVR	SOT-23	DBV	5	3000	183.0	183.0	20.0
TLV431ACDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV431ACDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV431ACDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV431ACDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV431ACDBZR	SOT-23	DBZ	3	3000	200.0	183.0	25.0
TLV431ACDBZR	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TLV431ACDBZRG4	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TLV431AIDBVR	SOT-23	DBV	5	3000	183.0	183.0	20.0
TLV431AIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV431AIDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV431AIDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV431AIDBZR	SOT-23	DBZ	3	3000	200.0	183.0	25.0
TLV431AIDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV431AIDBZRG4	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TLV431AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV431AQPK	SOT-89	PK	3	1000	340.0	340.0	38.0
TLV431BCDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV431BCDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV431BCDBZR	SOT-23	DBZ	3	3000	200.0	183.0	25.0
TLV431BCDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV431BCDBZR	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TLV431BCDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV431BCDBZT	SOT-23	DBZ	3	250	180.0	180.0	18.0
TLV431BCDBZTG4	SOT-23	DBZ	3	250	183.0	183.0	20.0
TLV431BCDCKR	SC70	DCK	6	3000	203.0	203.0	35.0
TLV431BCDCKT	SC70	DCK	6	250	203.0	203.0	35.0
TLV431BCPK	SOT-89	PK	3	1000	340.0	340.0	38.0
TLV431BIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV431BIDBVR	SOT-23	DBV	5	3000	200.0	183.0	25.0
TLV431BIDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV431BIDBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
TLV431BIDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV431BIDBZRG4	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TLV431BIDBZT	SOT-23	DBZ	3	250	180.0	180.0	18.0
TLV431BIDCKR	SC70	DCK	6	3000	203.0	203.0	35.0
TLV431BIDCKT	SC70	DCK	6	250	203.0	203.0	35.0
TLV431BIPK	SOT-89	PK	3	1000	340.0	340.0	38.0
TLV431BQDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV431BQDBVR	SOT-23	DBV	5	3000	200.0	183.0	25.0
TLV431BQDBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
TLV431BQDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV431BQDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV431BQDBZRG4	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TLV431BQDBZT	SOT-23	DBZ	3	250	180.0	180.0	18.0
TLV431BQDCKR	SC70	DCK	6	3000	200.0	183.0	25.0
TLV431BQDCKT	SC70	DCK	6	250	200.0	183.0	25.0
TLV431BQPK	SOT-89	PK	3	1000	340.0	340.0	38.0
TLV431CDBVR	SOT-23	DBV	5	3000	183.0	183.0	20.0
TLV431CDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV431CDBVT	SOT-23	DBV	5	250	183.0	183.0	20.0
TLV431CDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV431CDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV431CDBZR	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TLV431CDBZR	SOT-23	DBZ	3	3000	200.0	183.0	25.0
TLV431CDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
TLV431IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV431IDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV431IDBZR	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TLV431IDBZR	SOT-23	DBZ	3	3000	200.0	183.0	25.0
TLV431IDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0

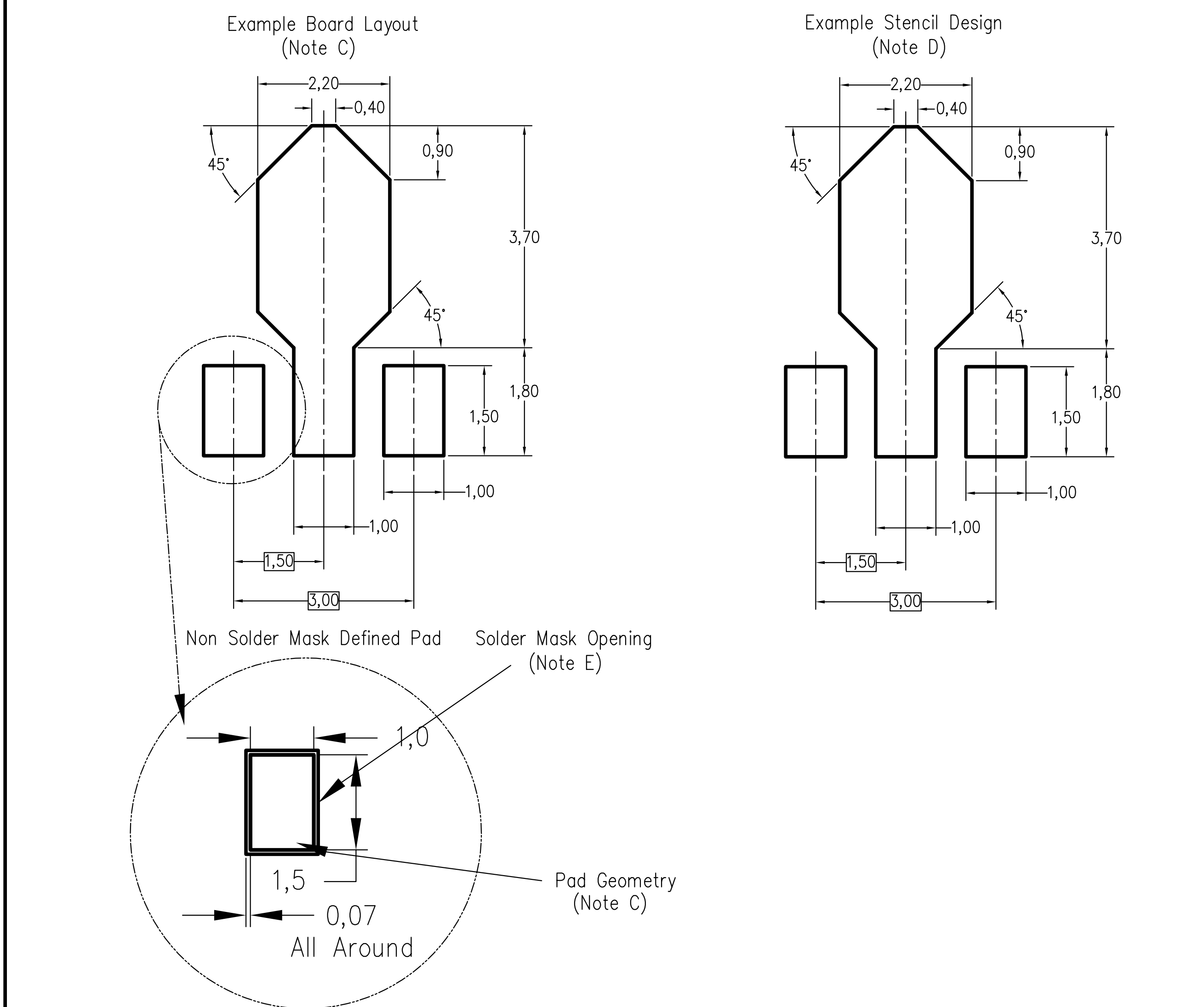
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV431IDBZRG4	SOT-23	DBZ	3	3000	183.0	183.0	20.0
TLV431QPK	SOT-89	PK	3	1000	340.0	340.0	38.0

PK (R–PSSO–F3) PLASTIC SINGLE–IN–LINE PACKAGE



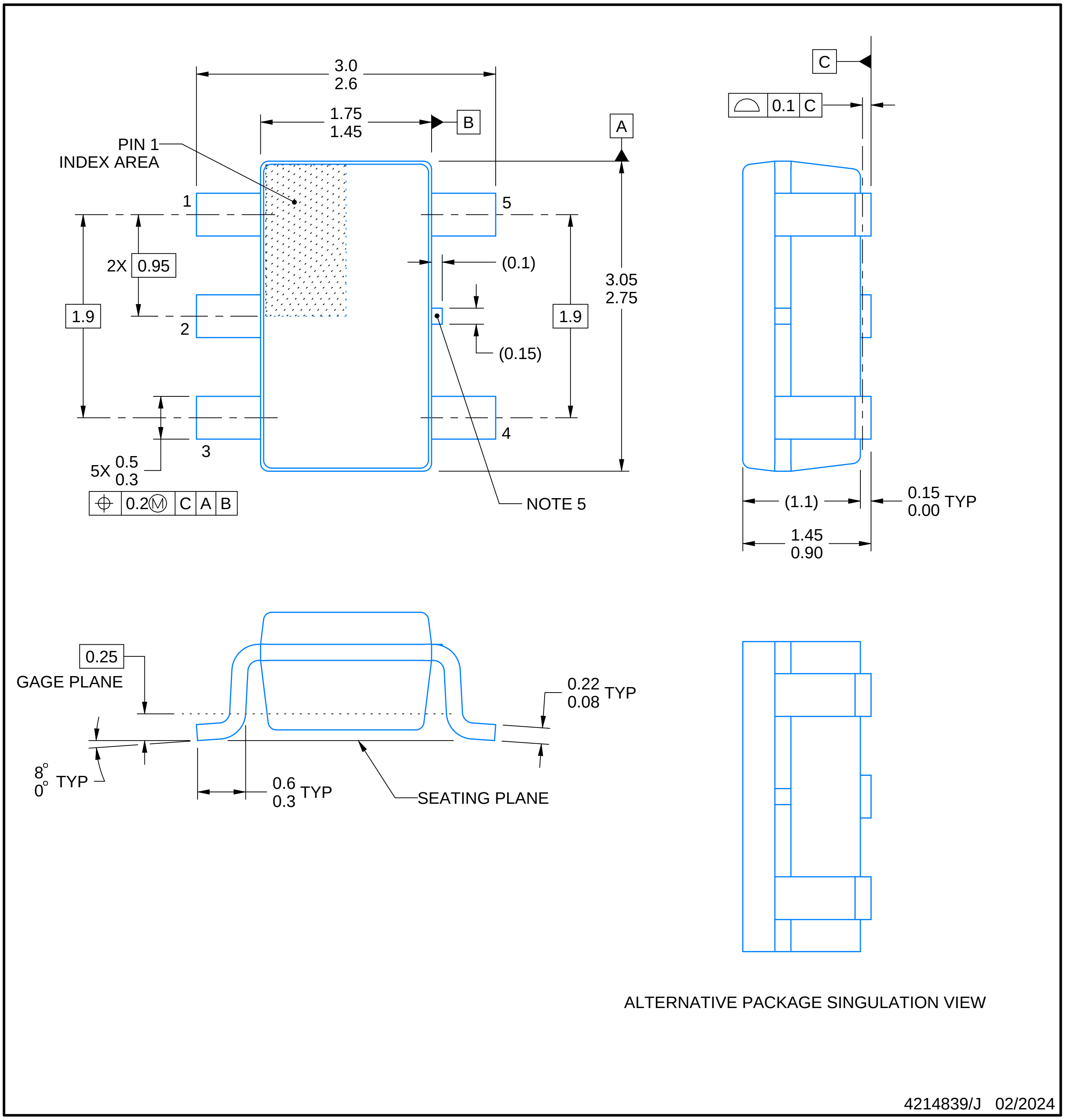
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the tab.
D. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion not to exceed 0.15 per side.
E. Thermal pad contour optional within these dimensions.
F. Falls within JEDEC TO–243 variation AA, except minimum lead length, pin 2 minimum lead width, minimum tab width.

PK (R–PDSO–G3)



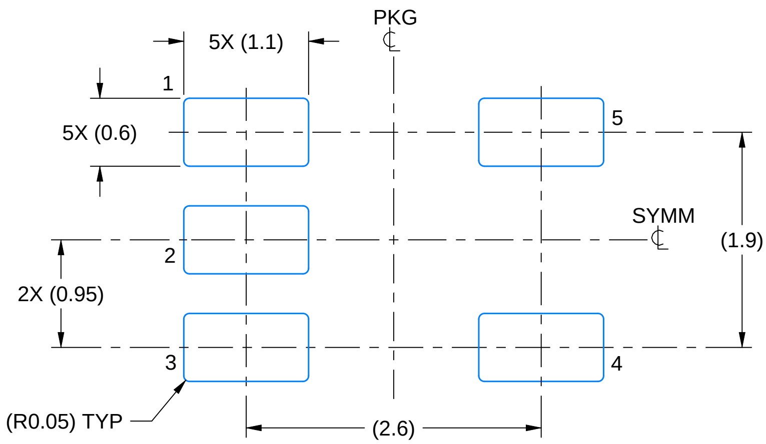
4208221/A 09/06

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

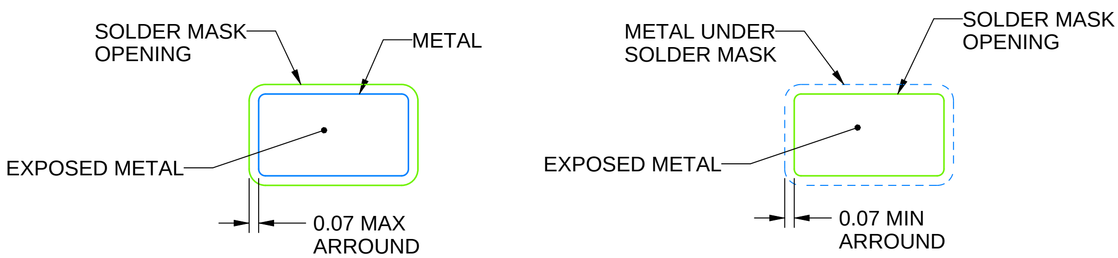


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK DEFINED (PREFERRED)

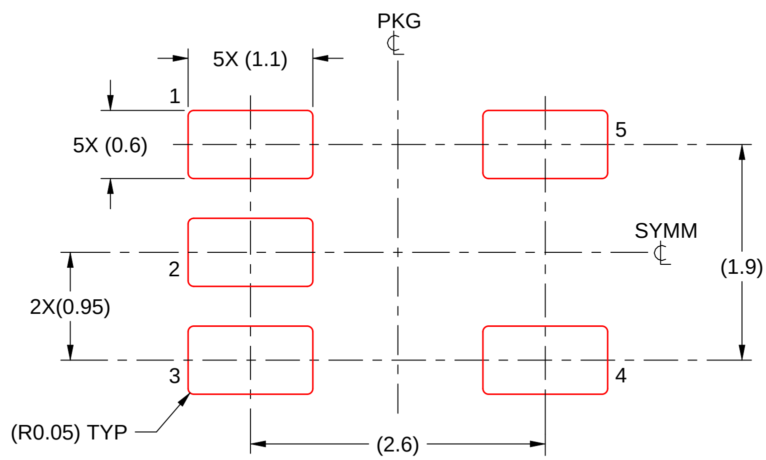
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

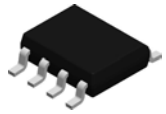


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

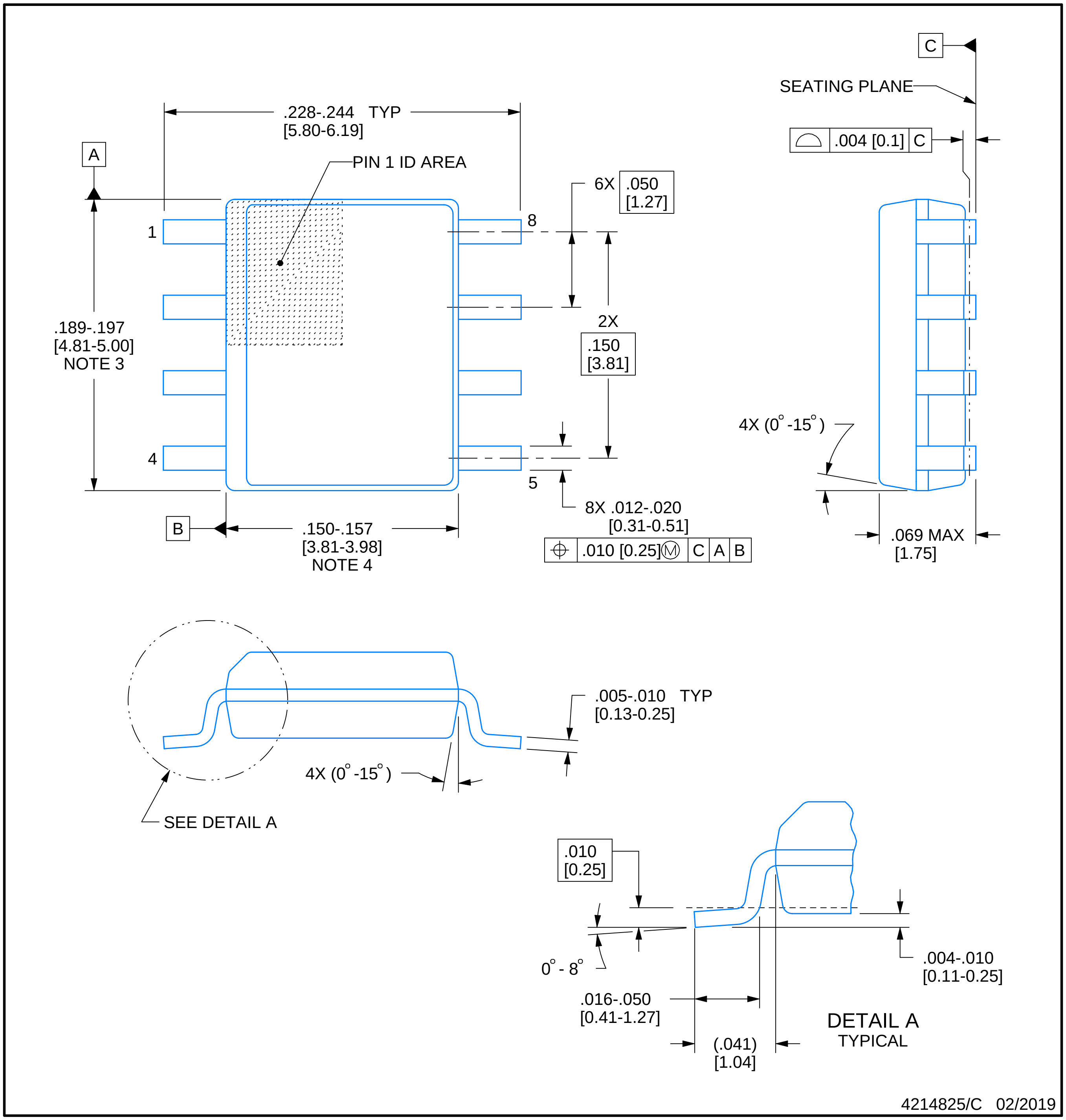


PACKAGE OUTLINE

D0008A

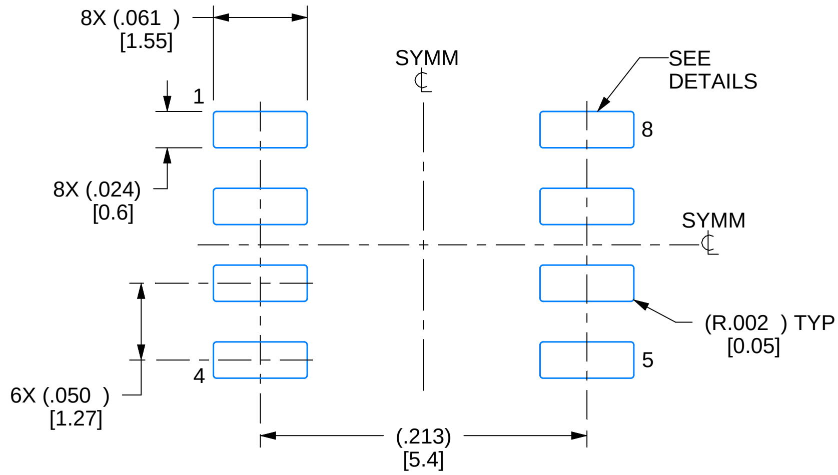
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

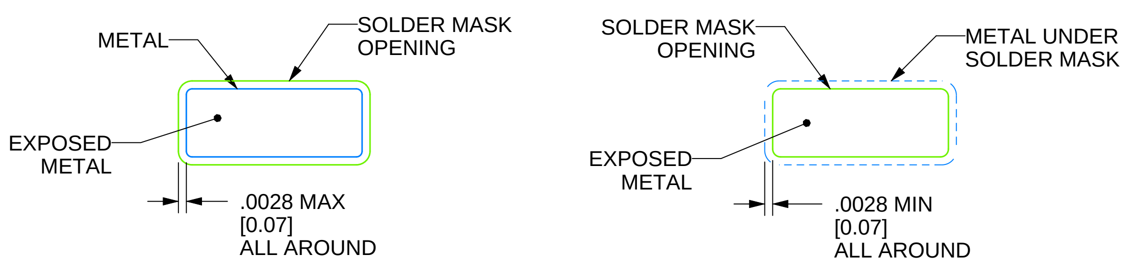


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

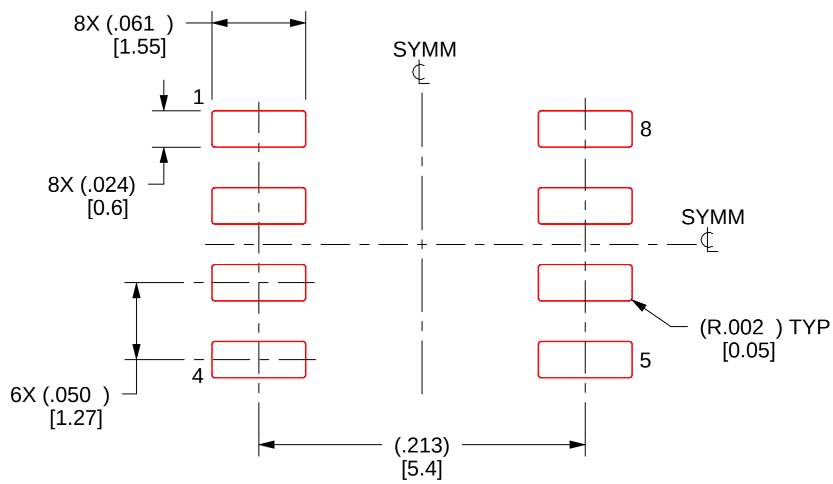
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

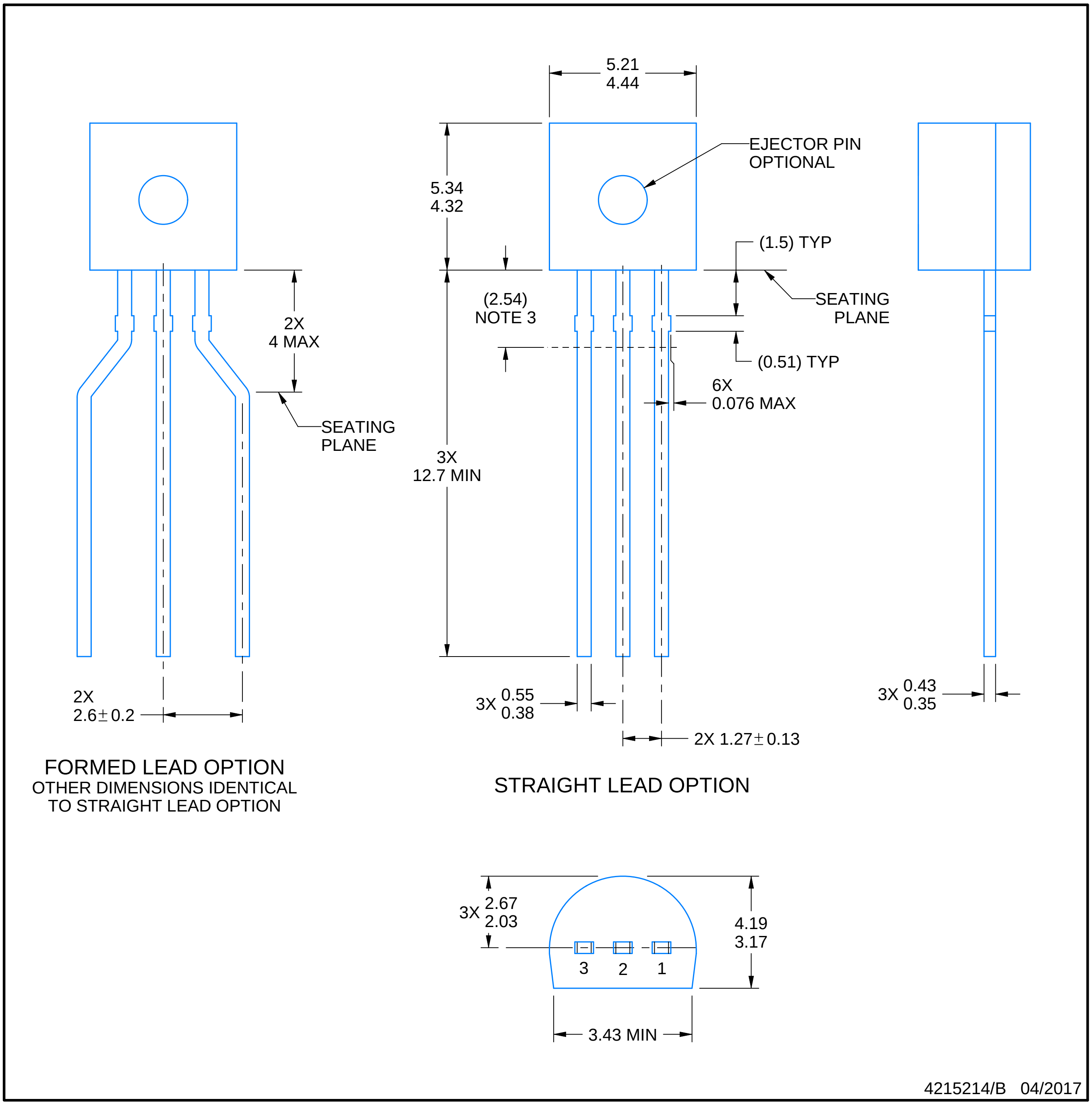
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

LP 3

TO-92 - 5.34 mm max height

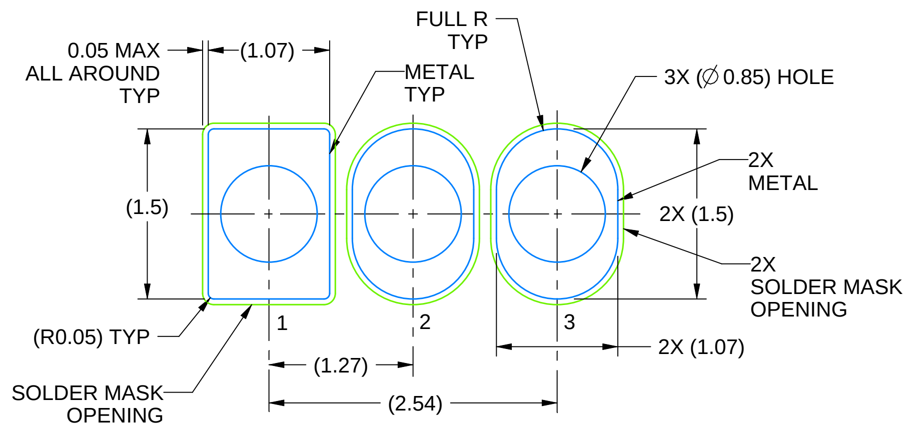
TRANSISTOR OUTLINE

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

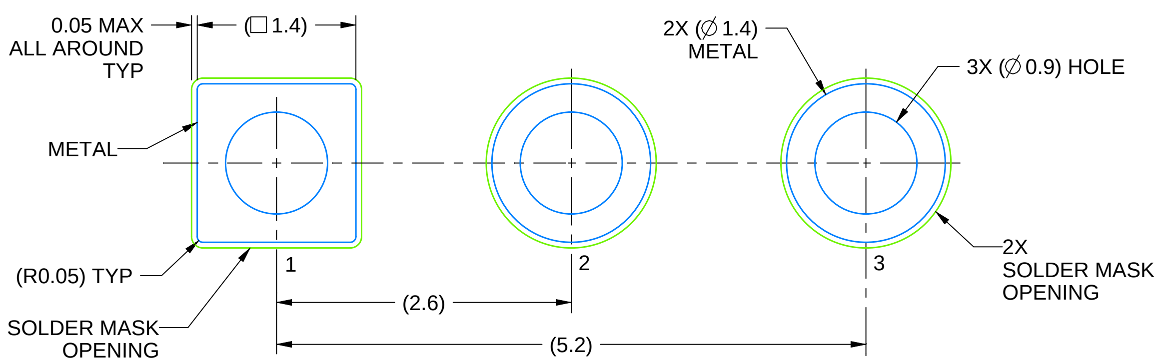


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
   a. Straight lead option available in bulk pack only.
   b. Formed lead option available in tape and reel or ammo pack.
   c. Specific products can be offered in limited combinations of shipping medium and lead options.
   d. Consult product folder for more information on available options.

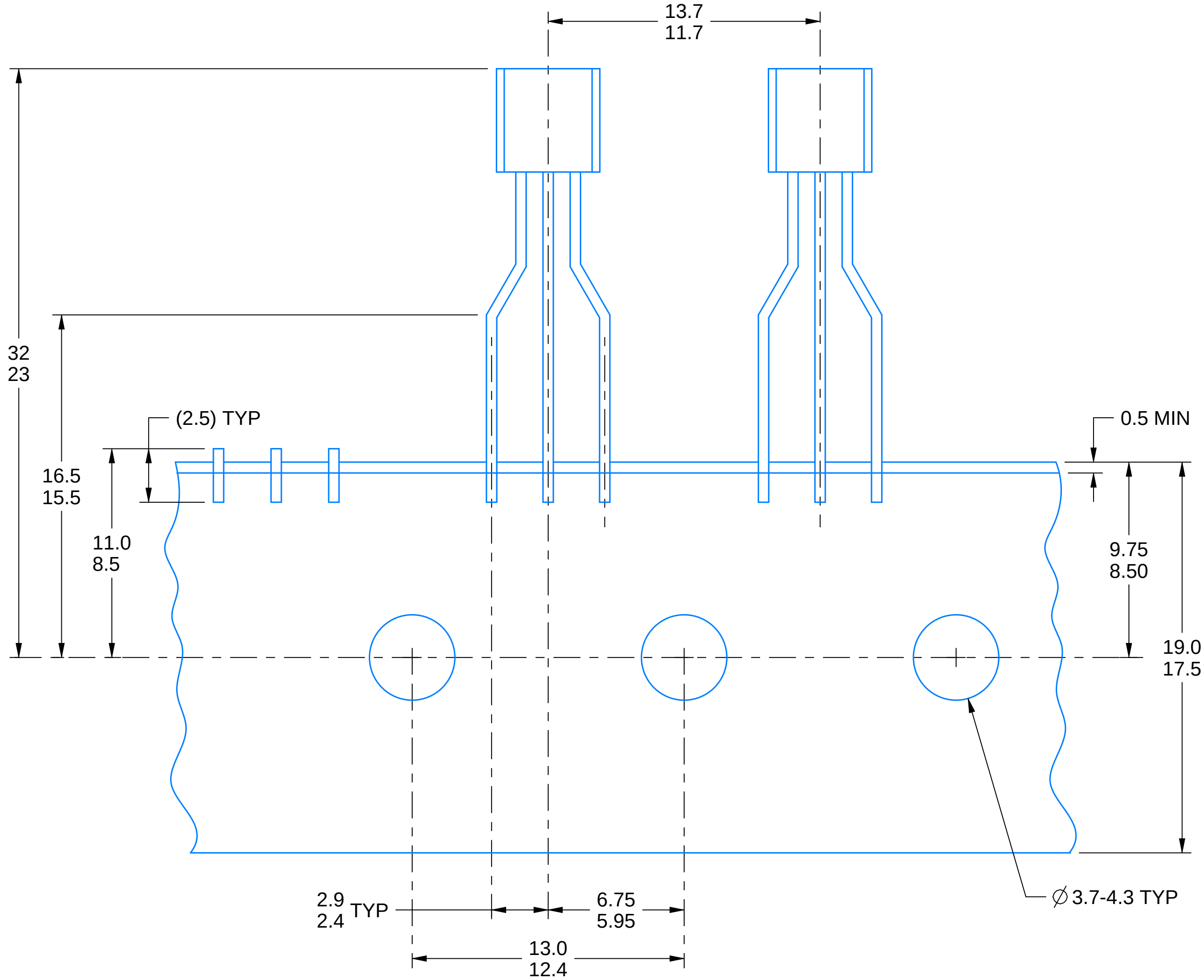


LAND PATTERN EXAMPLE
STRAIGHT LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



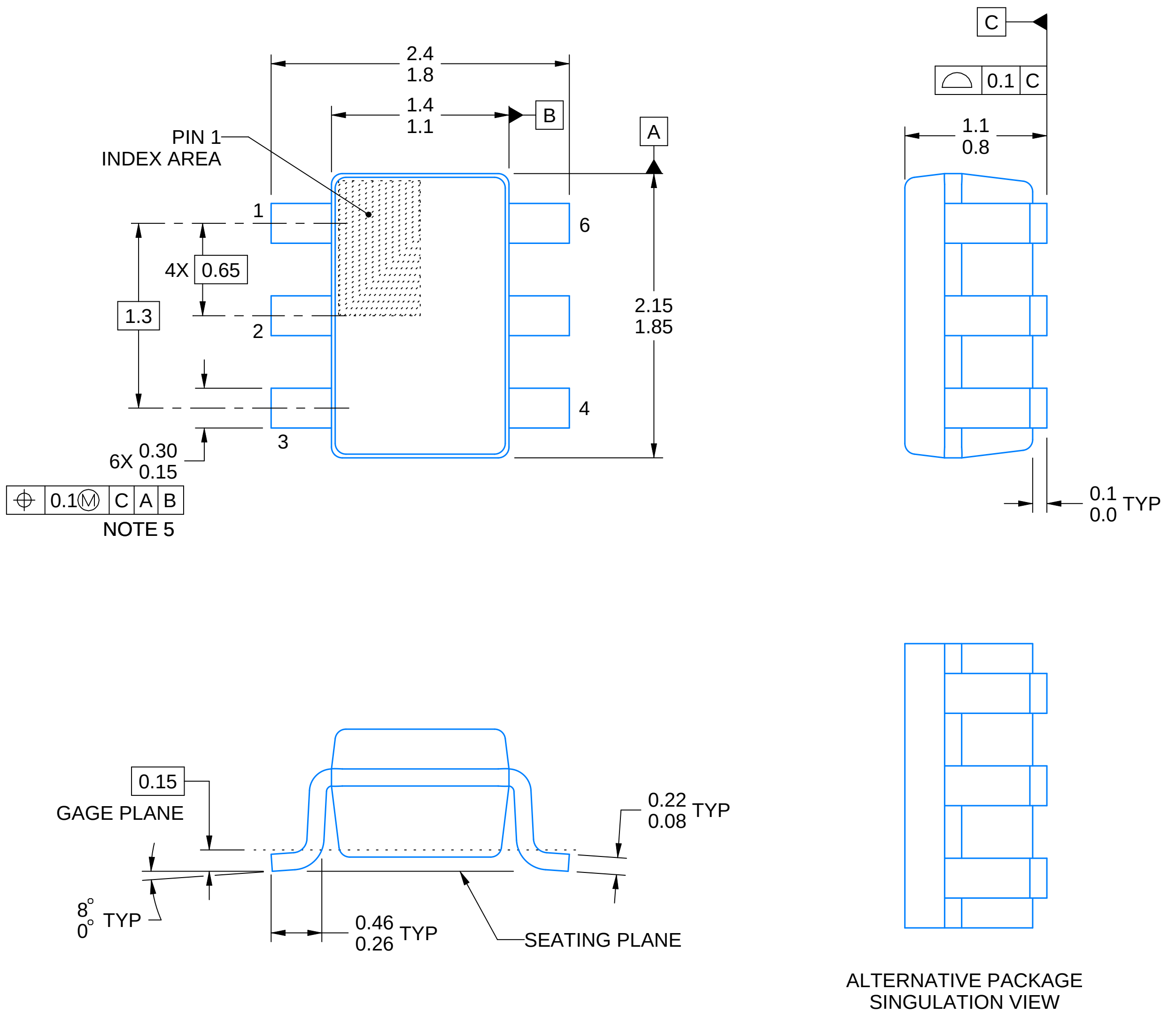
LAND PATTERN EXAMPLE
FORMED LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X

4215214/B 04/2017



FOR FORMED LEAD OPTION PACKAGE

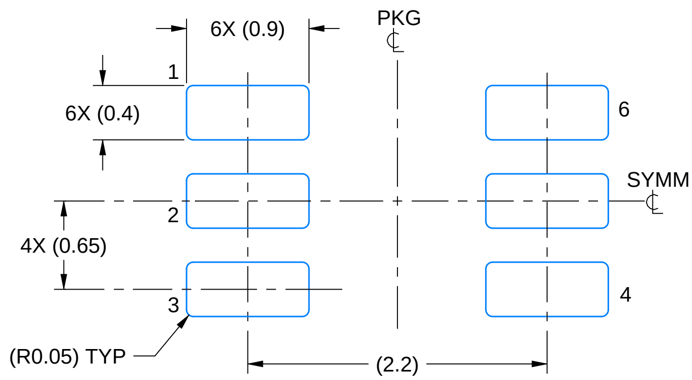
4215214/B 04/2017



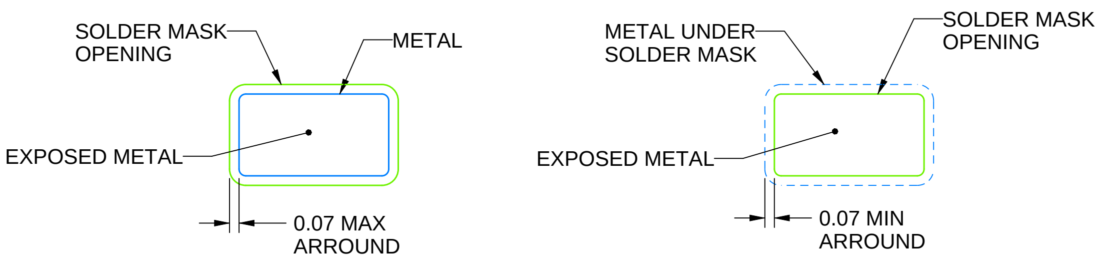
4214835/B 04/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



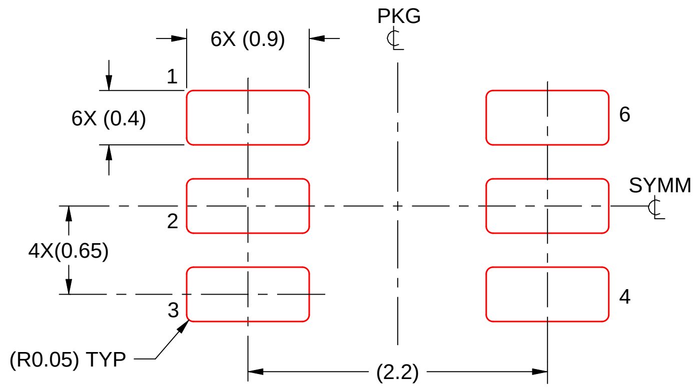
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/B 04/2024

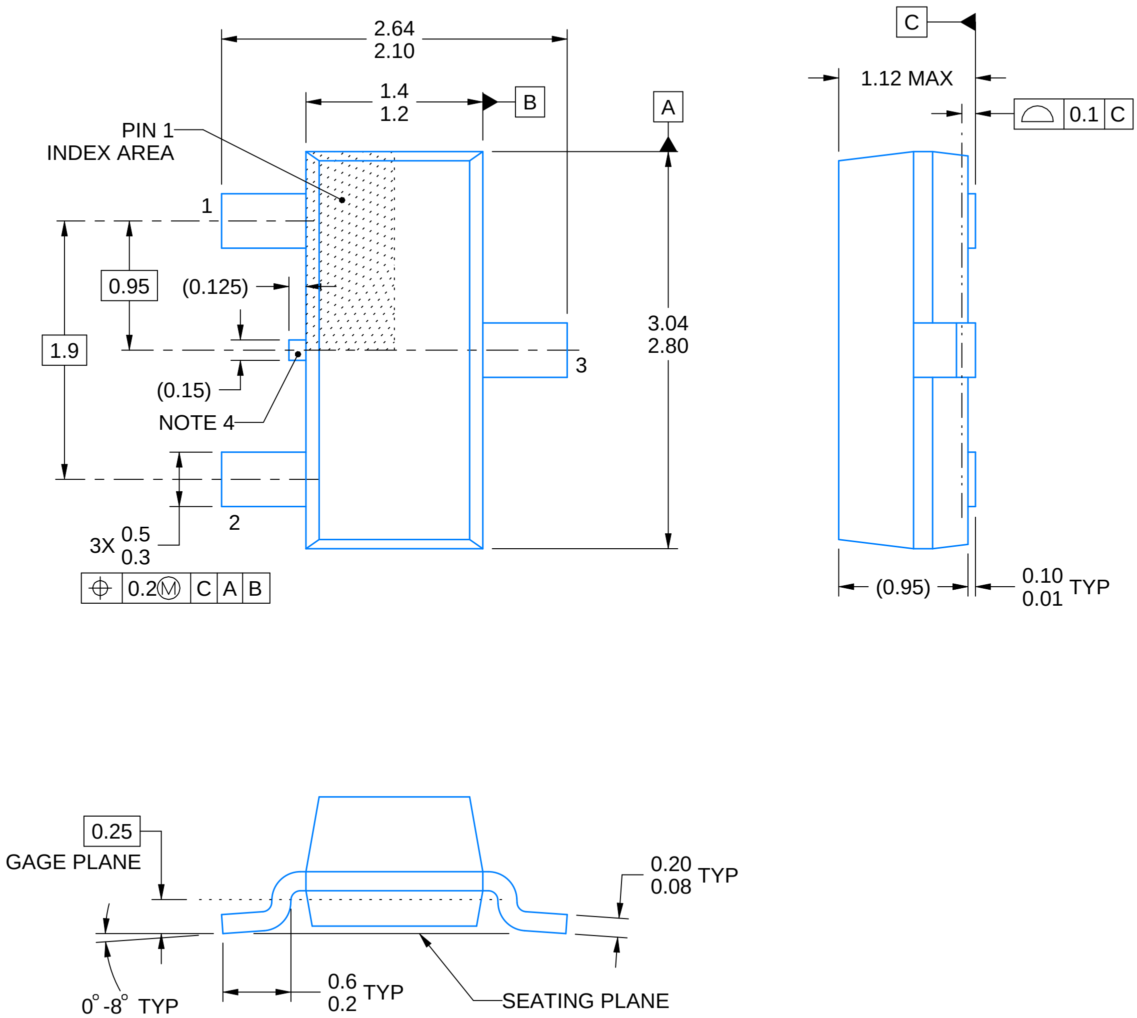
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

SOT-23 - 1.12 mm max height

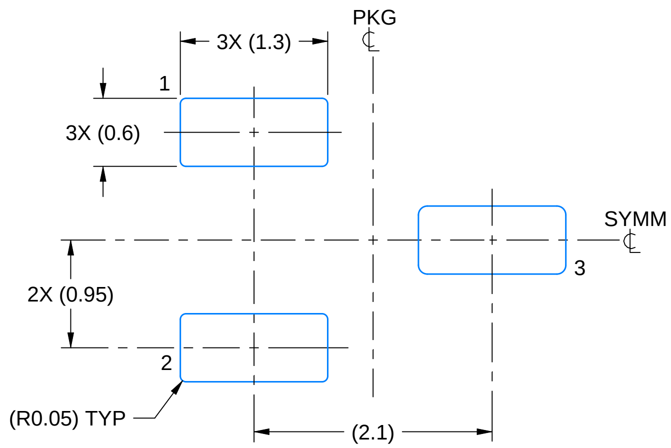
SMALL OUTLINE TRANSISTOR



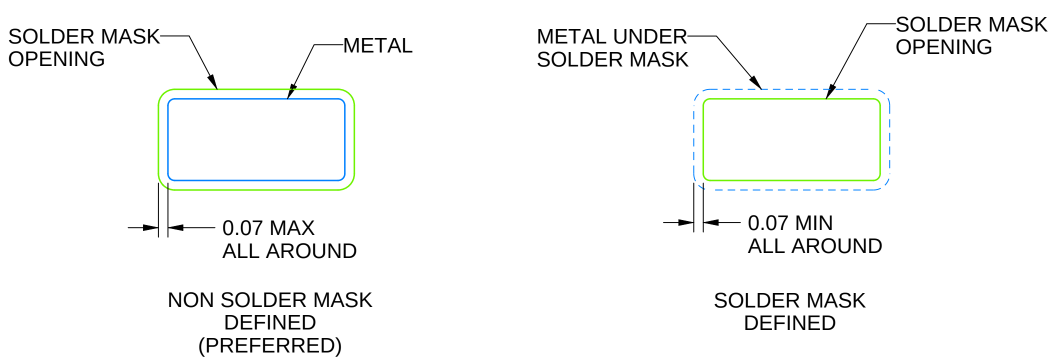
4214838/D 03/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE:15X

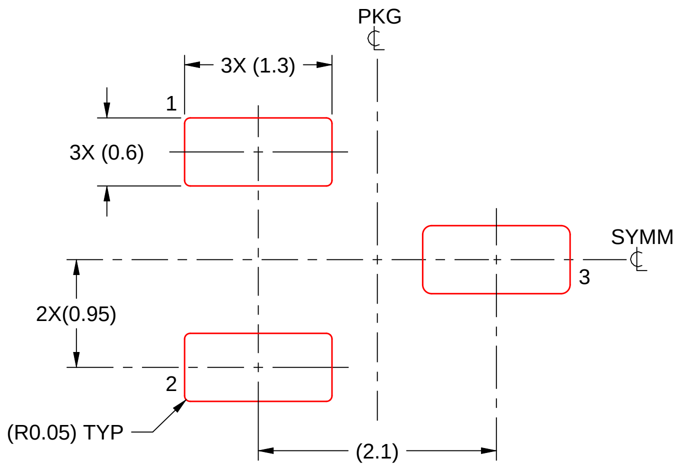


SOLDER MASK DETAILS

4214838/D 03/2023

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/D 03/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.