SNx4HC05 Hex Inverters With Open-Drain Outputs

1 Features

- Wide Operating Voltage Range of 2 V to 6 V
- Outputs can Drive up to 10 LSTTL Loads
- Low-Power Consumption, 20-μA Maximum ICC
- Typical t_{pd} = 8 ns
- ±4-mA Output Drive at 5 V
- Low Input Current of 1-μA Maximum

2 Applications

- Mice
- Printers
- AC Inverter Drives
- UPS
- AC Servo Drives
- Other Motor Drives

3 Description

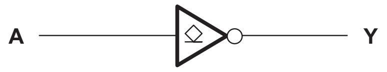
The SNx4HC05 devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$ in positive logic. The open-drain outputs require pullup resistors to perform correctly. They may be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74HC05	PDIP (14)	19.30 mm × 6.40 mm
	SOIC (14)	8.65 mm × 3.91 mm
	SOP (14)	10.30 mm × 5.30 mm
	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



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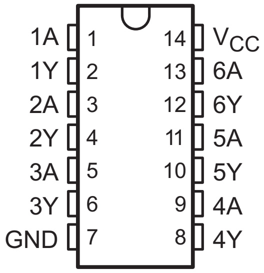
4 Revision History

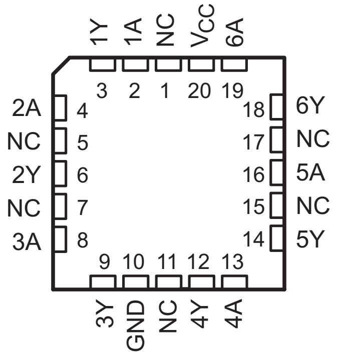
Changes from Revision D (August 2003) to Revision E	**Page**
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

SN74HC05: D, N, NS, or PW Package, 14-Pin SOIC, PDIP, SOP, or TSSOP
SN54HC05: J or W Package, 19-Pin CDIP or CFP
(Top View)



SN54HC05: FK Package
20-Pin LCCC
(Top View)



NC – No internal connection

Pin Functions

PIN			I/O	DESCRIPTION
NAME	**NO.**	**LCCC NO.**		
1A	1	2	I	Input 1
1Y	2	3	O	Output 1
2A	3	4	I	Input 2
2Y	4	6	O	Output 2
3A	5	8	I	Input 3
3Y	6	9	O	Output 3
GND	7	10	–	Ground pin
4A	9	13	I	Input 4
4Y	8	12	O	Output 4
5A	11	16	I	Input 5
5Y	10	14	O	Output 5
6A	13	19	I	Input 6
6Y	12	18	O	Output 6
NC	–	1, 5, 7, 11, 15, 17	–	No connect
V_{CC}	14	20	–	Power pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.5	7	V
I_{IK}	Input clamp current, $V_I < 0$ or $V_I > V_{CC}$ (2)	–20	20	mA
I_{OK}	Output clamp current, $V_O < 0$ or $V_O > V_{CC}$ (2)	–20	20	mA
I_O	Continuous output current, $V_O = 0$ to V_{CC}	–25	25	mA
	Continuous current through V_{CC} or GND	–50	50	mA
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See (1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5			V
		$V_{CC} = 4.5$ V	3.15			
		$V_{CC} = 6$ V	4.2			
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V			0.5	V
		$V_{CC} = 4.5$ V			1.35	
		$V_{CC} = 6$ V			1.8	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall time	$V_{CC} = 2$ V			1000	ns
		$V_{CC} = 4.5$ V			500	
		$V_{CC} = 6$ V			400	
T_A	Operating free-air temperature	SN54HC05	–55		125	°C
		SN74HC05	–40		125	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

THERMAL METRIC[1]		SN74HC05				UNIT
		D (SOIC)	N (PDIP)	NS (SOP)	PW (TSSOP)	
		14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	89.1	85.9	86.4	117.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.6	43.8	42.4	46.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	43.3	44.6	45.1	58.7	
ψ_{JT}	Junction-to-top characterization parameter	16.3	12	11.8	4.8	
ψ_{JB}	Junction-to-board characterization parameter	43	44.2	44.7	58.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC05		SN74HC05 –40°C to 85°C		SN74HC05 –40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{OH}	$V_I = V_{IH}$ or V_{IL}, $V_O = V_{CC}$		6 V		0.01	0.5		10		5		5	µA
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 µA	2 V		0.002	0.1		0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33		0.33	
I_I	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0, I_O = 0		6 V			2		40		20		20	µA
C_i			2 to 6 V		3	10		10		10		10	pF

6.6 Switching Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC05		SN74HC05 –40°C to 85°C		SN74HC05 –40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	2 V		60	115		175		145		160	ns
			4.5 V		13	23		35		29		31	
			6 V		10	20		30		25		28	
t_{PHL}	A	Y	2 V		45	85		130		105		120	
			4.5 V		9	17		26		21		23	
			6 V		8	14		22		18		21	
t_f		Y	2 V		38	75		110		95		110	
			4.5 V		8	15		22		19		22	
			6 V		6	13		19		16		19	

6.7 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per inverter	No load	20	pF

6.8 Typical Characteristics

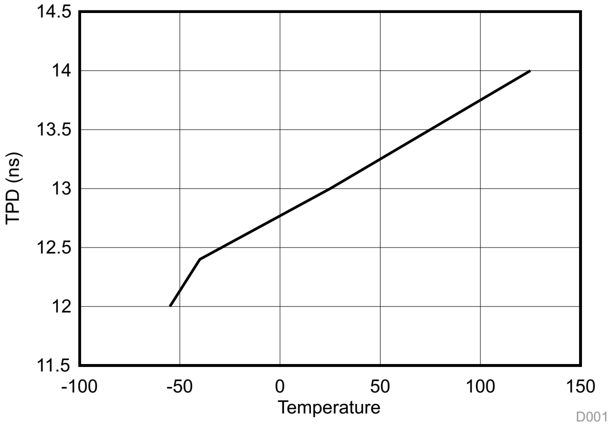


Figure 1. TPD vs. Temperature at 4.5 V, 25°C

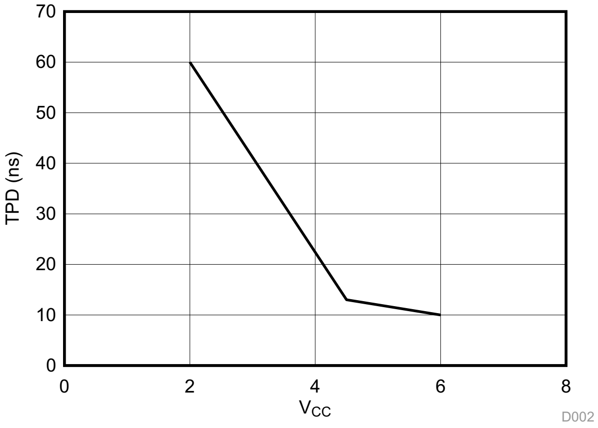
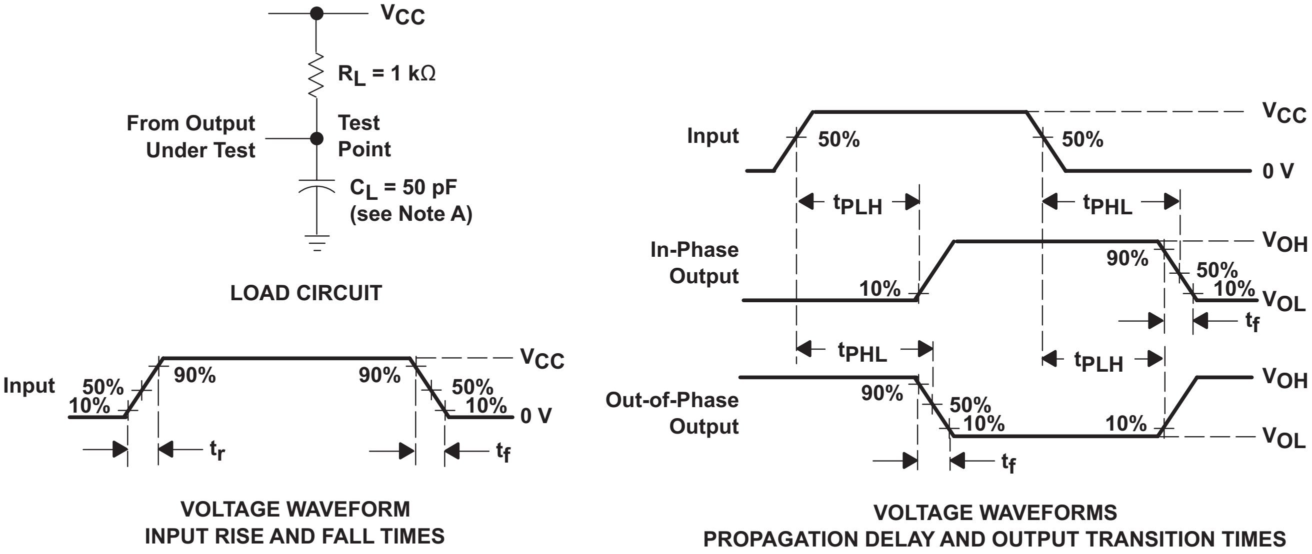


Figure 2. TPD vs. V_{CC} at 25°C

7 Parameter Measurement Information



A. C_L includes probe and test-fixture capacitance.

B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.

C. The outputs are measured one at a time with one input transition per measurement.

Figure 3. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SNx4HC05 devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$ in positive logic. The open-drain outputs require pullup resistors to perform correctly. They may be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

8.2 Functional Block Diagram

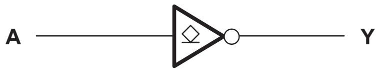


Figure 4. Logic Diagram (Positive Logic)

8.3 Feature Description

The device’s wide operating range allows it to be used in a variety of systems that use different logic levels. The strong current-sinking outputs allow the device to drive medium loads without significant increases in output voltage. In addition, the low power consumption makes this device a good choice for portable and battery power-sensitive applications.

8.4 Device Functional Modes

Table 1. Function Table (Each Inverter)

INPUT A	OUTPUT Y
H	L
L	H

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74HC05 device is a low drive open-drain CMOS device that can be used for a multitude of buffer type functions. The open-drain output can be pulled to any voltage between GND and V_{CC} making them Ideal for down translation.

9.2 Typical Application

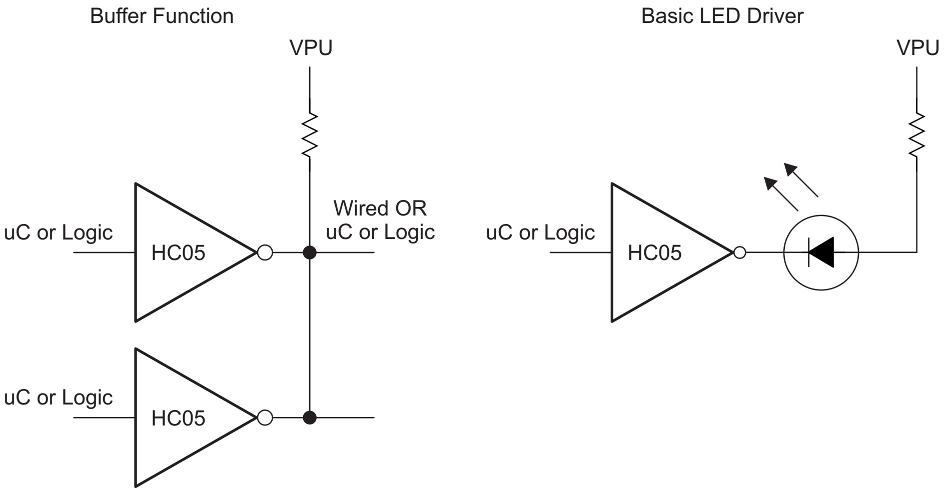


Figure 5. Simplified Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and is open-drain so it has low-output drive only. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. Parallel output drive can create fast edges into light loads so consider routing and load conditions to prevent ringing.

9.2.2 Detailed Design Procedure

- Recommended input conditions:
  - Rise time and fall time specs see (Δt/ΔV) in *Recommended Operating Conditions*.
  - Specified high and low levels. See (V_{IH} and V_{IL}) in *Recommended Operating Conditions*.
- Recommended output conditions:
  - Load currents should not exceed 25 mA per output and 50 mA total for the part.

Typical Application (continued)

9.2.3 Application Curve

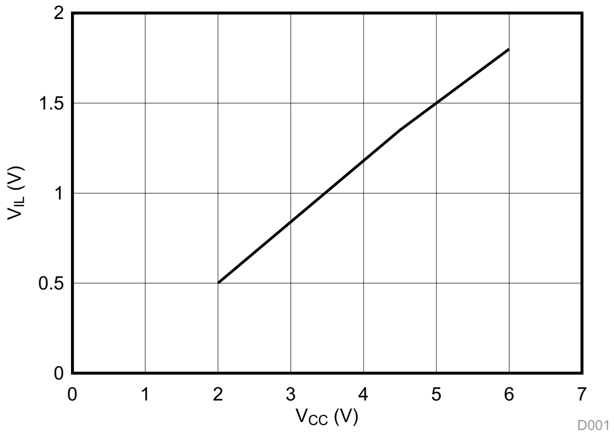


Figure 6. Max V_{IL} vs. V_{CC} Level

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-µF capacitor. If there are multiple VCC terminals, then TI recommends a 0.01-µF or 0.022-µF capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close as possible to the power terminal for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs should never float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever makes more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver.

11.2 Layout Example

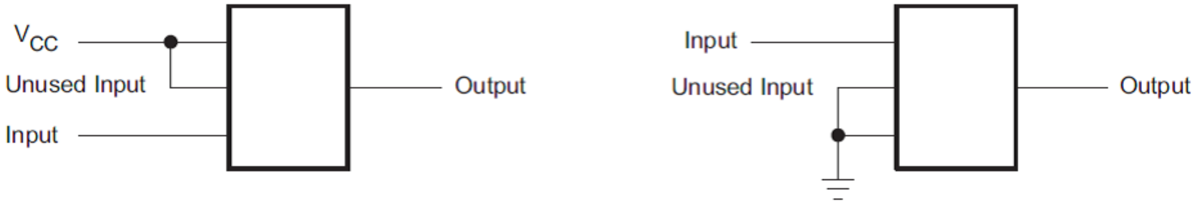


Figure 7. Layout Recommendation

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs, SCBA004

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54HC05	Click here	Click here	Click here	Click here	Click here
SN74HC05	Click here	Click here	Click here	Click here	Click here

12.3 Trademarks

All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-88718012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-88718012A SNJ54HC05FK	Samples
5962-8871801CA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8871801CA SNJ54HC05J	Samples
SN54HC05J	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	SN54HC05J	Samples
SN74HC05D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC05	Samples
SN74HC05DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC05	Samples
SN74HC05DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	HC05	Samples
SN74HC05DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC05	Samples
SN74HC05DT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC05	Samples
SN74HC05DTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC05	Samples
SN74HC05N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 125	SN74HC05N	Samples
SN74HC05NE4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 125	SN74HC05N	Samples
SN74HC05NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC05	Samples
SN74HC05NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC05	Samples
SN74HC05PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	HC05	Samples
SN74HC05PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC05	Samples
SN74HC05PWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC05	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54HC05FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-88718012A SNJ54HC05FK	Samples
SNJ54HC05J	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-8871801CA SNJ54HC05J	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54HC05, SN74HC05 :

- Catalog: SN74HC05

- Military: SN54HC05

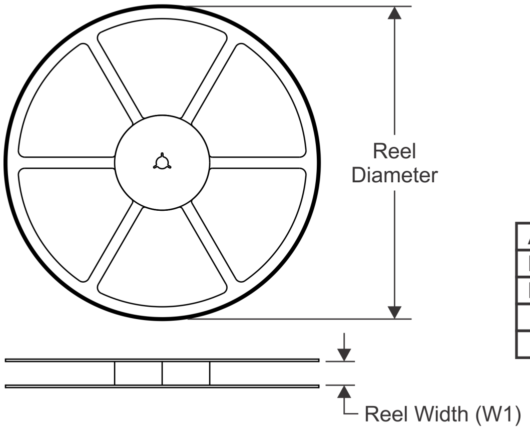
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

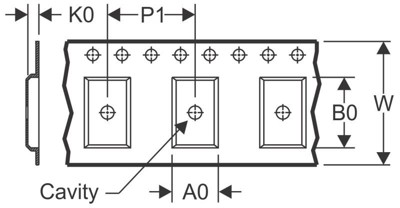
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

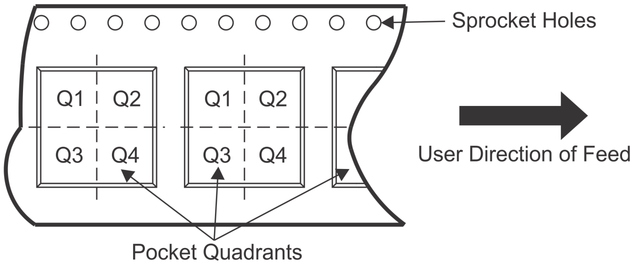


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

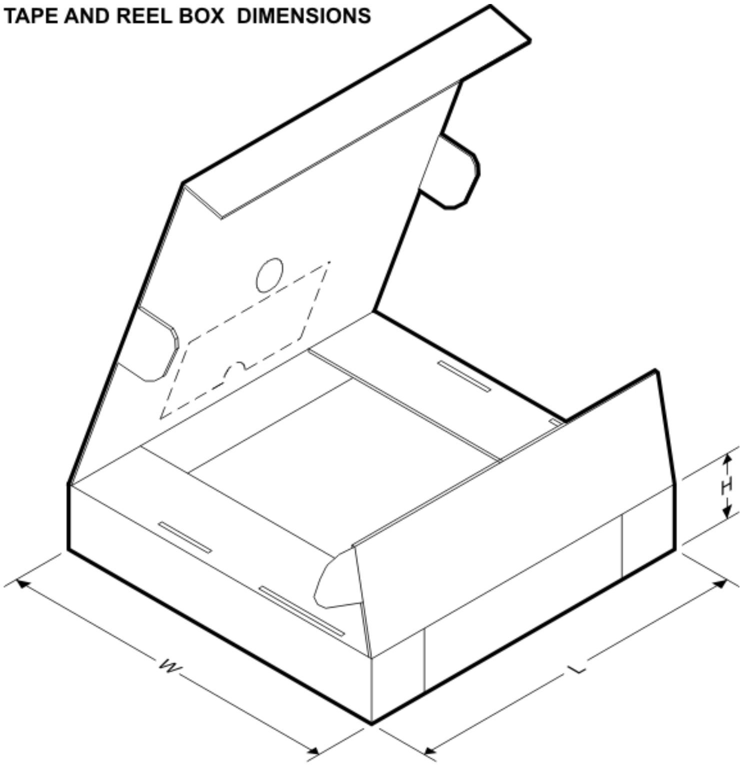
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC05DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC05DR	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
SN74HC05DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC05DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC05DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC05DT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC05NSR	SO	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74HC05PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC05PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC05PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC05PWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

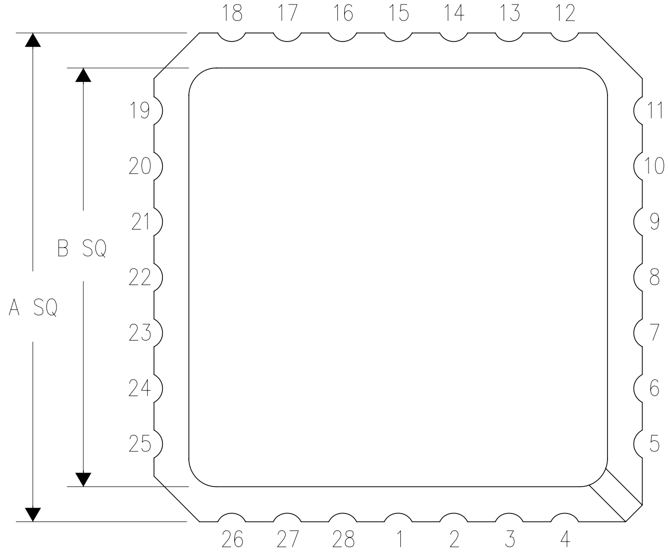


*All dimensions are nominal

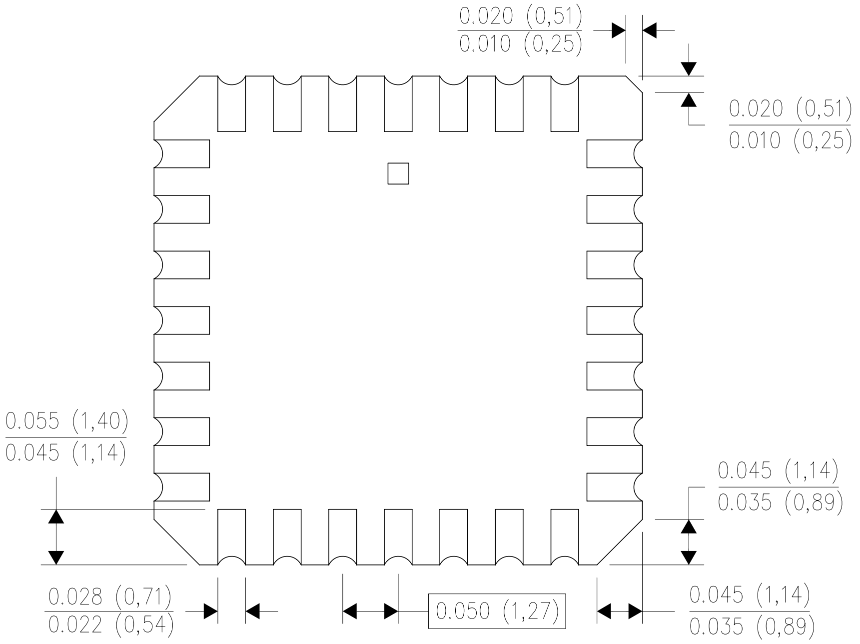
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC05DR	SOIC	D	14	2500	333.2	345.9	28.6
SN74HC05DR	SOIC	D	14	2500	364.0	364.0	27.0
SN74HC05DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74HC05DRG4	SOIC	D	14	2500	333.2	345.9	28.6
SN74HC05DRG4	SOIC	D	14	2500	367.0	367.0	38.0
SN74HC05DT	SOIC	D	14	250	210.0	185.0	35.0
SN74HC05NSR	SO	NS	14	2000	367.0	367.0	38.0
SN74HC05PWR	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74HC05PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74HC05PWRG4	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74HC05PWT	TSSOP	PW	14	250	367.0	367.0	35.0

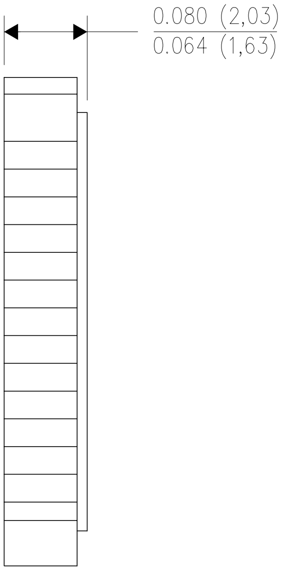
FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



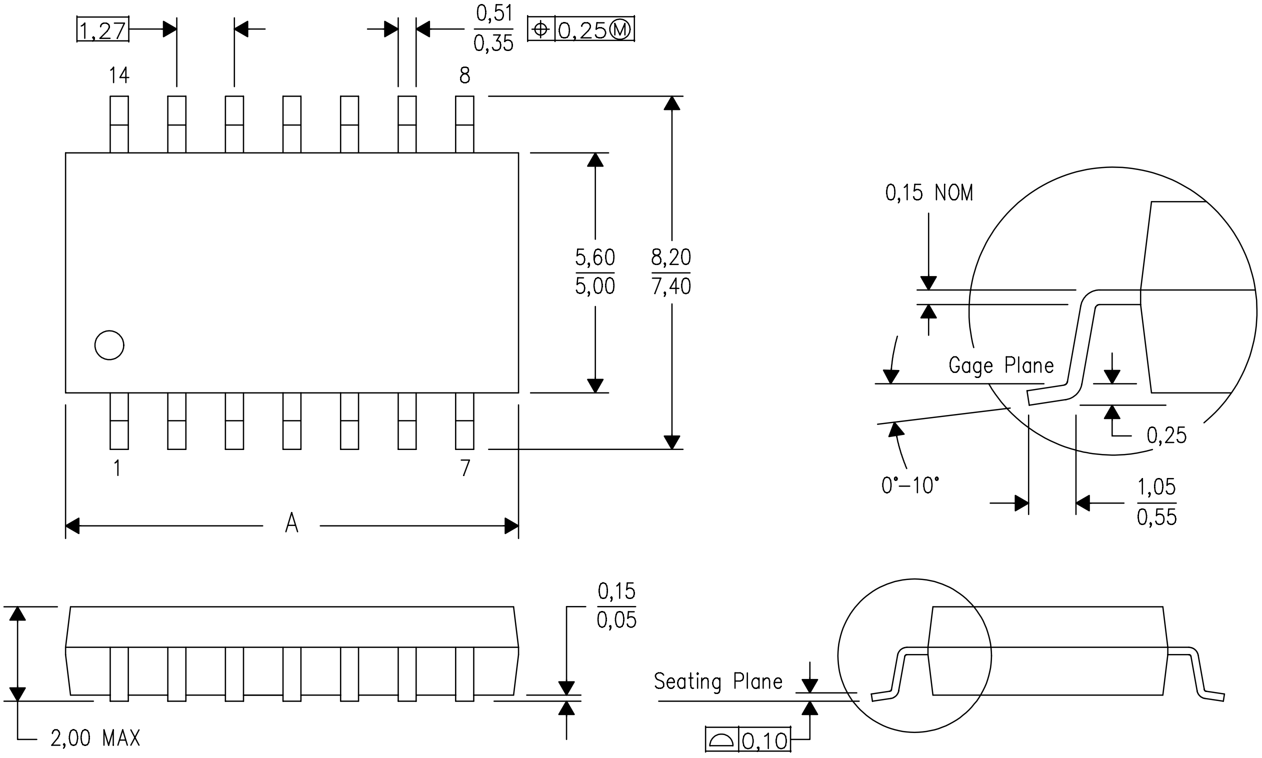


4040140/D 01/11

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS–004

NS (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



PINS ** DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

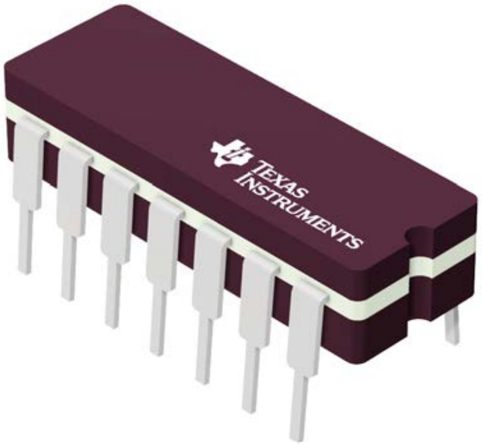
4040062/C 03/03

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J 14

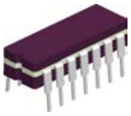
CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

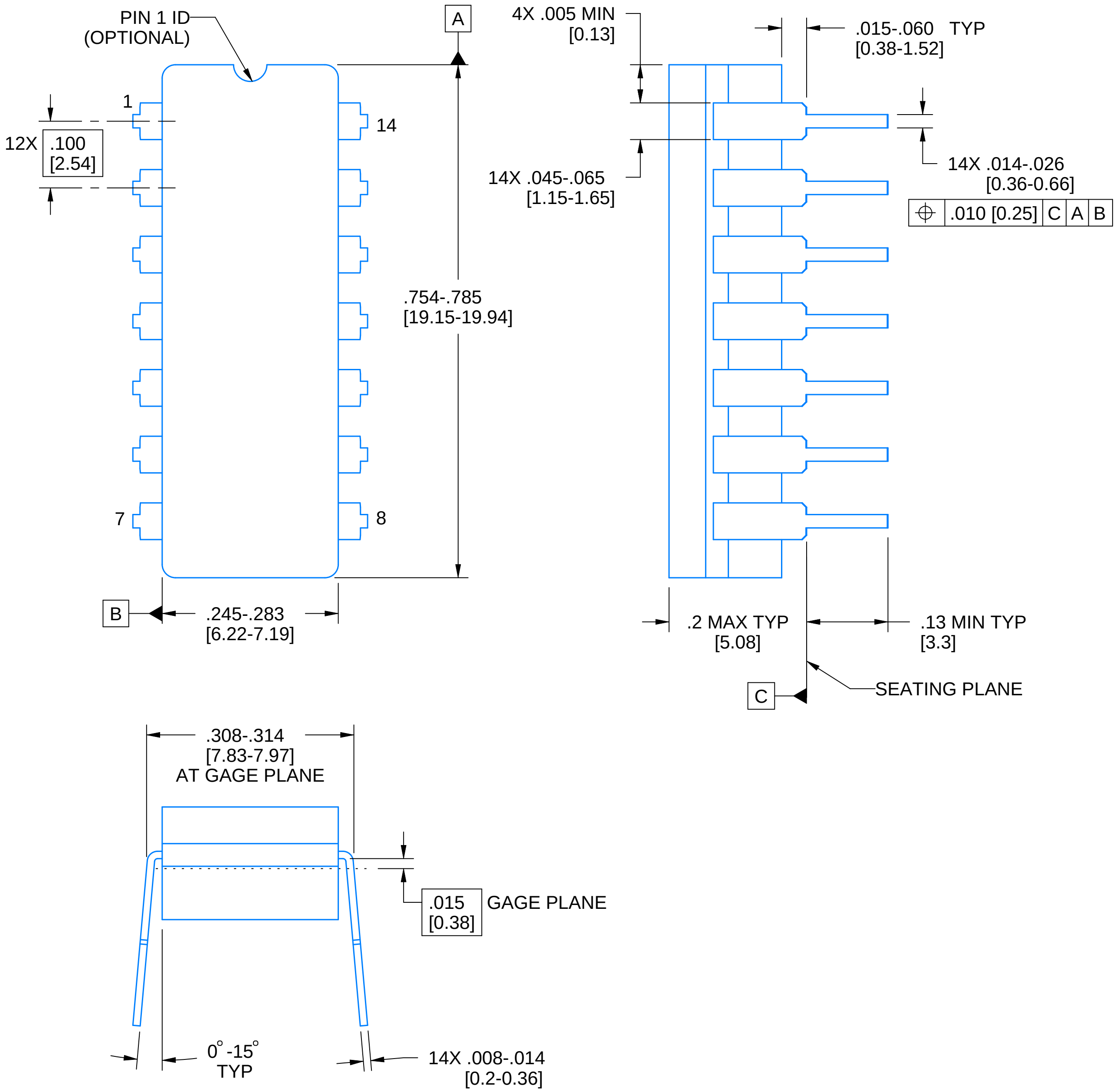
J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE

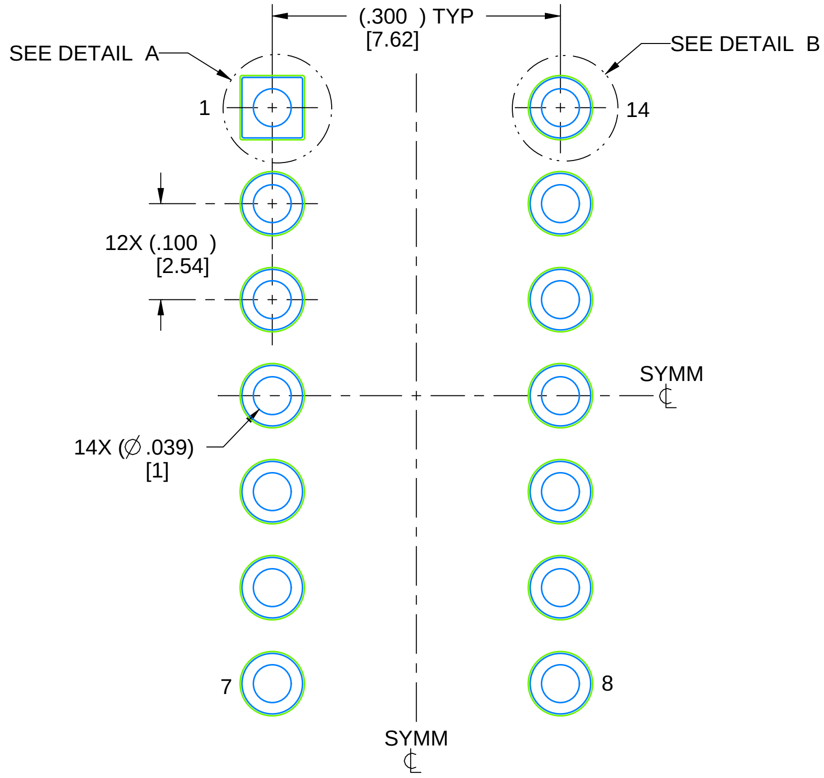


4214771/A 05/2017

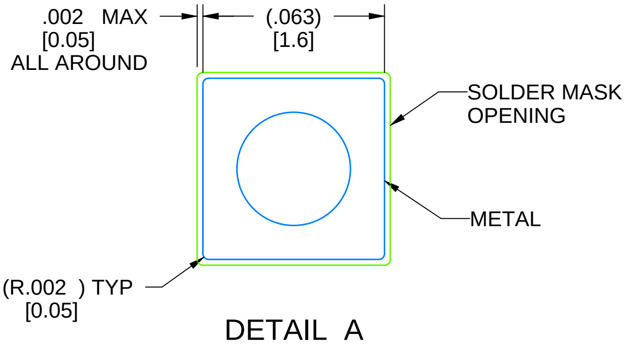
NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

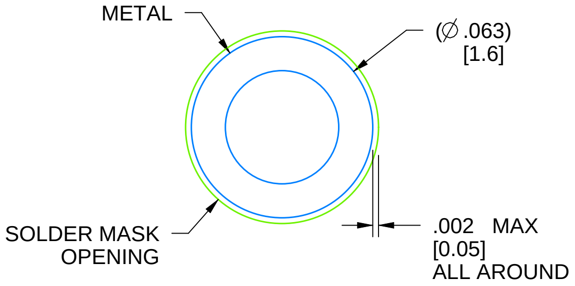
EXAMPLE BOARD LAYOUT



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



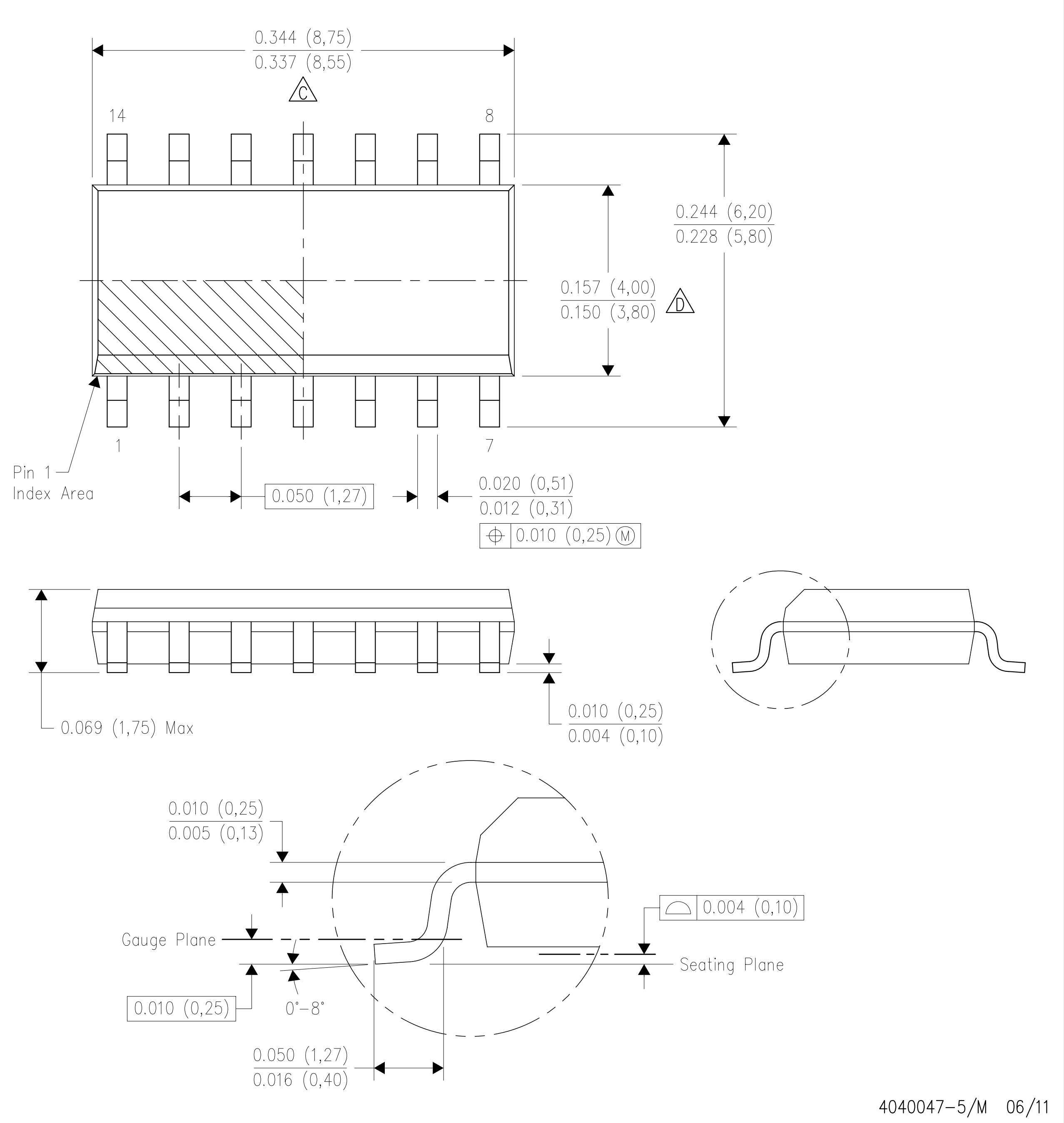
DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

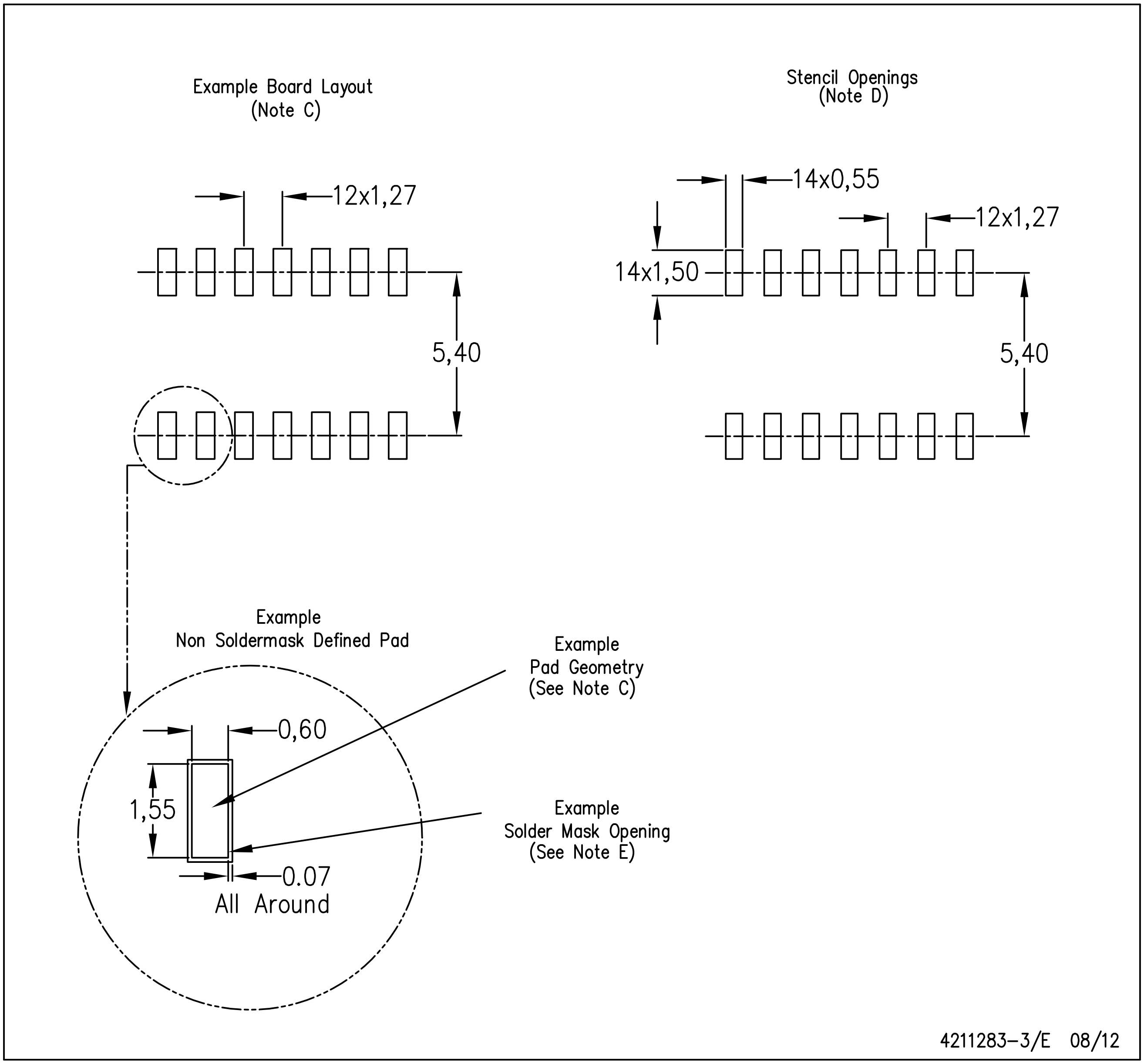
4214771/A 05/2017

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



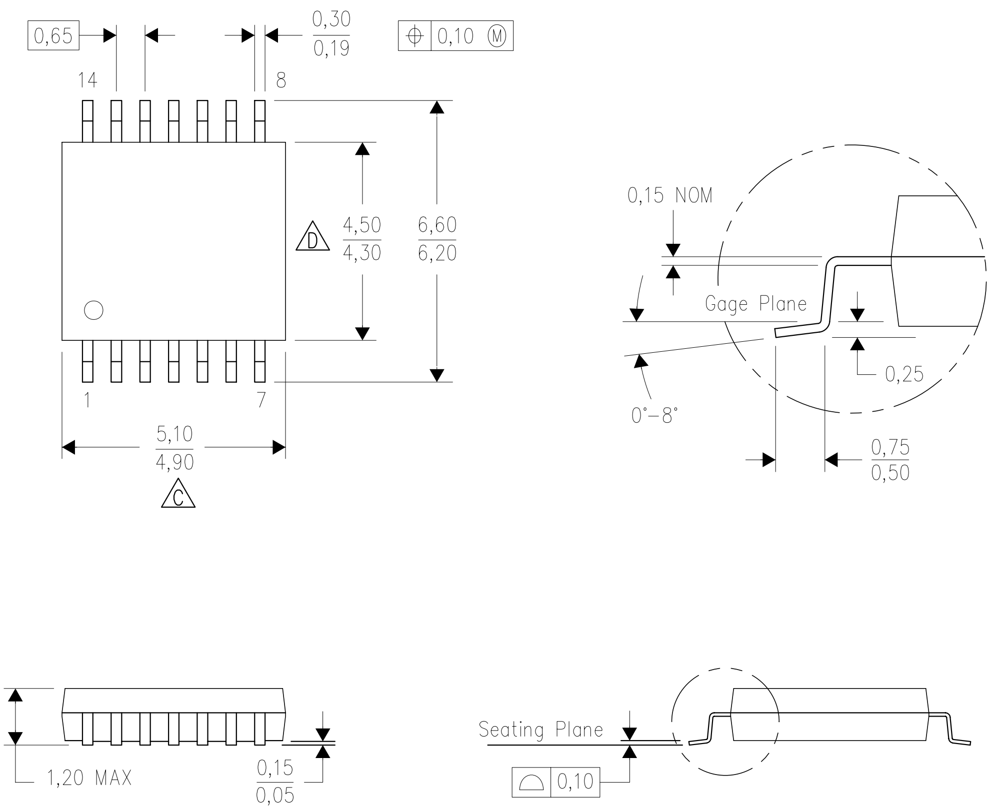
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AB.

D (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.

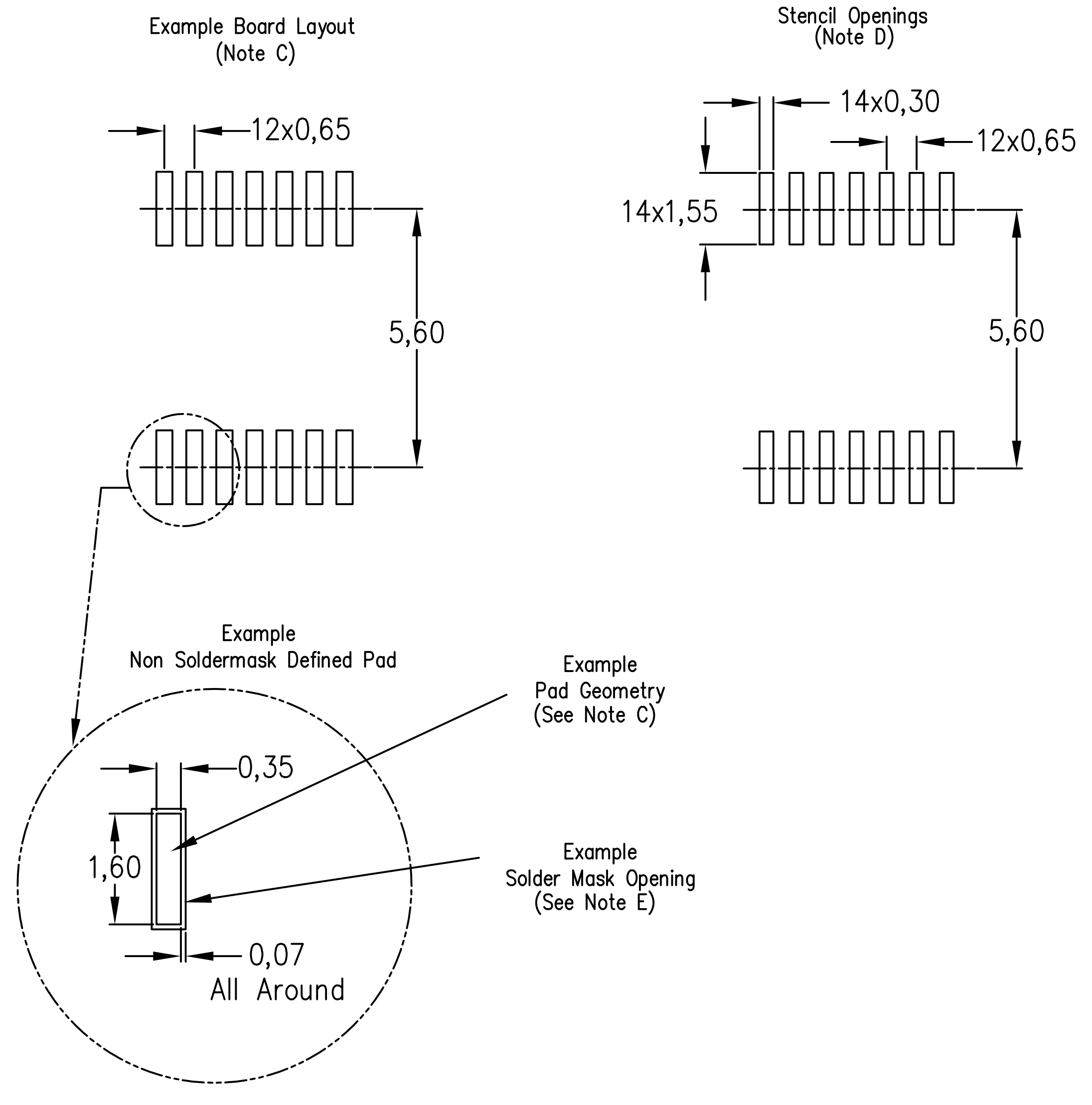
B. This drawing is subject to change without notice.

C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

D Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



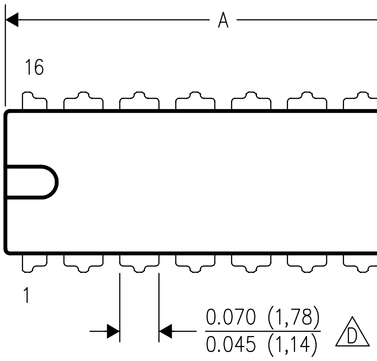
4211284–2/G 08/15

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

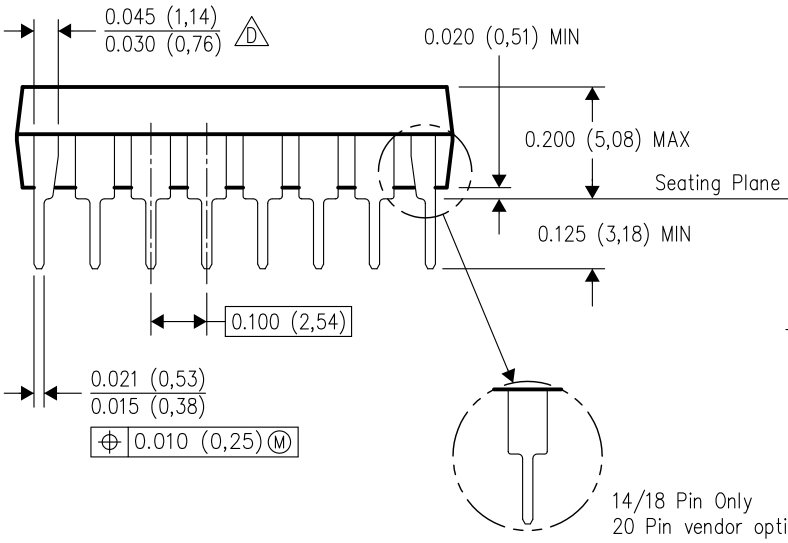
N (R–PDIP–T**)

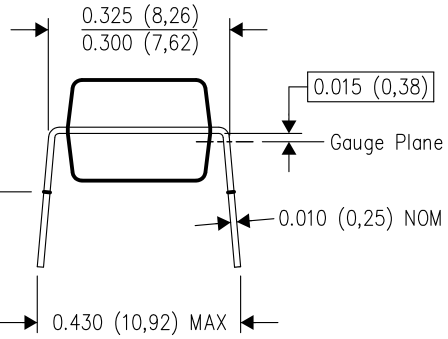
PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
△C MS–001 VARIATION	AA	BB	AC	AD





4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
△C Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
△D The 20 pin end lead shoulder width is a vendor option, either half or full width.

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