TEXAS INSTRUMENTS

DS90UH926Q-Q1

SNLS337M – OCTOBER 2010 – REVISED AUGUST 2017

DS90UH926Q-Q1 720p, 24-Bit Color FPD-Link III Deserializer With HDCP

1 Features

- AEC-Q100 Qualified for Automotive Applications
  - Device Temperature Grade 2: –40°C to +105°C Ambient Operating Temperature
  - Device HBM ESD Classification Level 3B
  - Device CDM ESD Classification Level C6
  - Device MM ESD Classification Level M3
- Integrated HDCP Cipher Engine With On-Chip Key Storage
- Bidirectional Control Interface Channel Interface With I^2C Compatible Serial Control Bus
- Supports High-Definition (720p) Digital Video Format
- RGB888 + VS, HS, DE and I2S Audio Supported
- 5- to 85-MHz PCLK Supported
- Single 3.3-V Operation With 1.8-V or 3.3-V Compatible LVCMOS I/O Interface
- AC-Coupled STP Interconnect up to 10 Meters
- Parallel LVCMOS Video Outputs
- DC-Balanced and Scrambled Data With Embedded Clock
- Adaptive Cable Equalization
- Supports HDCP Repeater Application
- Image Enhancement (White Balance and Dithering) and Internal Pattern Generation
- EMI Minimization (SSCG and EPTO)
- Low Power Modes Minimize Power Dissipation
- Backward-Compatible Modes

2 Applications

- Automotive Display for Navigation
- Rear Seat Entertainment Systems

3 Description

The DS90UH926Q-Q1 deserializer, in conjunction with the DS90UH925Q-Q1 serializer, provides a solution for secure distribution of content-protected digital video within automotive entertainment systems. This chipset translates a parallel RGB video interface into a single-pair high-speed serialized interface. The digital video data is protected using the industry standard HDCP copy protection scheme. The serial bus scheme, FPD-Link III, supports full duplex of high-speed forward data transmission and low-speed backchannel communication over a single differential link. Consolidation of video data and control over a single differential pair reduces the interconnect size and weight, while also eliminating skew issues and simplifying system design.

The DS90UH926Q-Q1 deserializer has a 31-bit parallel LVCMOS output interface to accommodate the RGB, video control, and audio data. The device extracts the clock from a high-speed serial stream. An output LOCK pin provides the link status if the incoming data stream is locked, without the use of a training sequence or special SYNC patterns, as well as a reference clock.

An adaptive equalizer optimizes the maximum cable reach. EMI is minimized by output SSC generation (SSCG) and enhanced progressive turnon (EPTO) features.

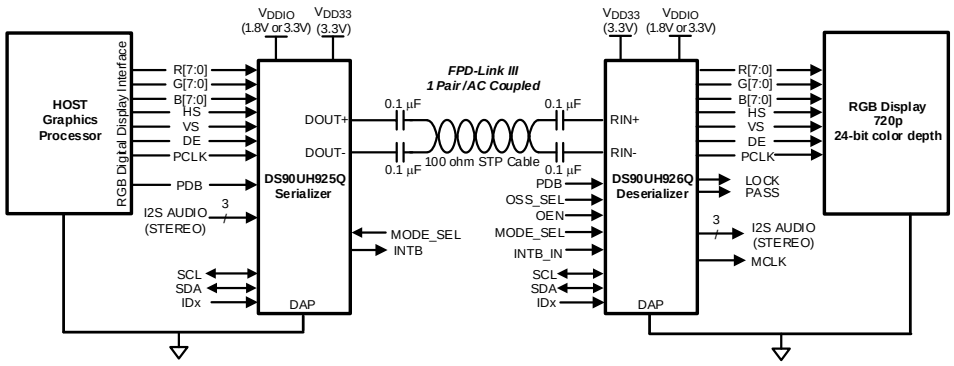
The HDCP cipher engine is implemented in both the serializer and deserializer. HDCP keys are stored in on-chip memory.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS90UH926Q-Q1	WQFN (60)	9.00 mm × 9.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision L (February 2017) to Revision M — **Page**

- Reverted all previous MLCK content changes made in Revision L back to Revision K ... 1
- Removed disable jitter cleaner note ... 5

Changes from Revision K (January 2015) to Revision L — **Page**

- Changed top view pin out diagram ... 4
- Changed CLK to RES2 ... 5
- Added note to disable jitter cleaner ... 5
- Changed MCLK to RES2 ... 5
- Deleted reference to MCLK in this section ... 8
- Deleted reference to MCLK in this section ... 11
- Deleted reference to MCLK ... 25
- Deleted *I2S Jitter Cleaning* section ... 25
- Deleted *MCLK* section ... 25
- Deleted MCLK columns in the *Audio Interface Frequencies* table ... 26
- Changed values in columns 2 to 5 of Configuration Select (MODE_SEL) table ... 29
- Changed values in columns 2 to 5 of IDx table ... 32
- Changed Removed register reference to MCLK ... 42
- Changed Typical Display System Diagram (removed MCLK) ... 47
- Changed Power-Up Requirements and PDB pin description and added Power-Up Sequence graphic. ... 50

Changes from Revision J (April 2013) to Revision K **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

Changes from Revision I (August 2012) to Revision J **Page**

- Changed layout of National Semiconductor data sheet to TI format..... 1

Changes from Revision H (March 2012) to Revision I **Page**

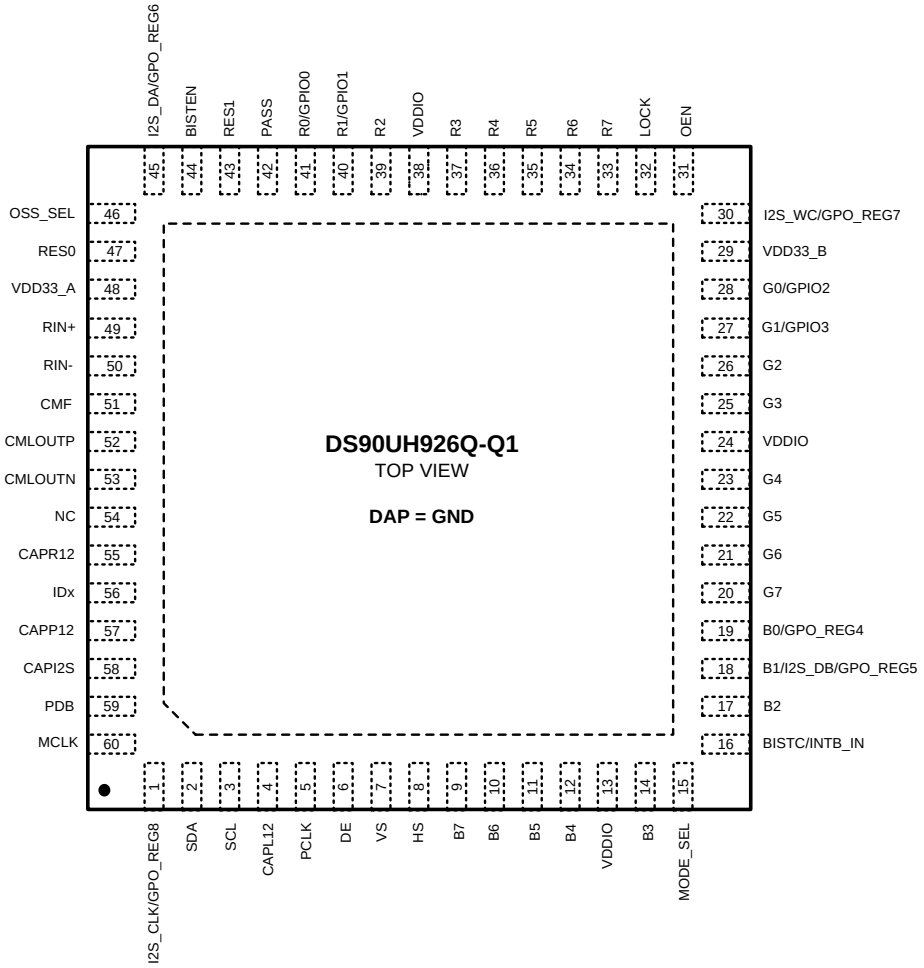
- : Configuration Select (MODE_SEL) #6 I2S Channel B (18–bit Mode) from L to H, corrected typo in table “DC and AC Serial Control Bus Characteristics” from VDDIO to VDD33, added Recommended FRC settings table, added “When backward compatible mode = *ON*, set LFMODE = 0” under Functional Description. Reformatted table 9 and added clarification to notes. Added clarification to notes on Serial Control Bus Registers, address 0x02[3:0] (backwards compatible and LFMODE registers), added “Note: Do not enable SSCG feature if PCLK source into the SER has an SSC clock already.” under Functional Description, EMI REDUCTION FEATURES, Spread Spectrum Clock Generation (SSCG) 1

Changes from Revision G (February 2012) to Revision H **Page**

- Deleted “DC Electrical Characteristics” PDB VDDIO = 1.71 to 1.89 V, added under “SUPPLY CURRENT $I_{DDZ,\ DDIOZ}$, I_{DDIOZ}Max = 10 mA, added under “CML MONITOR DRIVER OUTPUT AC SPECIFICATIONS” E_W Min = 0.3 UI AND E_H Min = 200 mV, added “INTERRUPT PIN — FUNCTIONAL DESCRIPTION AND USAGE (INTB)” under Functional Description section, updated "POWER DOWN (PDB) description under Functional Description from VDDIO to VDDIO = 3 to 3.6 V or V_{DD33}, updated Figure 24 1

5 Pin Configuration and Functions

NKB Package
60 Pin WQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
LVCMOS PARALLEL INTERFACE			
R[7:0]	33, 34, 35, 36, 37, 39, 40, 41	O, LVCMOS with pulldown	RED Parallel Interface Data Output Pins Leave open if unused R0 can optionally be used as GPIO0 and R1 can optionally be used as GPIO1
G[7:0]	20, 21, 22, 23, 25, 26, 27, 28	O, LVCMOS with pulldown	GREEN Parallel Interface Data Output Pins Leave open if unused G0 can optionally be used as GPIO2 and G1 can optionally be used as GPIO3.
B[7:0]	9, 10, 11, 12, 14, 17, 18, 19	O, LVCMOS with pulldown	BLUE Parallel Interface Data Output Pins Leave open if unused B0 can optionally be used as GPO_REG4 and B1 can optionally be used as I2S_DB or GPO_REG5.
HS	8	O, LVCMOS with pulldown	Horizontal Sync Output Pin Video control signal pulse width must be 3 PCLKs or longer to be transmitted when the Control Signal Filter is enabled. There is no restriction on the minimum transition pulse when the Control Signal Filter is disabled. The signal is limited to 2 transitions per 130 PCLKs. See Table 11

Pin Functions (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
VS	7	O, LVCMOS with pulldown	Vertical Sync Output Pin Video control signal is limited to 1 transition per 130 PCLKs. Thus, the minimum pulse width is 130 PCLKs.
DE	6	O, LVCMOS with pulldown	Data Enable Output Pin Video control signal pulse width must be 3 PCLKs or longer to be transmitted when the Control Signal Filter is enabled. There is no restriction on the minimum transition pulse when the Control Signal Filter is disabled. The signal is limited to 2 transitions per 130 PCLKs. See Table 11
PCLK	5	O, LVCMOS with pulldown	Pixel Clock Output Pin. Strobe edge set by RFB configuration register. See Table 11
I2S_CLK, I2S_WC, I2S_DA	1, 30, 45	O, LVCMOS with pulldown	Digital Audio Interface Data Output Pins Leave open if unused I2S_CLK can optionally be used as GPO_REG8, I2S_WC can optionally be used as GPO_REG7, and I2S_DA can optionally be used as GPO_REG6.
MCLK	60	O, LVCMOS with pulldown	I2S Master Clock Output x1, x2, or x4 of I2S_CLK Frequency
OPTIONAL PARALLEL INTERFACE			
I2S_DB	18	O, LVCMOS with pulldown	Second Channel Digital Audio Interface Data Output pin at 18–bit color mode and set by MODE_SEL or configuration register Leave open if unused I2S_B can optionally be used as BI or GPO_REG5.
GPIO[3:0]	27, 28, 40, 41	I/O, LVCMOS with pulldown	Standard General Purpose IOs. Available only in 18-bit color mode, and set by MODE_SEL or configuration register. See Table 11 Leave open if unused Shared with G1, G0, R1 and R0.
GPO_REG[8:4]	1, 30, 45, 18, 19	O, LVCMOS with pulldown	General Purpose Outputs and set by configuration register. See Table 11 Shared with I2S_CLK, I2S_WC, I2S_DA, I2S_DB or B1, B0.
INTB_IN	16	Input, LVCMOS with pulldown	Interrupt Input Shared with BISTC
CONTROL			
PDB	59	I, LVCMOS with pulldown	Power-down Mode Input Pin PDB = H, device is enabled (normal operation) Refer to *Power Supply Recommendations*. PDB = L, device is powered down. When the device is in the POWER DOWN state, the LVCMOS Outputs are in TRI-STATE, the PLL is shutdown and IDD is minimized.
OEN	31	Input, LVCMOS with pulldown	Output Enable Pin. See Table 8
OSS_SEL	46	Input, LVCMOS with pulldown	Output Sleep State Select Pin. See Table 8
MODE_SEL	15	I, Analog	Device Configuration Select. See Table 9
BISTEN	44	I, LVCMOS with pulldown	BIST Enable Pin. 0: BIST Mode is disabled. 1: BIST Mode is enabled.
BISTC	16	I, LVCMOS with pulldown	BIST Clock Select. Shared with INTB_IN 0: PCLK; 1: 33 MHz

Pin Functions (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
I2C			
IDx	56	I, Analog	I2C Serial Control Bus Device ID Address Select External pull-up to V_{DD33} is required under all conditions, DO NOT FLOAT. Connect to external pullup and pulldown resistor to create a voltage divider. See Figure 23
SCL	3	I/O, LVCMOS Open-Drain	I2C Clock Input / Output Interface Must have an external pullup to V_{DD33}, DO NOT FLOAT. Recommended pullup: 4.7 kΩ.
SDA	2	I/O, LVCMOS Open-Drain	I2C Data Input / Output Interface Must have an external pullup to V_{DD33}, DO NOT FLOAT. Recommended pullup: 4.7 kΩ.
STATUS			
LOCK	32	O, LVCMOS with pulldown	LOCK Status Output Pin 0: PLL is unlocked, RGB[7:0], I2S[2:0], HS, VS, DE and PCLK output states are controlled by OEN. May be used as Link Status or Display Enable 1: PLL is Locked, outputs are active
PASS	42	O, LVCMOS with pulldown	PASS Output Pin 0: One or more errors were detected in the received payload 1: ERROR FREE Transmission Leave Open if unused. Route to test point (pad) recommended
FPD-LINK III SERIAL INTERFACE			
RIN+	49	I, LVDS	True Input. The interconnection should be AC-coupled to this pin with a 0.1 μF capacitor.
RIN–	50	I, LVDS	Inverting Input. The interconnection should be AC-coupled to this pin with a 0.1 μF capacitor.
CMLOUTP	52	O, LVDS	True CML Output Monitor point for equalized differential signal
CMLOUTN	53	O, LVDS	Inverting CML Output Monitor point for equalized differential signal
CMF	51	Analog	Common Mode Filter. Connect 0.1-μF capacitor to GND.
POWER(1) AND GROUND			
VDD33_A, VDD33_B	48, 29	Power	Power to on-chip regulator **3 V – 3.6 V**. Requires 4.7 uF to GND at each VDD pin.
V_{DDIO}	13, 24, 38	Power	LVCMOS I/O Power **1.8 V ±5% OR 3 V – 3.6 V**. Requires 4.7 uF to GND at each VDDIO pin.
GND	DAP	Ground	DAP is the large metal contact at the bottom side, located at the center of the WQFN package. **Connect to the ground plane** (GND) with at least 9 vias.
REGULATOR CAPACITOR			
CAPR12	55	CAP	Decoupling capacitor connection for on-chip regulator. Requires a 4.7-μF to GND at each CAP pin.
CAPP12	57		
CAPI2S	58		
CAPL12	4	CAP	Decoupling capacitor connection for on-chip regulator. Requires two 4.7-μF to GND at this CAP pin.
OTHERS			
NC	54	NC	No connect. This pin may be left open or tied to any level.
RES[1:0]	43.47	GND	Reserved - tie to Ground

(1) The VDD (V_{DD33} and V_{DDIO}) supply ramp should be faster than 1.5 ms with a monotonic rise.

6 Specifications

6.1 Absolute Maximum Ratings

See (1)(2)(3)

		MIN	MAX	UNIT
Supply voltage – V_{DD33}		−0.3	4	V
Supply voltage – V_{DDIO}		−0.3	4	V
LVCMOS I/O voltage		−0.3	(V_{DDIO} + 0.3)	V
Deserializer input voltage		−0.3	2.75	V
Junction temperature			150	°C
60-pin WQFN Package Maximum power dissipation capacity at 25°C	Derate above 25 °C		1/ $R_{\theta JA}$	°C/W
	$R_{\theta JA}$		31	°C/W
	$R_{\theta JC}$		2.4	°C/W
Storage temperature, T_{stg}		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) For soldering specifications, see product folder at www.ti.com and *Absolute Maximum Ratings for Soldering* (SNOA549).

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±8000	V
		Charged-device model (CDM), per AEC Q100-011		±1250	
		Machine model, all pins		±250	
		(IEC, powered-up only) R_D = 330 Ω, C_S = 150 pF	Air Discharge (Pin 49 and 50)	±15000	
			Contact Discharge (Pin 49 and 50)	±8000	
		(ISO10605) R_D = 330 Ω, C_S = 150 pF	Air Discharge (Pin 49 and 50)	±15000	
			Contact Discharge (Pin 49 and 50)	±8000	
		(ISO10605) R_D = 2 kΩ, C_S = 150 & 330 pF	Air Discharge (Pin 49 and 50)	±15000	
			Contact Discharge (Pin 49 and 50)	±8000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage (V_{DD33})		3	3.3	3.6	V
LVCMOS supply voltage (V_{DDIO})	Connect V_{DDIO} to 3.3 V and use 3.3-V IOs	3	3.3	3.6	V
	Connect V_{DDIO} to 1.8 V and use 1.8-V IOs	1.71	1.8	1.89	V
Operating free air temperature (T_A)		−40	25	105	°C
PCLK frequency		5		85	MHz
Supply noise(1)				100	mV_{P-P}

(1) Supply noise testing was done with minimum capacitors on the PCB. A sinusoidal signal is AC-coupled to the V_{DD33} and V_{DDIO} supplies with amplitude = 100 mVp-p measured at the device V_{DD33} and V_{DDIO} pins. Bit error rate testing of input to the Ser and output of the Des with 10-meter cable shows no error when the noise frequency on the Ser is less than 50 MHz. The Des on the other hand shows no error when the noise frequency is less than 50 MHz.

6.4 Thermal Information

THERMAL METRIC[1]		DS90UH926Q-Q1 NKB (WQFN) 60 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	26.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	8.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.1	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

6.5 DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.[1][2][3]

PARAMETER		TEST CONDITIONS		PIN/FREQ.	MIN	TYP	MAX	UNIT
LVCMOS I/O DC SPECIFICATIONS								
V_{IH}	High Level Input Voltage	V_{DDIO} = 3 to 3.6 V		PDB	2		V_{DDIO}	V
V_{IL}	Low Level Input Voltage	V_{DDIO} = 3 to 3.6 V		PDB	GND		0.8	V
I_{IN}	Input Current	V_{IN} = 0 V or V_{DDIO} = 3 to 3.6 V		PDB	−10	±1	10	µA
V_{IH}	High Level Input Voltage	V_{DDIO} = 3 to 3.6 V		OEN, OSS_SEL, BISTEN, BISTC / INTB_IN, GPIO[3:0]	2		V_{DDIO}	V
		V_{DDIO} = 1.71 to 1.89 V			0.65 × V_{DDIO}		V_{DDIO}	V
V_{IL}	Low Level Input Voltage	V_{DDIO} = 3 to 3.6 V			GND		0.8	V
		V_{DDIO} = 1.71 to 1.89 V			GND		0.35 × V_{DDIO}	V
I_{IN}	Input Current	V_{IN} = 0 V or V_{DDIO}	V_{DDIO} = 3 to 3.6 V		−10	±1	10	µA
			V_{DDIO} = 1.7 to 1.89 V		−10	±1	10	µA
V_{OH}	High Level Output Voltage	I_{OH} = −4 mA	V_{DDIO} = 3 to 3.6 V	R[7:0], G[7:0], B[7:0], HS, VS, DE, PCLK, LOCK, PASS, MCLK, I2S_CLK, I2S_WC, I2S_DA, I2S_DB, GPO_REG[8:4]	2.4		V_{DDIO}	V
			V_{DDIO} = 1.7 to 1.89 V		V_{DDIO}-0.45		V_{DDIO}	V
V_{OL}	Low Level Output Voltage	I_{OL} = 4 mA	V_{DDIO} = 3 to 3.6 V		GND		0.4	V
			V_{DDIO} = 1.7 to 1.89 V		GND		0.35	V
I_{OS}	Output Short-Circuit Current	V_{OUT} = 0 V				−60		mA
I_{OZ}	Tri-state Output Current	V_{OUT} = 0 V or V_{DDIO}, PDB = L			−10		10	µA

(1) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the electrical characteristics conditions and/or notes. Typical specifications are estimations only and are not ensured.
(2) Typical values represent most likely parametric norms at V_{DD} = 3.3 V, T_A = 25 °C, and at *Recommended Operating Conditions* at the time of product characterization and are not ensured.
(3) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except VOD and ΔVOD, which are differential voltages.

DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.(1)(2)(3)

PARAMETER		TEST CONDITIONS		PIN/FREQ.	MIN	TYP	MAX	UNIT
FPD-LINK III CML RECEIVER INPUT DC SPECIFICATIONS								
V_{TH}	Differential Threshold High Voltage	V_{CM} = 2.5 V (Internal V_{BIAS})		RIN+, RIN–			50	mV
V_{TL}	Differential Threshold Low Voltage				−50			mV
V_{CM}	Differential Common-mode Voltage					1.8		V
R_T	Internal Termination Resistor - Differential				80	100	120	Ω
CML MONITOR DRIVER OUTPUT DC SPECIFICATIONS								
V_{ODp-p}	Differential Output Voltage	R_L = 100 Ω		CMLOUTP, CMLOUTN	360			mVp-p
SUPPLY CURRENT								
I_{DD1}	Supply Current (includes load current) f = 85 MHz	C_L = 12 pF, Checker Board Pattern Figure 1	V_{DD33}= 3.6 V	V_{DD33}		125	145	mA
I_{DDIO1}			V_{DDIO}= 3.6 V	V_{DDIO}		110	118	mA
			V_{DDIO} = 1.89 V			60	75	
I_{DD2}	Supply Current (includes load current) f = 85 MHz	C_L = 4 pF Checker Board Pattern, Figure 1	V_{DD33} = 3.6 V	V_{DD33}		125	145	mA
I_{DDIO2}			V_{DDIO} = 3.6 V	V_{DDIO}		75	85	mA
			V_{DDIO} = 1.89 V			50	65	
I_{DDS}	Supply Current Sleep Mode	Without Input Serial Stream	V_{DD33} = 3.6 V	V_{DD33}		90	115	mA
I_{DDIOS}			V_{DDIO} = 3.6 V	V_{DDIO}		3	5	mA
			V_{DDIO} = 1.89 V			2	3	
I_{DDZ}	Supply Current Power Down	PDB = L, All LVCMOS inputs are floating or tied to GND	V_{DD33} = 3.6 V	V_{DD33}		2	10	mA
I_{DDIOZ}			V_{DDIO} = 3.6 V	V_{DDIO}		0.05	10	mA
			V_{DDIO} = 1.89 V			0.05	10	

6.6 AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.(1)(2)(3)

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
GPIO BIT RATE							
B_R	Forward Channel Bit Rate	See(4) (5)	f = 5 – 85 MHz, GPIO[3:0]		0.25 × f		Mbps
	Back Channel Bit Rate			> 50	> 75		kbps
CML MONITOR DRIVER OUTPUT AC SPECIFICATIONS							
E_W	Differential Output Eye Opening Width(6)	R_L = 100 Ω, Jitter Freq > f / 40 Figure 2 (4)(5)	CMLOUTP, CMLOUTN, f = 85 MHz	0.3	0.4		UI
E_H	Differential Output Eye Height			200	300		mV
BIST MODE							
t_{PASS}	BIST PASS Valid Time BISTEN = H Figure 8 (4)(5)		PASS		800		ns
SSCG MODE							
f_{DEV}	Spread Spectrum Clocking Deviation Frequency	SeeFigure 14, Table 1 and Table 2 (4)(5)	f = 85 MHz, SSCG = *ON*	±0.5%		±2.5%	
f_{MOD}	Spread Spectrum Clocking Modulation Frequency			8		100	kHz

(1) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the electrical characteristics conditions and/or notes. Typical specifications are estimations only and are not ensured.
(2) Typical values represent most likely parametric norms at V_{DD} = 3.3 V, T_A = 25 °C, and at *Recommended Operating Conditions* at the time of product characterization and are not ensured.
(3) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except VOD and ΔVOD, which are differential voltages.
(4) Specification is ensured by characterization and is not tested in production.
(5) Specification is ensured by design and is not tested in production.
(6) UI – Unit Interval is equivalent to one serialized data bit width (1UI = 1 / 35 × PCLK). The UI scales with PCLK frequency.

6.7 DC and AC Serial Control Bus Characteristics

Over 3.3-V supply and temperature ranges unless otherwise specified.(1) (2) (3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input High Level	SDA and SCL	0.7 × V_{DD33}		V_{DD33}	V
V_{IL}	Input Low Level Voltage	SDA and SCL	GND		0.3 × V_{DD33}	V
V_{HY}	Input Hysteresis			> 50		mV
V_{OL}		SDA, IOL = 1.25 mA	0		0.36	V
I_{IN}		SDA or SCL, V_{IN} = V_{DD33} or GND	–10		10	µA
t_R	SDA Rise Time – READ	SDA, RPU = 10 kΩ, Cb ≤ 400 pF, Figure 9		430		ns
t_F	SDA Fall Time – READ			20		ns
$t_{SU;DAT}$	Setup Time — READ	SeeFigure 9		560		ns
$t_{HD;DAT}$	Holdup Time — READ	SeeFigure 9		615		ns
t_{SP}	Input Filter			50		ns
C_{IN}	Input Capacitance	SDA or SCL		<5		pF

(1) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the electrical characteristics conditions and/or notes. Typical specifications are estimations only and are not ensured.
(2) Typical values represent most likely parametric norms at V_{DD} = 3.3 V, T_A = 25 °C, and at *Recommended Operating Conditions* at the time of product characterization and are not ensured.
(3) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except VOD and ΔVOD, which are differential voltages.

6.8 Recommended Timing Requirements for the Serial Control Bus

Over 3.3-V supply and temperature ranges unless otherwise specified.

			MIN	NOM	MAX	UNIT
f_{SCL}	SCL Clock Frequency	Standard Mode	0		100	kHz
		Fast Mode	0		400	kHz
t_{LOW}	SCL Low Period	Standard Mode	4.7			µs
		Fast Mode	1.3			µs
t_{HIGH}	SCL High Period	Standard Mode	4			µs
		Fast Mode	0.6			µs
$t_{HD;STA}$	Hold time for a start or a repeated start condition Figure 9	Standard Mode	4			µs
		Fast Mode	0.6			µs
$t_{SU:STA}$	Setup time for a start or a repeated start condition Figure 9	Standard Mode	4.7			µs
		Fast Mode	0.6			µs
$t_{HD;DAT}$	Data Hold Time Figure 9	Standard Mode	0		3.45	µs
		Fast Mode	0		0.9	µs
$t_{SU;DAT}$	Data Setup Time Figure 9	Standard Mode	250			ns
		Fast Mode	100			ns
$t_{SU;STO}$	Setup Time for STOP Condition, Figure 9	Standard Mode	4			µs
		Fast Mode	0.6			µs
t_{BUF}	Bus Free Time Between STOP and START, Figure 9	Standard Mode	4.7			µs
		Fast Mode	1.3			µs
t_r	SCL and SDA Rise Time, Figure 9	Standard Mode			1000	ns
		Fast Mode			300	ns
t_f	SCL and SDA Fall Time, Figure 9	Standard Mode			300	ns
		Fast mode			300	ns

6.9 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
t_{RCP}	PCLK Output Period	$t_{RCP} = t_{TCP}$	PCLK	11.76	T	200	ns
t_{RDC}	PCLK Output Duty Cycle			45%	50%	55%	
t_{CLH}	LVCMOS Low-to-High Transition Time Figure 3	V_{DDIO} = 1.71 to 1.89 V, C_L = 12 pF	R[7:0], G[7:0], B[7:0], HS, VS, DE, PCLK, LOCK, PASS, MCLK, I2S_CLK, I2S_WC, I2S_DA, I2S_DB		2	3	ns
		V_{DDIO} = 3 to 3.6 V, C_L = 12 pF			2	3	ns
t_{CHL}	LVCMOS High-to-Low Transition Time Figure 3	V_{DDIO} = 1.71 to 1.89 V, C_L = 12 pF			2	3	ns
		V_{DDIO} = 3 to 3.6 V, C_L = 12 pF			2	3	ns
t_{ROS}	Data Valid before PCLK – Setup Time SSCG = *OFF* Figure 6	V_{DDIO} = 1.71 to 1.89 V, C_L = 12 pF		2.2			ns
		V_{DDIO} = 3 to 3.6 V, C_L = 12 pF		2.2			ns
t_{ROH}	Data Valid after PCLK – Hold Time SSCG = *OFF* Figure 6	V_{DDIO} = 1.71 to 1.89 V, C_L = 12 pF		3			ns
		V_{DDIO} = 3 to 3.6 V, C_L = 12 pF		3			ns

Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
t_{XZR}	Active to *OFF* Delay Figure 5 (1) (2)	OEN = L, OSS_SEL = H	R[7:0], G[7:0], B[7:0]		10		ns
			HS, VS, DE, PCLK, LOCK, PASS		15		ns
			MCLK,I2S_CLK, I2S_WC, I2S_DA, I2S_DB		60		ns
t_{DDLT}	Lock Time Figure 5 (1) (2) (3)	SSCG = *OFF*	f = 5 – 85 MHz		5	40	ms
t_{DD}	Delay – Latency (1) (2)		f = 5 – 85 MHz		147 × T		ns
t_{DCCJ}	Cycle-to-Cycle Jitter (1) (2)	SSCG = *OFF*	f = 5 to <15 MHz		0.5		ns
			f = 15 to 85 MHz		0.2		ns
			I2S_CLK = 1 to 12.28 MHz		±2		ns
t_{ONS}	Data Valid After OEN = H SetupTime Figure 7 (1) (2)	VDDIO = 1.71 to 1.89 V, CL = 12 pF	R[7:0], G[7:0], B[7:0], HS, VS, DE, PCLK, MCLK,I2S_CLK, I2S_WC, I2S_DA, I2S_DB		50		ns
		VDDIO = 3 to 3.6 V, CL = 12 pF			50		ns
t_{ONH}	Data Tri-State After OEN = L SetupTime Figure 7 (1) (2)	VDDIO = 1.71 to 1.89 V, CL = 12 pF			50		ns
		VDDIO = 3 to 3.6 V, CL = 12 pF			50		ns
t_{SES}	Data Tri-State after OSS_ SEL = H, Setup Time Figure 7 (1) (2)	VDDIO = 1.71 to 1.89 V, CL = 12 pF			5		ns
		VDDIO = 3 to 3.6 V, CL = 12 pF			5		ns
t_{SEH}	Data to Low after OSS_SEL = L Setup Time Figure 7 (1) (2)	VDDIO = 1.71 to 1.89 V, CL = 12 pF			5		ns
		VDDIO = 3 to 3.6 V, CL = 12 pF			5		ns

(1) Specification is ensured by characterization and is not tested in production.
(2) Specification is ensured by design and is not tested in production.
(3) t_{DDLT} is the time required by the device to obtain lock when exiting power-down state with an active serial stream.

6.10 Timing Diagrams

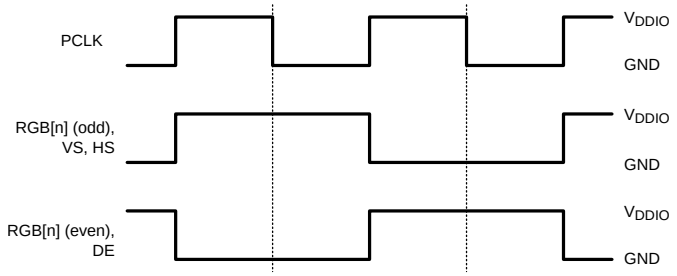


Figure 1. Checker Board Data Pattern

Timing Diagrams (continued)

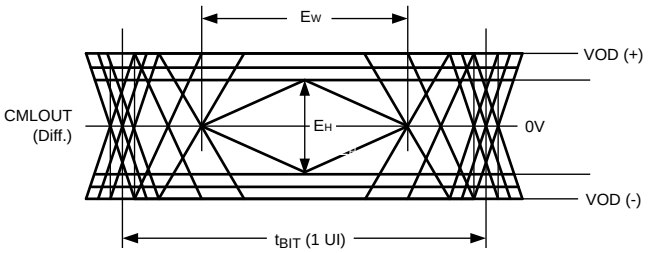


Figure 2. CML Output Driver

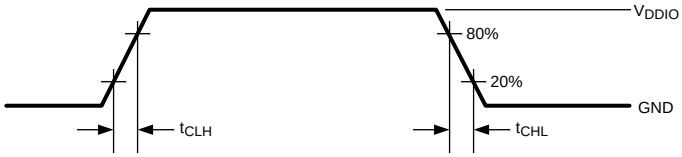


Figure 3. LVCMOS Transition Times

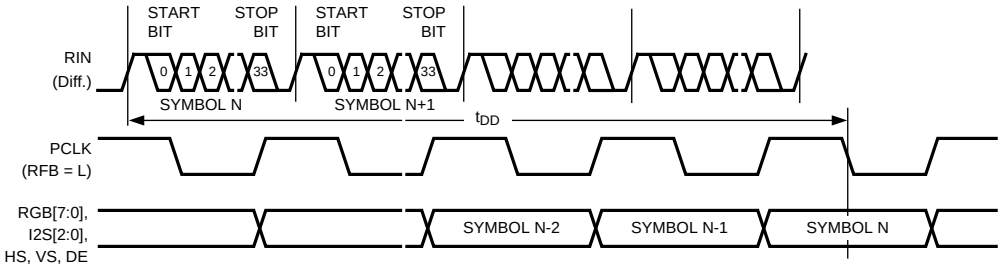


Figure 4. Delay - Latency

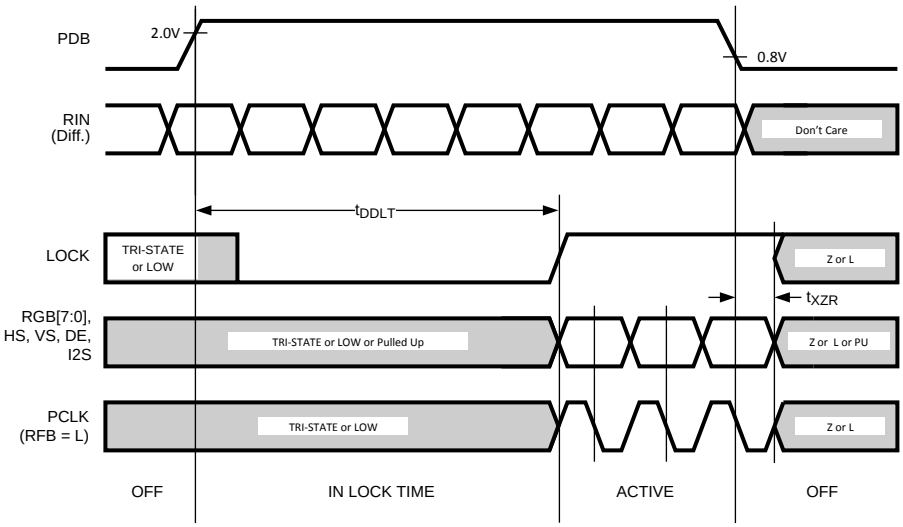


Figure 5. PLL Lock Times and PDB Tri-State Delay

Timing Diagrams (continued)

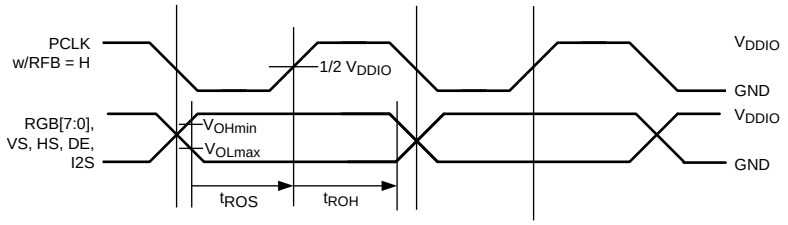


Figure 6. Output Data Valid (Setup and Hold) Times With SSCG = *OFF*

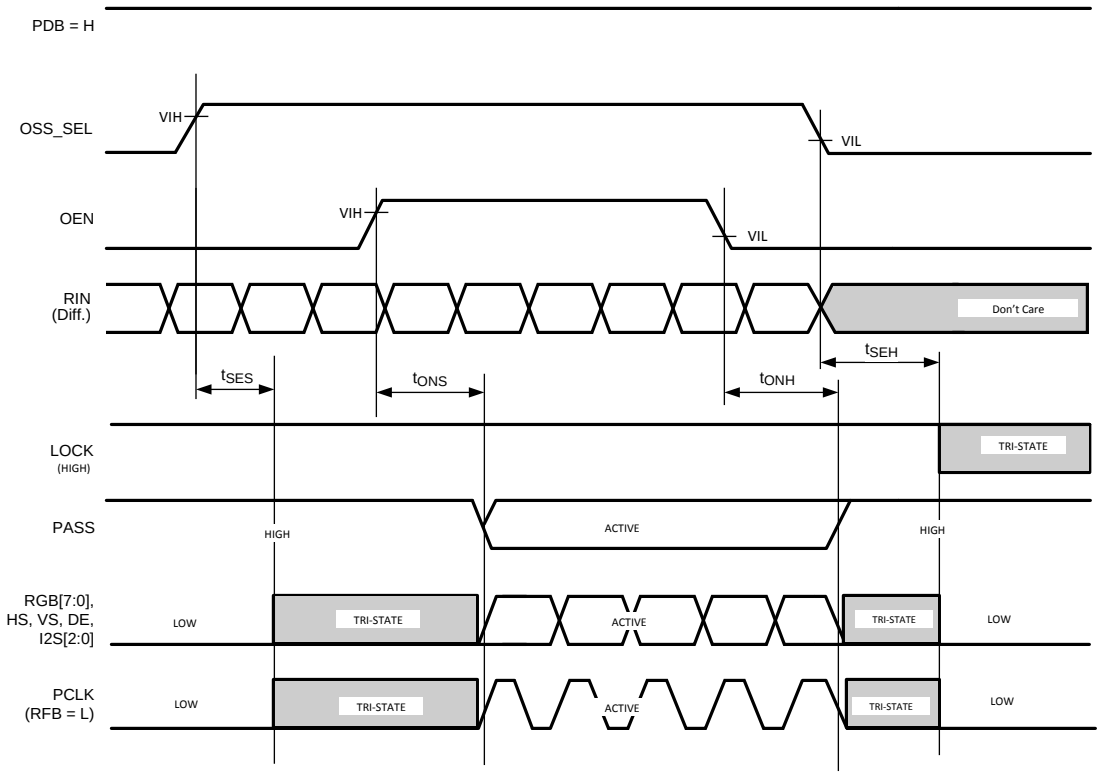


Figure 7. Output State (Setup and Hold) Times

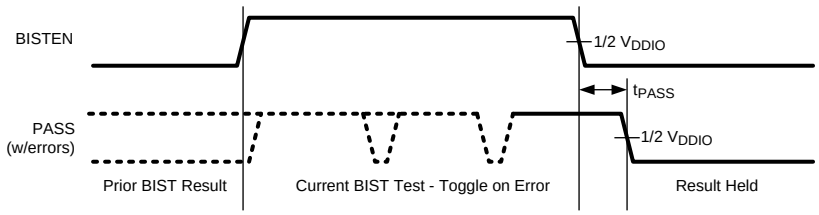


Figure 8. BIST PASS Waveform

Timing Diagrams (continued)

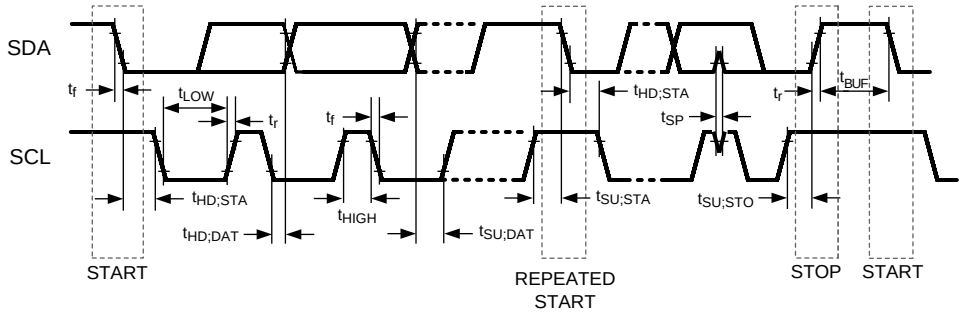
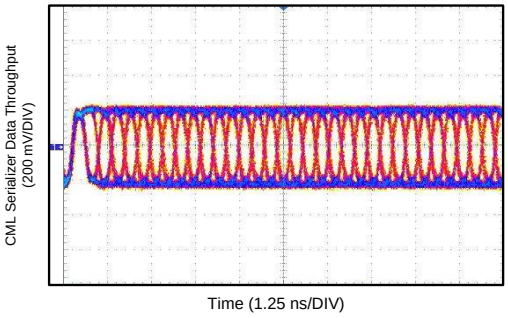


Figure 9. Serial Control Bus Timing Diagram

6.11 Typical Characteristics



NOTE: On the rising edge of each clock period, the CML driver outputs a low stop bit, high start bit, and 33 DC-scrambled data bits.

Figure 10. Serializer CML Driver Output With 78-MHZ TX Pixel Clock

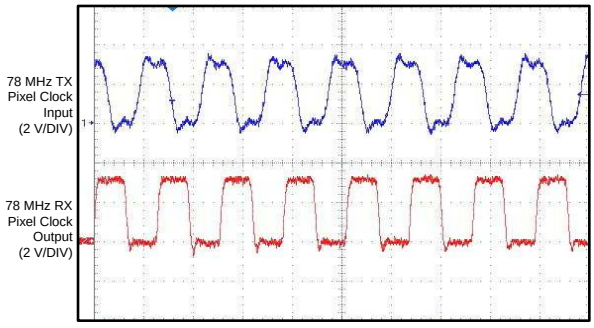


Figure 11. Comparison of Deserializer LVCMOS RX PCLK Output Locked to a 78-MHz TX PCLK

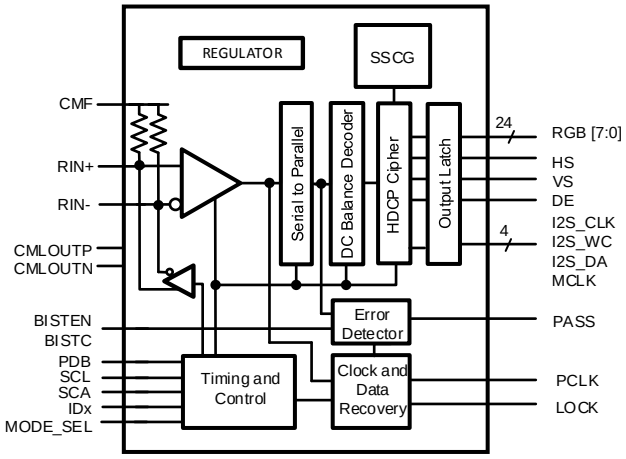
7 Detailed Description

7.1 Overview

The DS90UH926Q-Q1 deserializer receives a 35 bits symbol over a single serial FPD-Link III pair operating up to a 2.975 Gbps application payload. The serial stream contains an embedded clock, video control signals and the DC-balanced video data and audio data which enhance signal quality to support AC coupling.

The DS90UH926Q-Q1 deserializer attains lock to a data stream without the use of a separate reference clock source, which greatly simplifies system complexity and overall cost. The deserializer also synchronizes to the serializer regardless of the data pattern, delivering true automatic *plug and lock* performance. It can lock to the incoming serial stream without the need of special training patterns or sync characters. The deserializer recovers the clock and data by extracting the embedded clock information, validating then deserializing the incoming data stream. It also applies decryption through a High-Bandwidth Digital Content Protection (HDCP) Cipher to this video and audio data stream following reception of the data from the FPD-Link III decoder. The decrypted parallel LVCMOS video bus is provided to the display. The deserializer is intended for use with the DS90UH925Q serializer, but is also backward-compatible with DS90UR905Q or DS90UR907Q FPD-Link II serializer.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 High-Speed Forward Channel Data Transfer

The high-speed forward channel (HS_FC) is composed of 35 bits of data containing RGB data, sync signals, HDCP, I2C, and I2S audio transmitted from Serializer to Deserializer. Figure 12 illustrates the serial stream per PCLK cycle. This data payload is optimized for signal transmission over an AC-coupled link. Data is randomized, balanced and scrambled.

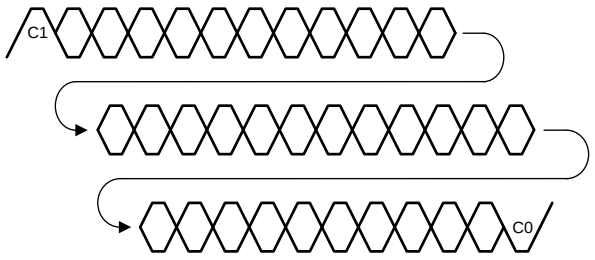


Figure 12. FPD-Link III Serial Stream

Feature Description (continued)

The device supports clocks in the range of 5 MHz to 85 MHz. The application payload rate is 2.975-Gbps maximum (175 Mbps minimum) with the actual line rate of 2.975 Gbps maximum and 525 Mbps minimum.

7.3.2 Low-Speed Back Channel Data Transfer

The low-speed backward channel (LS_BC) of the DS90UH926Q-Q1 provides bidirectional communication between the display and host processor. The information is carried back from the Deserializer to the Serializer per serial symbol. The back channel control data is transferred over the single serial link along with the high-speed forward data, DC balance coding, and embedded clock information. This architecture provides a backward path across the serial link together with a high-speed forward channel. The back channel contains the I2C, HDCP, CRC and 4 bits of standard GPIO information with 10-Mbps line rate.

7.3.3 Backward Compatible Mode

The DS90UH926Q-Q1 is also backward-compatible to DS90UR905Q and DS90UR907Q FPD Link II serializers with 15- to 65-MHz pixel clock frequencies supported. It receives 28 bits of data over a single serial FPD-Link II pair operating at the line rate of 420 Mbps to 1.82 Gbps. This backward-compatible mode is provided through the MODE_SEL pin (Table 9) or the configuration register (Table 11). When backward-compatible mode = *ON*, set LFMODE = 0.

7.3.4 Input Equalization Gain

FPD-Link III input adaptive equalizer provides compensation for transmission medium losses and reduces the medium-induced deterministic jitter. It equalizes up to 10 meter STP cables with 3 connection breaks at maximum serialized stream payload rate of 2.975 Gbps.

7.3.5 Common-Mode Filter Pin (CMF)

The deserializer provides access to the center tap of the internal termination. A capacitor must be placed on this pin for additional common-mode filtering of the differential pair. This can be useful in high noise environments for additional noise rejection capability. A 0.1-μF capacitor has to be connected to this pin to Ground.

7.3.6 Video Control Signal Filter

When operating the devices in Normal Mode, the Video Control Signals (DE, HS, VS) have the following restrictions:

- Normal Mode with Control Signal Filter Enabled: DE and HS — Only 2 transitions per 130 clock cycles are transmitted, the transition pulse must be 3 PCLK or longer.
- Normal Mode with Control Signal Filter Disabled: DE and HS — Only 2 transitions per 130 clock cycles are transmitted, no restriction on minimum transition pulse.
- VS — Only 1 transition per 130 clock cycles are transmitted, minimum pulse width is 130 clock cycles.

Video Control Signals are defined as low-frequency signals with limited transitions. Glitches of a control signal can cause a visual display error. This feature allows for the chipset to validate and filter out any high-frequency noise on the control signals. See Figure 13.

Feature Description (continued)

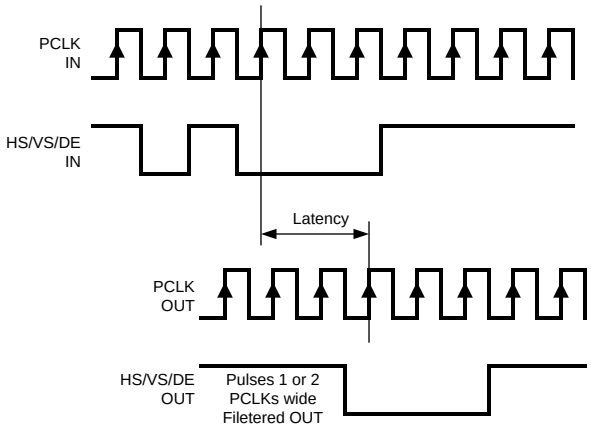


Figure 13. Video Control Signal Filter Waveform

7.3.7 EMI Reduction Features

7.3.7.1 Spread Spectrum Clock Generation (SSCG)

The DS90UH926Q-Q1 provides an internally-generated spread spectrum clock (SSCG) to modulate its outputs. Both clock and data outputs are modulated. This will aid to lower system EMI. Output SSCG deviations to ±2.5% (5% total) at up to 100-kHz modulations are available. This feature may be controlled by register. See Table 1, Table 2 and Table 11. Do not enable the SSCG feature if the source PCLK into the SER has a clock with spread spectrum already.

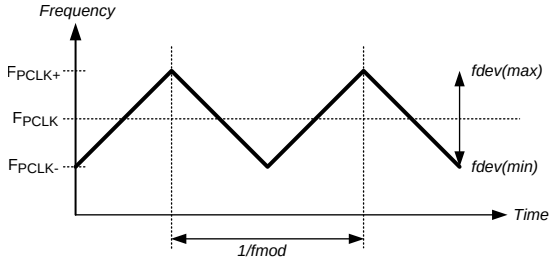


Figure 14. SSCG Waveform

Table 1. SSCG Configuration
LFMODE = L (15 to 85 MHz)

SSCG CONFIGURATION (0x2C) LFMODE = L (15 to 85 MHz)			SPREAD SPECTRUM OUTPUT	
SSC[2]	SSC[1]	SSC[0]	Fdev (%)	Fmod (kHz)
L	L	L	±0.9	PCLK / 2168
L	L	H	±1.2	
L	H	L	±1.9	
L	H	H	±2.5	
H	L	L	±0.7	PCLK / 1300
H	L	H	±1.3	
H	H	L	±2.0	
H	H	H	±2.5	

Table 2. SSCG Configuration
LFMODE = H (5 to < 15 MHz)

SSCG CONFIGURATION (0x2C) LFMODE = H (5 to <15 MHz)			SPREAD SPECTRUM OUTPUT	
SSC[2]	SSC[1]	SSC[0]	Fdev (%)	Fmod (kHz)
L	L	L	±0.5	PCLK / 628
L	L	H	±1.3	
L	H	L	±1.8	
L	H	H	±2.5	
H	L	L	±0.7	PCLK / 388
H	L	H	±1.2	
H	H	L	±2	
H	H	H	±2.5	

7.3.8 Enhanced Progressive Turnon (EPTO)

The deserializer LVCMOS parallel outputs timing are delayed. Groups of 8-bit R, G and B outputs switch in a different time. This minimizes the number of outputs switching simultaneously and helps to reduce supply noise. In addition it spreads the noise spectrum out reducing overall EMI.

7.3.9 LVCMOS VDDIO Option

The deserializer parallel bus can operate with 1.8 V or 3.3 V levels (VDDIO) for target (Display) compatibility. The 1.8 V levels will offer a lower noise (EMI) and also a system power savings.

7.3.10 Power Down (PDB)

The Serializer has a PDB input pin to ENABLE or POWER DOWN the device. This pin can be controlled by the host or through the V_{DDIO}, where V_{DDIO} = 3 to 3.6 V or V_{DD33}. To save power disable the link when the display is not needed (PDB = LOW). When the pin is driven by the host, make sure to release it after V_{DD33} and V_{DDIO} have reached final levels; no external components are required. In the case of driven by the V_{DDIO} = 3 to 3.6 V or V_{DD33} directly, a 10 kΩ resistor to the V_{DDIO} = 3 to 3.6 V or V_{DD33} , and a > 10 µF capacitor to the ground are required (See Figure 24).

7.3.11 Stop Stream Sleep

The deserializer enters a low power SLEEP state when the input serial stream is stopped. A STOP condition is detected when the embedded clock bits are not present. When the serial stream starts again, the deserializer will then lock to the incoming signal and recover the data.

NOTE
In STOP STREAM SLEEP, the Serial Control Bus Registers values are retained.

7.3.12 Serial Link Fault Detect

The serial link fault detection is able to detect any of following 7 conditions

1. cable open
2. + to - short
3. + short to GND
4. - short to GND
5. + short to battery
6. - short to battery
7. Cable is linked incorrectly

If any one of the fault conditions occurs, The Link Detect Status is 0 (cable is not detected) on the Serial Control Bus Register bit 0 of address 0x1C Table 11. The link errors can be monitored though Link Error Count of the Serial Control Bus Register bit [4:0] of address 0x41 Table 11.

7.3.13 Oscillator Output

The deserializer provides an optional PCLK output when the input clock (serial stream) has been lost. This is based on an internal oscillator. The frequency of the oscillator may be selected. This feature is controlled by register Address 0x02, bit 5 (OSC Clock Enable). See Table 11.

7.3.14 Pixel Clock Edge Select (RFB)

The RFB determines the edge that the data is strobed on. If RFB is High ('1'), output data is strobed on the Rising edge of the PCLK. If RFB is Low ('0'), data is strobed on the Falling edge of the PCLK. This allows for inter-operability with downstream devices. The deserializer output does not need to use the same edge as the Ser input. This feature may be controlled by register. See Table 11.

7.3.15 Built In Self Test (BIST)

An optional At-Speed, Built-In Self Test (BIST) feature supports the testing of the high speed serial link and the low- speed back channel. This is useful in the prototype stage, equipment production, in-system test and also for system diagnostics. The BIST is not available in backwards-compatible mode.

7.3.15.1 BIST Configuration and Status

The BIST mode is enabled at the deserializer by the Pin select (Pin 44 BISTEN and Pin 16 BISTC) or configuration register (Table 11) through the deserializer. When LFMODE = 0, the pin based configuration defaults to external PCLK or 33 MHz internal Oscillator clock (OSC) frequency. In the absence of PCLK, the user can select the desired OSC frequency (default 33 MHz or 25 MHz) through the register bit. When LFMODE = 1, the pin based configuration defaults to external PCLK or 12.5 MHz MHz internal Oscillator clock (OSC) frequency.

When BISTEN of the deserializer is high, the BIST mode enable information is sent to the serializer through the Back Channel. The serializer outputs a test pattern and drives the link at speed. The deserializer detects the test pattern and monitors it for errors. The PASS output pin toggles to flag any payloads that are received with 1- to 35-bit errors.

The BIST status is monitored real time on PASS pin. The result of the test is held on the PASS output until reset (new BIST test or Power Down). A High on PASS indicates NO ERRORS were detected. A Low on PASS indicates one or more errors were detected. The duration of the test is controlled by the pulse width applied to the deserializer BISTEN pin. This BIST feature also contains a Link Error Count and a Lock Status. If the connection of the serial link is broken, then the link error count is shown in the register. When the PLL of the deserializer is locked or unlocked, the lock status can be read in the register. See Table 11.

7.3.15.1.1 Sample BIST Sequence

See Figure 15 for the BIST mode flow diagram.

1. For the DS90UH925Q-Q1 and DS90UH926Q-Q1 FPD-Link III chipset, BIST Mode is enabled through the BISTEN pin of DS90UH926Q-Q1 FPD-Link III deserializer. The desired clock source is selected through BISTC pin.
2. The DS90UH925Q-Q1 serializer is woken up through the back channel if it is not already on. The all zero pattern on the data pins is sent through the FPD-Link III to the deserializer. Once the serializer and the deserializer are in BIST mode and the deserializer acquires Lock, the PASS pin of the deserializer goes high and BIST starts checking the data stream. If an error in the payload (1 to 35) is detected, the PASS pin will switch low for one half of the clock period. During the BIST test, the PASS output can be monitored and counted to determine the payload error rate.
3. To Stop the BIST mode, the deserializer BISTEN pin is set Low. The deserializer stops checking the data. The final test result is held on the PASS pin. If the test ran error free, the PASS output will be High. If there was one or more errors detected, the PASS output will be Low. The PASS output state is held until a new BIST is run, the device is RESET, or Powered Down. The BIST duration is user controlled by the duration of the BISTEN signal.
4. The Link returns to normal operation after the deserializer BISTEN pin is low. Figure 16 shows the waveform diagram of a typical BIST test for two cases. Case 1 is error free, and Case 2 shows one with multiple errors. In most cases it is difficult to generate errors due to the robustness of the link (differential data transmission etc.), thus they may be introduced by greatly extending the cable length, faulting the interconnect, reducing

signal condition enhancements (Rx Equalization).

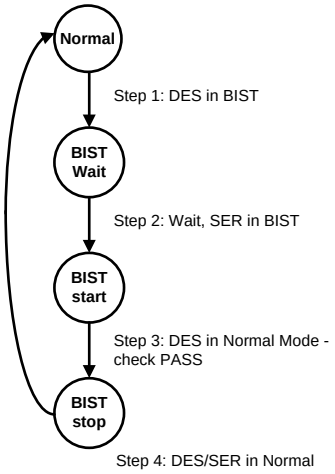


Figure 15. BIST Mode Flow Diagram

7.3.15.2 Forward-Channel and Back-Channel Error Checking

While in BIST mode, the serializer stops sampling RGB input pins and switches over to an internal all-zero pattern. The internal all-zeroes pattern goes through scrambler, dc-balancing etc. and goes over the serial link to the deserializer. The deserializer on locking to the serial stream compares the recovered serial stream with all-zeroes and records any errors in status registers and dynamically indicates the status on PASS pin. The deserializer then outputs a SSO pattern on the RGB output pins.

The back-channel data is checked for CRC errors once the serializer locks onto back-channel serial stream as indicated by link detect status (register bit 0x0C[0]). The CRC errors are recorded in an 8-bit register. The register is cleared when the serializer enters the BIST mode. As soon as the serializer exits BIST mode, the functional mode CRC register starts recording the CRC errors. The BIST mode CRC error register is active in BIST mode only and keeps the record of last BIST run until it clears or enters BIST mode again.

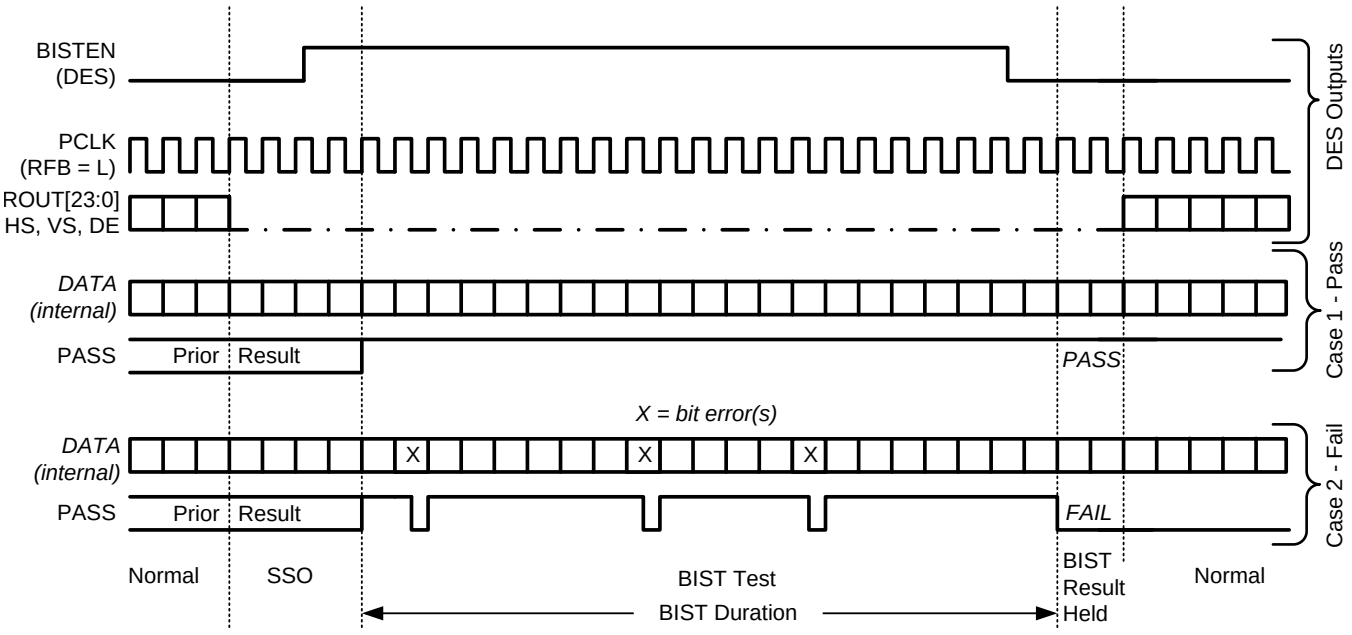


Figure 16. BIST Waveforms

7.3.16 Image Enhancement Features

Several image enhancement features are provided. White balance LUTs allow the user to define and target the color temperature of the display. Adaptive Hi-FRC dithering enables the presentation of “true-color” images on an 18–bit color display.

7.3.16.1 White Balance

The White Balance feature enables similar display appearance when using LCDs from different vendors. It compensates for native color temperature of the display, and adjusts relative intensities of R, G, B to maintain specified color temperature. Programmable control registers are used to define the contents of three LUTs (8-bit color value for Red, Green and Blue) for the white balance feature. The LUTs map input RGB values to new output RGB values. There are three LUTs, one LUT for each color. Each LUT contains 256 entries, 8 bits per entry with a total size of 6144 bits (3 x 256 x 8). All entries are readable and writable. Calibrated values are loaded into registers through the I2C interface (deserializer is a slave device). This feature may also be applied to lower color depth applications such as 18–bit (666) and 16–bit (565). White balance is enabled and configured through that serial control bus register.

7.3.16.1.1 LUT Contents

The user must define and load the contents of the LUT for each color (R,G,B). Regardless of the color depth being driven (888, 666, 656), the user must always provide contents for 3 complete LUTs - 256 colors x 8 bits x 3 tables. Unused bits - LSBs -shall be set to 0 by the user.

When 24-bit (888) input data is being driven to a 24-bit display, each LUT (R, G and B) must contain 256 unique 8-bit entries. The 8-bit white balanced data is then available at the output of the DS90UH926Q-Q1 deserializer, and driven to the display.

When 18-bit (666) input data is being driven to an 18-bit display, the white balance feature may be used in one of two ways. First, simply load each LUT with 256, 8-bit entries. Each 8-bit entry is a 6-bit value (6 MSBs) with the 2 LSBs set to 00. Thus as total of 64 unique 6-bit white balance output values are available for each color (R, G and B). The 6-bit white balanced data is available at the output of the DS90UH926Q-Q1 deserializer, and driven directly to the display.

Alternatively, with 6-bit input data the user may choose to load complete 8-bit values into each LUT. This mode of operation provides the user with finer resolution at the LUT output to more closely achieve the desired white point of the calibrated display. Although 8-bit data is loaded, only 64 unique 8-bit white balance output values are available for each color (R, G and B). The result is 8-bit white balanced data. Before driving to the output of the deserializer, the 8-bit data must be reduced to 6-bit with an FRC dithering function. To operate in this mode, the user must configure the DS90UH926Q-Q1 to enable the FRC2 function.

Examples of the three types of LUT configurations described are shown in Figure 17

7.3.16.1.2 Enabling White Balance

The user must load all 3 LUTs prior to enabling the white balance feature. The following sequence must be followed by the user.

To initialize white balance after power-on (Table 3):

1. Load contents of all 3 LUTs . This requires a sequential loading of LUTs - first RED, second GREEN, third BLUE. 256, 8-bit entries must be loaded to each LUT. Page registers must be set to select each LUT.
2. Enable white balance.

By default, the LUT data may not be reloaded after initialization at power-on.

An option does exist to allow LUT reloading after power-on and initial LUT loading (as described above). This option may only be used after enabling the white balance reload feature through the associated serial control bus register. In this mode the LUTs may be reloaded by the master controller through the I2C. This provides the user with the flexibility to refresh LUTs periodically , or upon system requirements to change to a new set of LUT values. The host controller loads the updated LUT values through the serial bus interface. There is no need to disable the white balance feature while reloading the LUT data. Refreshing the white balance to the new set of LUT data will be seamless - no interruption of displayed data.

It is important to note that initial loading of LUT values requires that all three LUTs be loaded sequentially. When reloading, partial LUT updates may be made.

8-bit in / 8 bit out

Gray level Entry	Data Out (8-bits)
0	00000000b
1	00000001b
2	00000011b
3	00000011b
4	00000110b
5	00000110b
6	00000111b
7	00000111b
8	00001000b
9	00001010b
10	00001001b
11	00001011b
⋮	⋮
248	11111010b
249	11111010b
250	11111011b
251	11111011b
252	11111110b
253	11111101b
254	11111101b
255	11111111b

6-bit in / 6 bit out

Gray level Entry	Data Out (8-bits)
0	00000**00**b
1	N/A
2	N/A
3	N/A
4	00001**00**b
5	N/A
6	N/A
7	N/A
8	00010**00**b
9	N/A
10	N/A
11	N/A
⋮	⋮
248	11110**00**b
249	N/A
250	N/A
251	N/A
252	11111**00**b
253	N/A
254	N/A
255	N/A

6-bit in / 8 bit out

Gray level Entry	Data Out (8-bits)
0	00000001b
1	N/A
2	N/A
3	N/A
4	00000110b
5	N/A
6	N/A
7	N/A
8	00001011b
9	N/A
10	N/A
11	N/A
⋮	⋮
248	11111010b
249	N/A
250	N/A
251	N/A
252	11111111b
253	N/A
254	N/A
255	N/A

Figure 17. White Balance LUT Configurations

Table 3. White Balance Register Table

PAGE	ADD (dec)	ADD (hex)	REGISTER NAME	BITS	ACCESS	DEFAULT (hex)	FUNCTION	DESCRIPTION
0	42	0x2A	White Balance Control	7:6	RW	0x00	Page Setting	00: Configuration Registers 01: Red LUT 10: Green LUT 11: Blue LUT
				5	RW		White Balance Enable	0: White Balance Disable 1: White Balance Enable
				4	RW			0: Reload Disable 1: Reload Enable
				3:0				***Reserved***
1	0 – 255	00 – FF	White Balance Red LUT	FF:0	RW	N/A	Red LUT	256 8–bit entries to be applied to the Red subpixel data
2	0 – 255	00 – FF	White Balance Green LUT	FF:0	RW	N/A	Green LUT	256 8–bit entries to be applied to the Green subpixel data
3	0 – 255	00 – FF	White Balance Blue LUT	FF:0	RW	N/A	Blue LUT	256 8–bit entries to be applied to the Blue subpixel data

7.3.16.2 Adaptive HI-FRC Dithering

The Adaptive FRC Dithering Feature delivers product-differentiating image quality. It reduces 24-bit RGB (8 bits per subpixel) to 18-bit RGB (6 bits per sub-pixel), smoothing color gradients, and allowing the flexibility to use lower cost 18-bit displays. FRC (Frame Rate Control) dithering is a method to emulate “missing” colors on a lower color depth LCD display by changing the pixel color slightly with every frame. FRC is achieved by controlling on and off pixels over multiple frames (Temporal). Static dithering regulates the number of on and off pixels in a small defined pixel group (Spatial). The FRC module includes both Temporal and Spatial methods and also Hi-FRC. Conventional FRC can display only 16,194,277 colors with 6-bit RGB source. “Hi-FRC” enables full (16,777,216) color on an 18-bit LCD panel. The “adaptive” FRC module also includes input pixel detection to apply specific Spatial dithering methods for smoother gray level transitions. When enabled, the lower LSBs of each RGB output are not active; only 18 bit data (6 bits per R,G and B) are driven to the display. This feature is enabled through the serial control bus register.

Two FRC functional blocks are available, and may be independently enabled. FRC1 precedes the white balance LUT, and is intended to be used when 24-bit data is being driven to an 18-bit display with a white balance LUT that is calibrated for an 18-bit data source. The second FRC block, FRC2, follows the white balance block and is intended to be used when fine adjustment of color temperature is required on an 18-bit color display, or when a 24-bit source drives an 18-bit display with a white balance LUT calibrated for 24-bit source data.

For proper operation of the FRC dithering feature, the user must provide a description of the display timing control signals. The timing mode, “sync mode” (HS, VS) or “DE only” must be specified, along with the active polarity of the timing control signals. All this information is entered to DS90UH926Q-Q1 control registers through the serial bus interface.

Adaptive Hi-FRC dithering consists of several components. Initially, the incoming 8-bit data is expanded to 9-bit data. This allows the effective dithered result to support a total of 16.7 million colors. The incoming 9-bit data is evaluated, and one of four possible algorithms is selected. The majority of incoming data sequences are supported by the default dithering algorithm. Certain incoming data patterns (black/white pixel, full on/off sub-pixel) require special algorithms designed to eliminate visual artifacts associated with these specific gray level transitions. Three algorithms are defined to support these critical transitions.

An example of the default dithering algorithm is illustrated in Figure 18. The 1 or 0 value shown in the table describes whether the 6-bit value is increased by 1 (1) or left unchanged (0). In this case, the 3 truncated LSBs are 001.

F0L0	Frame = 0, Line = 0
PD1	Pixel Data one
Cell Value 010	R[7:2]+0, G[7:2]+1, B[7:2]+0
LSB=001	three lsb of 9 bit data (8 to 9 for Hi-Frc)

Pixel Index	PD1	PD2	PD3	PD4	PD5	PD6	PD7	PD8	
LSB = 001									
F0L0	010	000	000	000	000	000	010	000	R = 4/32 G = 4/32 B = 4/32
F0L1	101	000	000	000	101	000	000	000	
F0L2	000	000	010	000	010	000	000	000	
F0L3	000	000	101	000	000	000	101	000	
F1L0	000	000	000	000	000	000	000	000	R = 4/32 G = 4/32 B = 4/32
F1L1	000	111	000	000	000	111	000	000	
F1L2	000	000	000	000	000	000	000	000	
F1L3	000	000	000	111	000	000	000	111	
F2L0	000	000	010	000	010	000	000	000	R = 4/32 G = 4/32 B = 4/32
F2L1	000	000	101	000	000	000	101	000	
F2L2	010	000	000	000	000	000	010	000	
F2L3	101	000	000	000	101	000	000	000	
F3L0	000	000	000	000	000	000	000	000	R = 4/32 G = 4/32 B = 4/32
F3L1	000	000	000	111	000	000	000	111	
F3L2	000	000	000	000	000	000	000	000	
F3L3	000	111	000	000	000	111	000	000	

Figure 18. Default FRC Algorithm

Table 4. Recommended FRC Settings

SOURCE	WHITE BALANCE LUT	DISPLAY	FRC1	FRC2
24–bit	24–bit	24–bit	Disabled	Disabled
24–bit	24–bit	18–bit	Disabled	Enabled
24–bit	18–bit	18–bit	Enabled	Disabled
18–bit	24–bit	24–bit	Disabled	Disabled
18–bit	24–bit	18–bit	Disabled	Enabled
18–bit	18–bit	18–bit	Disabled	Disabled

7.3.17 Internal Pattern Generation

The DS90UH926Q-Q1 serializer supports the internal pattern generation feature. It allows basic testing and debugging of an integrated panel. The test patterns are simple and repetitive and allow for a quick visual verification of panel operation. As long as the device is not in power down mode, the test pattern will be displayed even if no parallel input is applied. If no PCLK is received, the test pattern can be configured to use a programmed oscillator frequency. For detailed information, refer to *AN-2198 Exploring the Internal Test Pattern Generation Feature of 720p FPD-Link III Devices* (SNLA132).

7.3.18 I2S Receiving

In normal 24-bit RGB operation mode, the DS90UH926Q-Q1 provides up to 3-bit of I2S. They are I2S_CLK, I2S_WC and I2S_DA, as well as the Master I2S Clock (MCLK). The audio is received through the forward video frame, or can be configured to receive during video blanking periods. A jitter cleaning feature reduces I2S_CLK output jitter to +/- 2ns. The encrypted and packetized audio information is received during the video blanking periods along with specific information about the clock frequency. The bit rates of any I2S input bits must maintain one fourth of the PCLK rate. The audio decryption is supported per HDCP v1.3.

7.3.18.1 I2S Jitter Cleaning

In 18-bit RGB operation mode, the secondary I2S data (I2S_DB) can be used as the additional I2S audio channel in additional to the 3–bit of I2S. The I2S_DB is synchronized to the I2S_CLK. To enable this synchronization feature on this bit, set the MODE_SEL (Table 9) or program through the register bit ()

7.3.18.2 Secondary I2S Channel

In 18-bit RGB operation mode, the secondary I2S data (I2S_DB) can be used as the additional I2S audio channel in additional to the 3–bit of I2S. The I2S_DB is synchronized to the I2S_CLK. To enable this synchronization feature on this bit, set the MODE_SEL (Table 9) or program through the register bit (Table 11).

7.3.18.2.1 MCLK

The deserializer has an I2S Master Clock Output. It supports x1, x2, or x4 of I2S CLK Frequency. When the I2S PLL is disabled, the MCLK output is off. Table 5 below covers the range of I2S sample rates and MCLK frequencies. By default, all the MCLK output frequencies are x2 of the I2S CLK frequencies. The MCLK frequencies can also be enabled through the register bit [7:4] (I2S MCLK Output) of 0x3A shown in Table 11. To select desired MCLK frequency, write bit 7 (0x3A) = 1, then write to bit [6:4] accordingly.

Table 5. Audio Interface Frequencies

SAMPLE RATE (kHz)	I2S DATA WORD SIZE (BITS)	I2S CLK (MHz)	MCLK OUTPUT (MHz)	REGISTER 0x3A[6:4]'b
32	16	1.024	I2S_CLK x1	000
			I2S_CLK x2	001
			I2S_CLK x4	010
44.1		1.4112	I2S_CLK x1	000
			I2S_CLK x2	001
			I2S_CLK x4	010
48		1.536	I2S_CLK x1	000
			I2S_CLK x2	001
			I2S_CLK x4	010
96		3.072	I2S_CLK x1	001
			I2S_CLK x2	010
			I2S_CLK x4	011
192		6.144	I2S_CLK x1	010
			I2S_CLK x2	011
			I2S_CLK x4	100
32	24	1.536	I2S_CLK x1	000
			I2S_CLK x2	001
			I2S_CLK x4	010
44.1		2.117	I2S_CLK x1	001
			I2S_CLK x2	010
			I2S_CLK x4	011
48		2.304	I2S_CLK x1	001
			I2S_CLK x2	010
			I2S_CLK x4	011
96		4.608	I2S_CLK x1	010
			I2S_CLK x2	011
			I2S_CLK x4	100
192		9.216	I2S_CLK x1	011
			I2S_CLK x2	100
			I2S_CLK x4	101
32	32	2.048	I2S_CLK x1	001
			I2S_CLK x2	010
			I2S_CLK x4	011
44.1		2.8224	I2S_CLK x1	001
			I2S_CLK x2	010
			I2S_CLK x4	011
48		3.072	I2S_CLK x1	001
			I2S_CLK x2	010
			I2S_CLK x4	011
96		6.144	I2S_CLK x1	010
			I2S_CLK x2	011
			I2S_CLK x4	100
192		12.288	I2S_CLK x1	011
			I2S_CLK x2	100
			I2S_CLK x4	110

7.3.19 Interrupt Pin: Functional Description and Usage (INTB)

1. On DS90UH925Q-Q1, set register 0xC6[5] = 1 and 0xC6[0] = 1
2. DS90UH926Q-Q1 deserializer INTB_IN (pin 16) is set LOW by some downstream device.
3. DS90UH925Q-Q1 serializer pulls INTB (pin 31) LOW. The signal is active low, so a LOW indicates an interrupt condition.
4. External controller detects INTB = LOW; to determine interrupt source, read HDCP_ISR register .
5. A read to HDCP_ISR will clear the interrupt at the DS90UH925, releasing INTB.
6. The external controller typically must then access the remote device to determine downstream interrupt source and clear the interrupt driving INTB_IN. This would be when the downstream device releases the INTB_IN (pin 16) on the DS90UH926Q-Q1. The system is now ready to return to step (1) at next falling edge of INTB_IN.

7.3.20 GPIO[3:0] and GPO_REG[8:4]

In 18-bit RGB operation mode, the optional R[1:0] and G[1:0] of the DS90UH926Q-Q1 can be used as the general purpose IOs GPIO[3:0] in either forward channel (Outputs) or back channel (Inputs) application.

7.3.20.1 GPIO[3:0] Enable Sequence

See Table 6 for the GPIO enable sequencing.

1. Enable the 18-bit mode either through the configuration register bit Table 11 on DS90UH925Q-Q1 only. DS90UH926Q-Q1 is automatically configured as in the 18-bit mode.
2. To enable GPIO3 forward channel, write 0x03 to address 0x0F on DS90UH925Q-Q1, then write 0x05 to address 0x1F on DS90UH926Q-Q1.

Table 6. GPIO Enable Sequencing Table

NO.	DESCRIPTION	DEVICE	FORWARD CHANNEL	BACK CHANNEL
1	Enable 18-bit mode	DS90UH925Q-Q1	0x12 = 0x04	0x12 = 0x04
		DS90UH926Q-Q1	Auto Load from DS90UH925Q-Q1	Auto Load from DS90UH925Q-Q1
2	GPIO3	DS90UH925Q-Q1	0x0F = 0x03	0x0F = 0x05
		DS90UH926Q-Q1	0x1F = 0x05	0x1F = 0x03
3	GPIO2	DS90UH925Q-Q1	0x0E = 0x30	0x0E = 0x50
		DS90UH926Q-Q1	0x1E = 0x50	0x1E = 0x30
4	GPIO1	DS90UH925Q-Q1	0x0E = 0x03	0x0E = 0x05
		DS90UH926Q-Q1	0x1E = 0x05	0x0E = 0x05
5	GPIO0	DS90UH925Q-Q1	0x0D = 0x93	0x0D = 0x95
		DS90UH926Q-Q1	0x1D = 0x95	0x1D = 0x93

7.3.20.2 GPO_REG[8:4] Enable Sequence

GPO_REG[8:4] are the outputs only pins. They must be programmed through the local register bits. See Table 11 for the GPO_REG enable sequencing.

1. Enable the 18-bit mode either through the configuration register bit Table 11 on DS90UH925Q-Q1 only. DS90UH926Q-Q1 is automatically configured as in the 18-bit mode.
2. To enable GPO_REG8 outputs a 1, write 0x90 to address 0x11 on DS90UH925Q.

Table 7. GPO_REG Enable Sequencing Table

NO.	DESCRIPTION	DEVICE	LOCAL ACCESS	LOCAL OUTPUT VALUE
1	Enable 18-bit mode	DS90UH926Q-Q1	0x12 = 0x04 (on DS90UH925Q-Q1)	
2	GPO_REG8	DS90UH926Q-Q1	0x21 = 0x90	1
			0x21 = 0x10	0
3	GPO_REG7	DS90UH926Q-Q1	0x21 = 0x09	1
			0x21 = 0x01	0

Table 7. GPO_REG Enable Sequencing Table (continued)

NO.	DESCRIPTION	DEVICE	LOCAL ACCESS	LOCAL OUTPUT VALUE
4	GPO_REG6	DS90UH926Q-Q1	0x20 = 0x90	1
			0x20 = 0x10	0
5	GPO_REG5	DS90UH926Q-Q1	0x20 = 0x09	1
			0x20 = 0x01	0
6	GPO_REG4	DS90UH926Q-Q1	0x1F = 0x90	1
			0x1F = 0x10	0

7.4 Device Functional Modes

7.4.1 Clock-Data Recovery Status Flag (LOCK), Output Enable (OEN), and Output State Select (OSS_SEL)

When PDB is driven HIGH, the CDR PLL begins locking to the serial input and LOCK is TRI-STATE or LOW (depending on the value of the OEN setting). After the DS90UH926Q-Q1 completes its lock sequence to the input serial data, the LOCK output is driven HIGH, indicating valid data and clock recovered from the serial input is available on the parallel bus and PCLK outputs. The State of the outputs are based on the OEN and OSS_SEL setting (Table 8) or register bit (Table 11). See Figure 7.

Table 8. Output States

INPUTS				OUTPUTS			
Serial input	PDB	OEN	OSS_SEL	Lock	Pass	Data, GPIO, I2S	CLK
X	0	X	X	Z	Z	Z	Z
X	1	0	0	L or H	L	L	L
X	1	0	1	L or H	Z	Z	Z
Static	1	1	0	L	L	L	L/OSC (Register bit enable)
Static	1	1	1	L	Previous Status	L	L
Active	1	1	0	H	L	L	L
Active	1	1	1	H	Valid	Valid	Valid

7.4.2 Low Frequency Optimization (LFMODE)

The LFMODE is set through a register (Table 11) or MODE_SEL Pin 24 (Table 9). It controls the operating frequency of the deserializer. If LFMODE is Low (default), the PCLK frequency is between 15 MHz and 85 MHz. If LFMODE is High, the PCLK frequency is between 5 MHz and <15 MHz. Please note: when the device LFMODE is changed, a PDB reset is required.

7.4.3 Configuration Select (MODE_SEL)

Configuration of the device may be done through the MODE_SEL input pin, or through the configuration register bit. A pullup resistor and a pulldown resistor of suggested values may be used to set the voltage ratio of the MODE_SEL input (V_{R4}) and V_{DD33} to select one of the other 10 possible selected modes. See Figure 19 and Table 9.

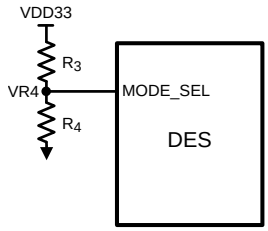


Figure 19. MODE_SEL Connection Diagram

Table 9. Configuration Select (MODE_SEL)

NO.	IDEAL RATIO V_{R4}/V_{DD33}	IDEAL V_{R4} (V)	SUGGESTED RESISTOR R3 kΩ (1% tol)	SUGGESTED RESISTOR R4 kΩ (1% tol)	LFMODE(1)	REPEATER(2)	BACKWARD COMPATIBLE(3)	I2S CHANNEL B (18–bit MODE)(4)
1	0	0	Open	40.2	L	L	L	L
2	0.123	0.407	115	16.2	L	L	L	H
3	0.167	0.552	121	24.3	L	H	L	L
4	0.227	0.748	162	47.5	L	H	L	H
5	0.291	0.960	137	56.2	H	L	L	L
6	0.366	1.209	107	61.9	H	L	L	H
7	0.458	1.510	113	95.3	H	H	L	L
8	0.542	1.790	95.3	113	H	H	L	H
9	0.611	2.016	73.2	115	L	L	H	L

(1) LFMODE:
L = frequency range is 15 MHz to 85 MHz (Default)
H = frequency range is 5 to < 15 MHz
(2) Repeater:
L = Repeater mode is *OFF* (Default)
H = Repeater mode is *ON*
(3) Backward Compatible:
L = Backward Compatible mode is *OFF* (Default)
H = Backward Compatible mode is *ON*; SER = DS90UR905Q or DS90UR907Q
– frequency range = 15 to 65 MHz, set LFMODE = L
(4) I2S Channel B:
L = I2S Channel B mode is *OFF*, normal 24-bit RGB Mode (Default)
H = I2S Channel B mode is *ON*, 18-bit RGB Mode with I2S_DB Enabled. Note: use of GPIO(s) on unused inputs must be enabled by register.

7.4.4 HDCP Repeater

When DS90UH925Q-Q1 and DS90UH926Q-Q1 are configured as the HDCP Repeater application, it provides a mechanism to extend HDCP transmission over multiple links to multiple display devices. This repeater application provides a mechanism to authenticate all HDCP Receivers in the system and distribute protected content to the HDCP Receivers using the encryption mechanisms provided in the HDCP specification.

In this document, the DS90UH925Q-Q1 is referred to as the HDCP Transmitter or transmit port (TX), and the DS90UH926Q-Q1 is referred to as the HDCP Receiver (RX). Figure 20 shows the maximum configuration supported for HDCP Repeater implementations using the DS90UH925Q-Q1 (TX) and DS90UH926Q-Q1 (RX). Two levels of HDCP Repeaters are supported with a maximum of three HDCP Transmitters per HDCP Receiver.

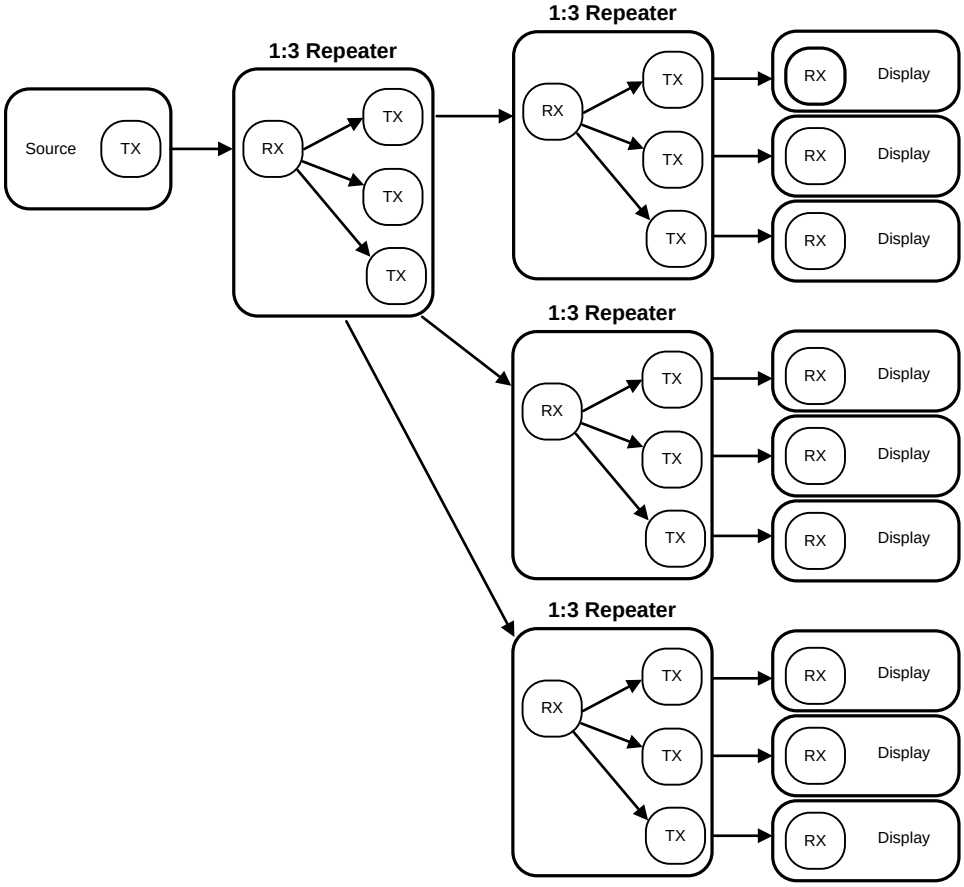


Figure 20. HDCP Maximum Repeater Application

To support HDCP Repeater operation, the DS90UH926Q-Q1 Deserializer includes the ability to control the downstream authentication process, assemble the KSV list for downstream HDCP Receivers, and pass the KSV list to the upstream HDCP Transmitter. An I2C master within the DS90UH926Q-Q1 communicates with the I2C slave within the DS90UH925Q-Q1 Serializer. The DS90UH925Q-Q1 Serializer handles authenticating with a downstream HDCP Receiver and makes status available through the I2C interface. The DS90UH926Q-Q1 monitors the transmit port status for each DS90UH925Q-Q1 and reads downstream KSV and KSV list values from the DS90UH925Q-Q1.

In addition to the I2C interface used to control the authentication process, the HDCP Repeater implementation includes two other interfaces. A parallel LVCMOS interface provides the unencrypted video data in 24-bit RGB format and includes the DE/VS/HS control signals. In addition to providing the RGB video data, the parallel LVCMOS interface communicates control information and packetized audio data during video blanking intervals. A separate I2S audio interface may optionally be used to send I2S audio data between the HDCP Receiver and HDCP Transmitter in place of using the packetized audio over the parallel LVCMOS interface. All audio and video data is decrypted at the output of the HDCP Receiver and is re-encrypted by the HDCP Transmitter.

Figure 21 provides more detailed block diagram of a 1:2 HDCP repeater configuration.

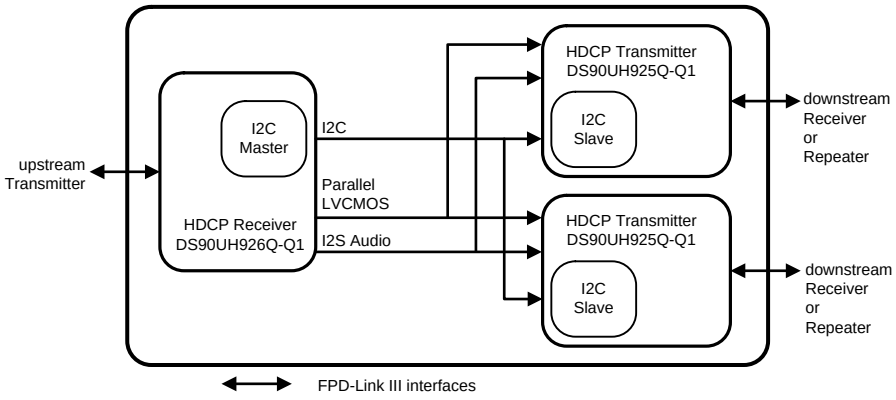


Figure 21. HDCP 1:2 Repeater Configuration

7.4.4.1 Repeater Connections

The HDCP Repeater requires the following connections between the HDCP Receiver and each HDCP Transmitter Figure 22.

1. Video Data – Connect PCLK, RGB and control signals (DE, VS, HS).
2. I2C – Connect SCL and SDA signals. Both signals should be pulled up to V_{DD33} with 4.7-kΩ resistors
3. Audio – Connect I2S_CLK, I2S_WC, and I2S_DA signals.
4. IDx pin – Each HDCP Transmitter and Receiver must have an unique I2C address.
5. MODE_SEL pin – All HDCP Transmitter and Receiver must be set into the Repeater Mode.
6. Interrupt pin– Connect DS90UH926Q-Q1 INTB_IN pin to DS90UH925Q-Q1 INTB pin. The signal must be pulled up to V_{DDIO}.

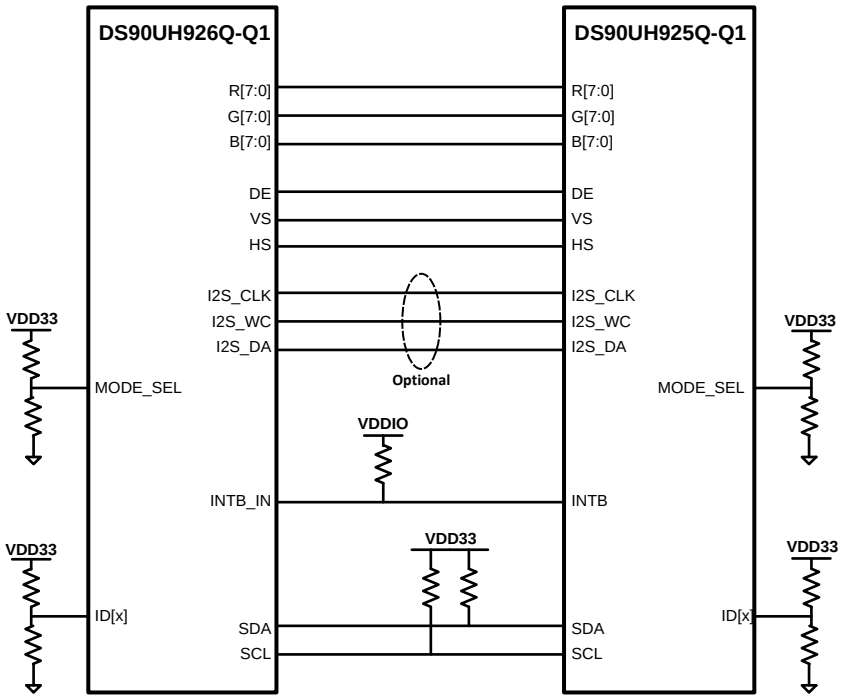


Figure 22. HDCP Repeater Connection Diagram

7.5 Programming

7.5.1 Serial Control Bus

The DS90UH926Q-Q1 is configured by the use of a serial control bus that is I2C protocol compatible. . Multiple deserializer devices may share the serial control bus since 16 device addresses are supported. Device address is set through the R_1 and R_2 values on IDx pin. See Figure 23.

The serial control bus consists of two signals and a configuration pin. The SCL is a Serial Bus Clock Input / Output. The SDA is the Serial Bus Data Input / Output signal. Both SCL and SDA signals require an external pull-up resistor to V_{DD33}. For most applications a 4.7 kΩ pull-up resistor to V_{DD33} may be used. The resistor value may be adjusted for capacitive loading and data rate requirements. The signals are either pulled High, or driven Low.

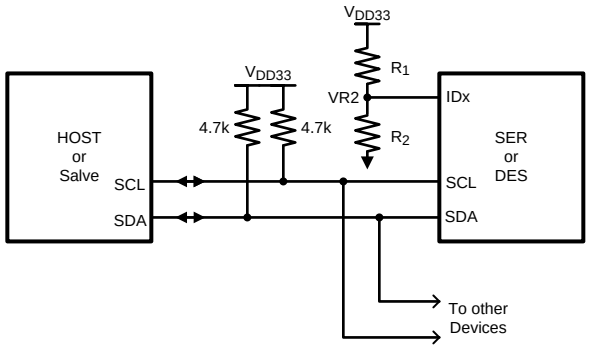


Figure 23. Serial Control Bus Connection

The configuration pin is the IDx pin. This pin sets one of 16 possible device addresses. A pull-up resistor and a pull-down resistor of suggested values may be used to set the voltage ratio of the IDx input (V_{R2}) and V_{DD33} to select one of the other 16 possible addresses. See Table 10

Table 10. Serial Control Bus Addresses for IDx

NO.	IDEAL RATIO V_{R2} / V_{DD33}	IDEAL V_{R2} (V)	SUGGESTED RESISTOR R1 kΩ (1% tol)	SUGGESTED RESISTOR R2 kΩ (1% tol)	ADDRESS 7'b	ADDRESS 8'b APPENDED
1	0	0	Open	40.2	0x2C	0x58
2	0.123	0.406	124	17.4	0x2D	0x5A
3	0.151	0.500	107	19.1	0x2E	0x5C
4	0.181	0.597	133	29.4	0x2F	0x5E
5	0.210	0.694	113	30.1	0x30	0x60
6	0.240	0.791	137	43.2	0x31	0x62
7	0.268	0.885	102	37.4	0x32	0x64
8	0.303	0.999	115	49.9	0x33	0x66
9	0.344	1.137	102	53.6	0x34	0x68
10	0.389	1.284	115	73.2	0x35	0x6A
11	0.430	1.418	115	86.6	0x36	0x6C
12	0.476	1.572	56.2	51.1	0x37	0x6E
13	0.523	1.725	93.1	102	0x38	0x70
14	0.565	1.863	82.5	107	0x39	0x72
15	0.611	2.016	73.2	115	0x3A	0x74
16	0.677	2.236	57.6	121	0x3B	0x76

7.6 Register Maps

Table 11. Serial Control Bus Registers

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Descriptions
0	0x00	I2C Device ID	7:1	RW		Device ID	7–bit address of Deserializer See Table 9
			0	RW		ID Setting	I2C ID Setting 1: Register I2C Device ID (Overrides IDx pin) 0: Device ID is from IDx pin
1	0x01	Reset	7	RW	0x04	Remote Auto Power Down	Remote Auto Power Down 1: Power down when no forward channel link is detected 0: Do not power down when no forward channel link is detected
			6:3				***Reserved***.
			2	RW		BC Enable	Back channel enable 1: Enable 0: Disable
			1	RW		Digital RESET1	Reset the entire digital block including registers This bit is self-clearing. 1: Reset 0: Normal operation
			0	RW		Digital RESET0	Reset the entire digital block except registers This bit is self-clearing 1: Reset 0: Normal operation
2	0x02	Configuration [0]	7	RW	0x00	Output Enable	LVCMOS Output Enable. 1: Enable 0: Disable. Tri-state Outputs
			6	RW		OEN and OSS_SEL Override	Overrides Output Enable Pin and Output State pin 1: Enable override 0: Disable - no override
			5	RW		OSC Clock Enable	OSC Clock Output Enable If loss of lock OSC clock is output onto PCLK 0: Disable 1: Enable
			4	RW		Output Sleep State Select (OSS_SEL)	OSS Select to Control Output State during Lock Low Period 1: Enable 0: Disable
			3	RW		Backward Compatible select by pin or register control	Backward Compatible (BC) mode set by MODE_SEL pin or register. 1: BC is set by register bit. Use register bit reg_0x02[2] to set BC Mode 0: Use MODE_SEL pin.
			2	RW		Backward Compatible Mode Select	Backward compatible (BC) mode to DS90UR905Q or DS90UR907Q, if reg_0x02[3] = 1 1: Backward compatible with DS90UR905Q or DS90UR907Q (Set LFMODE = 0) 0: Backward Compatible is *OFF* (default)
			1	RW		LFMODE select by pin or register control	Frequency range is set by MODE_SEL pin or register 1: Frequency range is set by register. Use register bitreg_0x02[0] to set LFMODE 0: Frequency range is set by MODE_SEL pin.
			0	RW		LFMODE	Frequency range select 1: PCLK range = 5 to <15 MHz, if reg_0x02[1] = 1 0: PCLK range = 15 to 85 MHz (default)

Register Maps (continued)

Table 11. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Descriptions
3	0x03	Configuration [1]	7		0xF0		***Reserved***.
			6	RW		CRC Generator Enable	CRC Generator Enable (Back Channel) 1: Enable 0: Disable
			5				***Reserved***
			4	RW		Filter Enable	HS, VS, DE two clock filter When enabled, pulses less than two full PCLK cycles on the DE, HS, and VS inputs will be rejected 1: Filtering enable 0: Filtering disable
			3	RW		I2C Pass-through	I2C Pass-Through Mode 1: Pass-Through Enabled 0: Pass-Through Disabled
			2	RW		Auto ACK	ACK Select 1: Auto ACK enable 0: Self ACK
			1				***Reserved***
			0	RW		RRFB	Pixel Clock Edge Select 1: Parallel Interface Data is strobed on the Rising Clock Edge. 0: Parallel Interface Data is strobed on the Falling Clock Edge.
4	0x04	BCC Watchdog Control	7:1	RW	0xFE	BCC Watchdog Timer	The watchdog timer allows termination of a control channel transaction, if it fails to complete within a programmed amount of time. This field sets the Bidirectional Control Channel Watchdog Timeout value in units of 2 milliseconds. This field should not be set to 0
			0	RW		BCC Watchdog Timer Disable	Disable Bidirectional Control Channel Watchdog Timer 1: Disables BCC Watchdog Timer operation 0: Enables BCC Watchdog Timer operation"
5	0x05	I2C Control [1]	7	RW	0x2E	I2C Pass Through All	I2C Pass-Through All Transactions 1: Enabled 0: Disabled
			6:4	RW		I2C SDA Hold Time	Internal I2C SDA Hold Time It configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 50 ns.
			3:0	RW		I2C Filter Depth	I2C Glitch Filter Depth It configures the maximum width of glitch pulses on the SCL and SDA inputs that will be rejected. Units are 5 ns.

Register Maps (continued)

Table 11. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Descriptions
6	0x06	I2C Control [2]	7	R	0x00	Forward Channel Sequence Error	Control Channel Sequence Error Detected It indicates a sequence error has been detected in forward control channel. It this bit is set, an error may have occurred in the control channel operation.
			6	RW		Clear Sequence Error	It clears the Sequence Error Detect bit This bit is not self-clearing.
			5				***Reserved***
			4:3	RW		SDA Output Delay	SDA Output Delay This field configures output delay on the SDA output. Setting this value will increase output delay in units of 50 ns. Nominal output delay values for SCL to SDA are: 00 : 250 ns 01: 300 ns 10: 350 ns 11: 400 ns
			2	RW		Local Write	Disable Remote Writes to Local Registers through Serializer (Does not affect remote access to I2C slaves at Deserializer) 1: Stop remote write to local device registers 0: remote write to local device registers
			1	RW		I2C Bus Timer Speed	Speed up I2C Bus Watchdog Timer 1: Timer expires after approximately 50 ms 0: Timer expires after approximately 1 s
			0	RW		I2C Bus Timer Disable	Disable I2C Bus Timer When the I2C Timer may be used to detect when the I2C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signalling occurs for approximately 1 s, the I2C bus is assumed to be free. If SDA is low and no signaling occurs, the device will try to clear the bus by driving 9 clocks on SCL
7	0x07	Remote Device ID	7:1	RW	0x18	Remote ID	Remote ID Configures the I2C Slave ID of the remote Serializer. A value of 0 in this field disables I2C access to remote Serializer. This field is automatically configured through the Serializer Forward Channel. Software may overwrite this value, but should also set the FREEZE DEVICE ID bit to prevent overwriting by the Forward Channel.
			0	RW		Freeze Device ID	Freeze Serializer Device ID 1: Prevent auto-loading of the Serializer Device ID from the Forward Channel. The ID will be frozen at the value written. 0: Update
8	0x08	SlaveID[0]	7:1	RW	0x00	Target Slave Device ID0	7-bit Remote Slave Device ID 0 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID0, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
			0				***Reserved***
9	0x09	SlaveID[1]	7:1	RW	0x00	Target Slave Device ID1	7-bit Remote Slave Device ID 1 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID1, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
			0				***Reserved***

Register Maps (continued)

Table 11. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Descriptions
10	0x0A	SlaveID[2]	7:1	RW	0x00	Target Slave Device ID2	7-bit Remote Slave Device ID 2 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID2, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
			0				***Reserved***
11	0x0B	SlaveID[3]	7:1	RW	0x00	Target Slave Device ID3	7-bit Remote Slave Device ID 3 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID3, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
			0				***Reserved***
12	0x0C	SlaveID[4]	7:1	RW	0x00	Target Slave Device ID4	7-bit Remote Slave Device ID 4 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID4, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
			0				***Reserved***
13	0x0D	SlaveID[5]	7:1	RW	0x00	Target Slave Device ID5	7-bit Remote Slave Device ID 5 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID5, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
			0				***Reserved***
14	0x0E	SlaveID[6]	7:1	RW	0x00	Target Slave Device ID6	7-bit Remote Slave Device ID 6 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID6, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
			0				***Reserved***
15	0x0F	SlaveID[7]	7:1	RW	0x00	Target Slave Device ID7	7-bit Remote Slave Device ID 7 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID7, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
			0				***Reserved***
16	0x10	SlaveAlias[0]	7:1	RW	0x00	ID[0] Match	7-bit Remote Slave Device Alias ID 0 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID0 register. A value of 0 in this field disables access to the remote I2C Slave.
			0				***Reserved***

Register Maps (continued)

Table 11. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Descriptions
17	0x11	SlaveAlias[1]	7:1	RW	0x00	ID[1] Match	7-bit Remote Slave Device Alias ID 1 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID1 register. A value of 0 in this field disables access to the remote I2C Slave.
			0				***Reserved***
18	0x12	SlaveAlias[2]	7:1	RW	0x00	ID[2] Match	7-bit Remote Slave Device Alias ID 2 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID2 register. A value of 0 in this field disables access to the remote I2C Slave.
			0				***Reserved***
19	0x13	SlaveAlias[3]	7:1	RW	0x10	ID[3] Match	7-bit Remote Slave Device Alias ID 3 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID3 register. A value of 0 in this field disables access to the remote I2C Slave.
			0				***Reserved***
20	0x14	SlaveAlias[4]	7:1	RW	0x00	ID[4] Match	7-bit Remote Slave Device Alias ID 4 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID4 register. A value of 0 in this field disables access to the remote I2C Slave.
			0				***Reserved***
21	0x15	SlaveAlias[5]	7:1	RW	0x00	ID[5] Match	7-bit Remote Slave Device Alias ID 5 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID5 register. A value of 0 in this field disables access to the remote I2C Slave.
			0				***Reserved***
22	0x16	SlaveAlias[6]	7:1	RW	0x00	ID[6] Match	7-bit Remote Slave Device Alias ID 6 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID6 register. A value of 0 in this field disables access to the remote I2C Slave.
			0	RW			***Reserved***
23	0x17	SlaveAlias[7]	7:1	RW	0x00	ID[7] Match	7-bit Remote Slave Device Alias ID 7 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID7 register. A value of 0 in this field disables access to the remote I2C Slave.
			0				***Reserved***

Register Maps (continued)

Table 11. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Descriptions
28	0x1C	General Status	7:4	RW	0x00		***Reserved***
			3	R		I2S Locked	I2S Lock Status 0: I2S PLL controller not locked 1: I2S PLL controller locked to input I2S clock
			2				***Reserved***
			1	R		Signal Detect	Signal Detect 1: Serial input detected 0: Serial input not detected
			0	R		Lock	Deserializer CDR, PLL's clock to recovered clock frequency 1: Deserializer locked to recovered clock 0: Deserializer not locked
29	0x1D	GPIO0 Config	7:4	R	0xA0	Rev-ID	Revision ID: 1010: Production Device
			3	RW		GPIO0 Output Value	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
			2	RW		GPIO0 Remote Enable	Remote GPIO0 Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Deserializer. 0: Disable GPIO control from remote Serializer
			1	RW		GPIO0 Direction	Local GPIO Direction 1: Input 0: Output
			0	RW		GPIO0 Enable	GPIO Function Enable 1: Enable GPIO operation 0: Enable normal operation
30	0x1E	GPIO2 and GPIO1 Config	7	RW	0x00	GPIO2 Output Value	Local GPIO Output Value This value is output on the GPIO when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
			6	RW		GPIO2 Remote Enable	Remote GPIO2 Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Deserializer. 0: Disable GPIO control from remote Serializer.
			5	RW		GPIO2 Direction	Local GPIO Direction 1: Input 0: Output
			4	RW		GPIO2 Enable	GPIO Function Enable 1: Enable GPIO operation 0: Enable normal operation
			3	RW		GPIO1 Output Value	Local GPIO Output Value This value is output on the GPIO when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
			2	RW		GPIO1 Remote Enable	Remote GPIO1 Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Deserializer. 0: Disable GPIO control from remote Serializer.
			1	RW		GPIO1 Direction	Local GPIO Direction 1: Input 0: Output
			0	RW		GPIO1 Enable	GPIO Function Enable 1: Enable GPIO operation 0: Enable normal operation

Register Maps (continued)

Table 11. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Descriptions
31	0x1F	GPO_REG4 and GPO3 Config	7	RW	0x00	GPO_REG4 Output Value	Local GPO_REG4 Output Value This value is output on the GPO when the GPO function is enabled, the local GPO direction is Output, and remote GPO control is disabled.
			6:5				***Reserved***
			4	RW		GPO_REG4 Enable	GPO_REG4 Function Enable 1: Enable GPO operation 0: Enable normal operation
			3	RW		GPIO3 Output Value	Local GPIO Output Value This value is output on the GPIO when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
			2	RW		GPIO3 Remote Enable	Remote GPIO3 Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Deserializer. 0: Disable GPIO control from remote Serializer.
			1	RW		GPIO3 Direction	Local GPIO Direction 1: Input 0: Output
			0	RW		GPIO3 Enable	GPIO Function Enable 1: Enable GPIO operation 0: Enable normal operation
32	0x20	GPO_REG6 and GPO_REG5 Config	7	RW	0x00	GPO_REG6 Output Value	Local GPO_REG6 Output Value This value is output on the GPO when the GPO function is enabled, the local GPO direction is Output, and remote GPO control is disabled.
			6:5				***Reserved***
			4	RW		GPO_REG6 Enable	GPO_REG6 Function Enable 1: Enable GPO operation 0: Enable normal operation
			3	RW		GPO_REG5 Output Value	Local GPO_REG5 Output Value This value is output on the GPO when the GPO function is enabled, the local GPO direction is Output, and remote GPO control is disabled.
			2:1				***Reserved***
			0	RW		GPO_REG5 Enable	GPO_REG5 Function Enable 1: Enable GPO operation 0: Enable normal operation
33	0x21	GPO8 and GPO7 Config	7	RW	0x00	GPO_REG8 Output Value	Local GPO_REG8 Output Value This value is output on the GPO when the GPO function is enabled, the local GPO direction is Output, and remote GPO control is disabled.
			6:5				***Reserved***
			4	RW		GPO_REG8 Enable	GPO_REG8 Function Enable 1: Enable GPO operation 0: Enable normal operation
			3	RW		GPO_REG7 Output Value	Local GPO_REG7 Output Value This value is output on the GPO when the GPO function is enabled, the local GPO direction is Output, and remote GPO control is disabled.
			2:1				***Reserved***
			0	RW		GPO_REG7 Enable	GPO_REG7 Function Enable 1: Enable GPO operation 0: Enable normal operation

Register Maps (continued)

Table 11. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Descriptions
34	0x22	Data Path Control	7	RW	0x00	Override FC Config	1: Disable loading of this register from the forward channel, keeping locally written values intact 0: Allow forward channel loading of this register
			6	RW		Pass RGB	Setting this bit causes RGB data to be sent independent of DE. This allows operation in systems which may not use DE to frame video data or send other data when DE is deasserted. Note that setting this bit prevents HDCP operation and blocks packetized audio. This bit does not need to be set in DS90UB925 or in Backward Compatible mode. 1: Pass RGB independent of DE 0: Normal operation Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set.
			5	RW		DE Polarity	This bit indicates the polarity of the DE (Data Enable) signal. 1: DE is inverted (active low, idle high) 0: DE is positive (active high, idle low) Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set.
			4	RW		I2S_Gen	This bit controls whether the HDCP Receiver outputs packetized Auxiliary/Audio data on the RGB video output pins. 1: Don't output packetized audio data on RGB video output pins 0: Output packetized audio on RGB video output pins. Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set.
			3	RW		I2S Channel B Enable Override	1: Set I2S Channel B Enable from reg_0x22[0] 0: Set I2S Channel B Enable from MODE_SEL pin Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set.
			2	RW		18-bit Video Select	1: Select 18-bit video mode Note: use of GPIO(s) on unused inputs must be enabled by register. 0: Select 24-bit video mode Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set.
			1	RW		I2S Transport Select	1: Enable I2S Data Forward Channel Frame Transport 0: Enable I2S Data Island Transport Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set.
			0	RW		I2S Channel B Enable	I2S Channel B Enable 1: Enable I2S Channel B on B1 output 0: I2S Channel B disabled Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set.
35	0x23	General Purpose Control	7	RW	0x10	Rx RGB Checksum	RX RGB Checksum Enable Setting this bit enables the Receiver to validate a one-byte checksum following each video line. Checksum failures are reported in the HDCP_STS register
			6:5				***Reserved***
		Mode Status	4	R		Mode_Sel	Mode Select is Done
			3	R		LFMODE	Low Frequency Mode Status
			2	R		Repeater	Repeater Mode Status
			1	R		Backward	Backward Compatible Mode Status
			0	R		I2S Channel B	I2S Channel B Status

Register Maps (continued)

Table 11. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Descriptions
36	0x24	BIST Control	7:4		0x08		***Reserved***
			3	RW		BIST Pin Config	BIST Configured through Pin 1: BIST configured through pin 0: BIST configured through register bit
			2:1	RW		BIST Clock Source	BIST Clock Source 00: External Pixel Clock 01: 33 MHz Oscillator 10: Reserved 11: 25 MHz Oscillator
			0	RW		BIST Enable	BIST Control 1: Enabled 0: Disabled
37	0x25	BIST Error	7:0	R	0x00	BIST Error Count	BIST Error Count
38	0x26	SCL High Time	7:0	RW	0x83	SCL High Time	I2C Master SCL High Time This field configures the high pulse width of the SCL output when the Deserializer is the Master on the local I2C bus. Units are 50 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5 us SCL high time with the internal oscillator clock running at 26 MHz rather than the nominal 20 MHz.
39	0x27	SCL Low Time	7:0	RW	0x84	SCL Low Time	I2C SCL Low Time This field configures the low pulse width of the SCL output when the De-Serializer is the Master on the local I2C bus. This value is also used as the SDA setup time by the I2C Slave for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. Units are 50 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5 us SCL low time with the internal oscillator clock running at 26 MHz rather than the nominal 20 MHz.
41	0x29	FRC Control	7	RW	0x00	Timing Mode Select	Select display timing mode 0: DE only Mode 1: Sync Mode (VS,HS)
			6	RW		VS Polarity	0: Active High 1: Active Low
			5	RW		HS Polarity	0: Active High 1: Active Low
			4	RW		DE Polarity	0: Active High 1: Active Low
			3	RW		FRC2 Enable	0: FRC2 Disable 1: FRC2 Enable
			2	RW		FRC1 Enable	0: FRC1 Disable 1: FRC1 Enable
			1	RW		Hi-FRC 2 Disable	0: Hi-FRC2 Enable 1: Hi-FRC2 Disable
			0	RW		Hi-FRC 1 Disable	0: Hi-FRC1 Enable 1: Hi-FRC1 Disable
42	0x2A	White Balance Control	7:6	RW	0x00	Page Setting	00: Configuration Registers 01: Red LUT 10: Green LUT 11: Blue LUT
			5	RW		White Balance Enable	0: White Balance Disable 1: White Balance Enable
			4	RW		LUT Reload Enable	0: Reload Disable 1: Reload Enable
			3:0				***Reserved***

Register Maps (continued)

Table 11. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Descriptions
43	0x2B	I2S Control	7	RW	0x00	I2S PLL	I2S PLL Control 0: I2S PLL is *ON* for I2S data jitter cleaning 1: I2S PLL is *OFF*. No jitter cleaning
			6:1				***Reserved***
			0	RW		I2S Clock Edge	I2S Clock Edge Select 0: I2S Data is strobed on the Rising Clock Edge 1: I2S Data is strobed on the Falling Clock Edge
44	0x2C	SSCG Control	7:4		0x00		***Reserved***
			3	RW		SSCG Enable	Enable Spread Spectrum Clock Generator 0: Disable 1: Enable
			2:0	RW		SSCG Selection	SSCG Frequency Deviation: When LFMODE = H fdev fmod 000: ±0.7 CLK / 628 001: ±1.3 010: ±1.8 011: ±2.5 100: ±0.7 CLK / 388 101: ±1.2 110: ±2.0 111: ±2.5 When LFMODE = L fdev fmod 000: ±0.9 CLK / 2168 001: ±1.2 010: ±1.9 011: ±2.5 100: ±0.7 CLK / 1300 101: ±1.3 110: ±2.0 111: ±2.5
58	0x3A	I2S DIVSEL	7	RW	0x00	MCLK Div Override	0: No override for MCLK divider (default) 1: Override divider select for MCLK
			6:4	RW		MCLK Div	See Table 5
			3:0				***Reserved***
65	0x41	Link Error Count	7:5		0x03		***Reserved***
			4	RW		Link Error Count Enable	Enable serial link data integrity error count 1: Enable error count 0: Disable
			3:0	RW		Link Error Count	Link error count threshold. Counter is pixel clock based. clk0, clk1 and DCA are monitored for link errors, if error count is enabled, deserializer loose lock once error count reaches threshold. If disabled deserilizer loose lock with one error.

Register Maps (continued)

Table 11. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Descriptions
68	0x44	Equalization	7:5	RW	0x60	EQ Stage 1 Select	EQ select value. Used if adaptive EQ is bypassed. 000 Min EQ 1st Stage 001 010 011 100 101 110 111 Max EQ 1st Stage
			4				***Reserved***
			3:1	RW		EQ Stage 2 Select	EQ select value. Used if adaptive EQ is bypassed. 000 Min EQ 2nd Stage 001 010 011 100 101 110 111 Max EQ 2nd Stage
			0	RW		Adaptive EQ	1: Disable adaptive EQ (to write EQ select values) 0: Enable adaptive EQ
86	0x56	CML Output	7:4		0x08		***Reserved***
			3	RW		CMLOUT+/- Enable	1: Disabled (Default) 0: Enabled
			2:0				***Reserved***
100	0x64	Pattern Generator Control	7:4	RW	0x10	Pattern Generator Select	Fixed Pattern Select This field selects the pattern to output when in Fixed Pattern Mode. Scaled patterns are evenly distributed across the horizontal or vertical active regions. This field is ignored when Auto-Scrolling Mode is enabled. The following table shows the color selections in non-inverted followed by inverted color mode 0000: Reserved 0001: White/Black 0010: Black/White 0011: Red/Cyan 0100: Green/Magenta 0101: Blue/Yellow 0110: Horizontally Scaled Black to White/White to Black 0111: Horizontally Scaled Black to Red/Cyan to White 1000: Horizontally Scaled Black to Green/Magenta to White 1001: Horizontally Scaled Black to Blue/Yellow to White 1010: Vertically Scaled Black to White/White to Black 1011: Vertically Scaled Black to Red/Cyan to White 1100: Vertically Scaled Black to Green/Magenta to White 1101: Vertically Scaled Black to Blue/Yellow to White 1110: Custom color (or its inversion) configured in PGRS, PGGS, PGBS registers 1111: Reserved
			3:1				***Reserved***
			0	RW		Pattern Generator Enable	Pattern Generator Enable 1: Enable Pattern Generator 0: Disable Pattern Generator

Register Maps (continued)

Table 11. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Descriptions
101	0x65	Pattern Generator Configuration	7:5		0x00		***Reserved***
			4	RW		Pattern Generator 18 Bits	18-bit Mode Select 1: Enable 18-bit color pattern generation. Scaled patterns will have 64 levels of brightness and the R, G, and B outputs use the six most significant color bits. 0: Enable 24-bit pattern generation. Scaled patterns use 256 levels of brightness.
			3	RW		Pattern Generator External Clock	Select External Clock Source 1: Selects the external pixel clock when using internal timing. 0: Selects the internal divided clock when using internal timing This bit has no effect in external timing mode (PATGEN_TSEL = 0).
			2	RW		Pattern Generator Timing Select	Timing Select Control 1: The Pattern Generator creates its own video timing as configured in the Pattern Generator Total Frame Size, Active Frame Size. Horizontal Sync Width, Vertical Sync Width, Horizontal Back Porch, Vertical Back Porch, and Sync Configuration registers. 0: the Pattern Generator uses external video timing from the pixel clock, Data Enable, Horizontal Sync, and Vertical Sync signals.
			1	RW		Pattern Generator Color Invert	Enable Inverted Color Patterns 1: Invert the color output. 0: Do not invert the color output.
			0	RW		Pattern Generator Auto-Scroll Enable	Auto-Scroll Enable: 1: The Pattern Generator will automatically move to the next enabled pattern after the number of frames specified in the Pattern Generator Frame Time (PGFT) register. 0: The Pattern Generator retains the current pattern.
102	0x66	Pattern Generator Indirect Address	7:0	RW	0x00	Indirect Address	This 8-bit field sets the indirect address for accesses to indirectly-mapped registers. It should be written prior to reading or writing the Pattern Generator Indirect Data register. See *AN-2198 Exploring Int Test Patt Gen Feat of 720p FPD-Link III Devices* (SNLA132)
103	0x67	Pattern Generator Indirect Data	7:0	RW	0x00	Indirect Data	When writing to indirect registers, this register contains the data to be written. When reading from indirect registers, this register contains the read back value. See *AN-2198 Exploring Int Test Patt Gen Feat of 720p FPD-Link III Devices* (SNLA132)
128	0x80	RX_BKSV0	7:0	R	0x00	RX BKSV0	BKSV0: Value of byte 0 of the Deserializer KSV
129	0x81	RX_BKSV1	7:0	R	0x00	RX BKSV1	BKSV1: Value of byte 1 of the Deserializer KSV
130	0x82	RX_BKSV2	7:0	R	0x00	RX BKSV2	BKSV2: Value of byte 2 of the Deserializer KSV
131	0x83	RX_BKSV3	7:0	R	0x00	RX BKSV3	BKSV3: Value of byte 3 of the Deserializer KSV.
132	0x84	RX_BKSV4	7:0	R	0x00	RX BKSV4	BKSV4: Value of byte 4 of the Deserializer KSV.
144	0x90	TX_KSV0	7:0	R	0x00	TX KSV0	KSV0: Value of byte 0 of the Serializer KSV.
145	0x91	TX_KSV1	7:0	R	0x00	TX KSV1	KSV1: Value of byte 1 of the Serializer KSV.
146	0x92	TX_KSV2	7:0	R	0x00	TX KSV2	KSV2: Value of byte 2 of the Serializer KSV.
147	0x93	TX_KSV3	7:0	R	0x00	TX KSV3	KSV3: Value of byte 3 of the Serializer KSV.
148	0x94	TX_KSV4	7:0	R	0x00	TX KSV4	KSV4: Value of byte 4 of the Serializer KSV.

Register Maps (continued)

Table 11. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Descriptions
192	0xC0	HDCP_DBG	7:4		0x00		***Reserved***
			3	R		RGB_CHK SUM_EN	Enable RBG video line checksum. 1: Enables sending of ones-complement checksum for each 8-bit RBG data channel following end of each video data line. 0: Checksum disabled Set via the HDCP_DBG register in the HDCP Transmitter.
			2	R		FC_TEST MODE	Frame Counter Testmode: 1: Speeds up frame counter used for Pj and Ri verification. When set to a 1, Pj is computed every 2 frames and Ri is computed every 16 frames. 0: Pj is computed every 16 frames and Ri is computed every 128 frames. Set via the HDCP_DBG register in the HDCP Transmitter.
			1	R		TMR_ SPEEDUP	Timer Speedup: 1: Speed up HDCP authentication timers. 0: Standard authentication timing Set via the HDCP_DBG register in the HDCP Transmitter.
			0	R		HDCP_I2C _FAST	HDCP I2C Fast mode Enable: 1: Enable the HDCP I2C Master in the HDCP Receiver to operation with Fast mode timing. 0:Tthe I2C Master will operate with Standard mode timing. Set via the HDCP_DBG register in the HDCP Transmitter.
193	0xC1	HDCP_DBG2	7:2		0x00		***Reserved***
			1	RW		NO_ DECRYPT	No Decrypt: 1: The HDCP Receiver outputs the encrypted data on the RGB pins. All other functions will work normally. This provides a simple way of showing that the link is encrypted. 0: Normal Operation
			0				***Reserved***
196	0xC4	HDCP Status	7:2		0x00		***Reserved***
			1	R		RGB_CHK SUM_ERR	RGB Checksum Error Detected: If RGB Checksum in enabled through the HDCP Transmitter HDCP_DBG register, this bit will indicate if a checksum error is detected. This register may be cleared by writing any value to this register.
			0	R		HDCP Status	HDCP Authenticated: Indicates the HDCP authentication has completed successfully. The controller may now send video data requiring content protection. This bit will be cleared if authentication is lost or if the controller restarts authentication.
224	0xE0	RPTR TX0	7:1	R	0x0	HDCP Serializer Port 0 Address	Serializer Port 0 I2C Address: Indicates the I2C address for the Repeater Serializer Port.
			0	R			Serializer Port 0 Valid: Indicates that the HDCP Repeater has a Serializer port at the I2C Address identified by upper 7 bits of this register.
225	0xE1	RPTR TX1	7:1	R	0x00	HDCP Serializer Port 1 Address	Serializer Port 1 I2C Address: Indicates the I2C address for the Repeater Serializer Port.
			0	R			Serializer Port 1 Valid: Indicates that the HDCP Repeater has a Serializer port at the I2C Address identified by upper 7 bits of this register.
226	0xE2	RPTR TX2	7:1		0x00	HDCP Serializer Port 2 Address	Serializer Port 2 I2C Address: Indicates the I2C address for the Repeater Serializer Port.
			0	R			Serializer Port 2 Valid: Indicates that the HDCP Repeater has a Serializer port at the I2C Address identified by upper 7 bits of this register.

Register Maps (continued)

Table 11. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	Register Name	Bit(s)	Register Type	Default (hex)	Function	Descriptions
227	0xE3	RPTR TX3	7:1	R	0x00	HDCP Serializer Port 3 Address	Serializer Port 3 I2C Address: Indicates the I2C address for the Repeater Serializer Port.
			0	R			Serializer Port 3 Valid: Indicates that the HDCP Repeater has a Serializer port at the I2C Address identified by upper 7 bits of this register
240	0xF0	HDCP RX ID	7:0	R	0x5F	ID0	First byte ID code: _
241	0xF1		7:0	R	0x55	ID1	Second byte of ID code: U
242	0xF2		7:0	R	0x48	ID2	Third byte of ID code, Value will be either ‘B’ or ‘H’. ‘H’ indicates an HDCP capable device.
243	0xF3		7:0	R	0x39	ID3	Fourth byte of ID code: 9
244	0xF4		7:0	R	0x32	ID4	Fifth byte of ID code: 2
245	0xF5		7:0	R	0x36	ID5	Sixth byte of ID code: 6

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DS90UH926Q-Q1, in conjunction with the DS90UH925Q-Q1, is intended for interface between a HDCP compliant host (graphics processor) and a Display. It supports an 24-bit color depth (RGB888) and high definition (720p) digital video format. It allows to receive a three 8-bit RGB stream with a pixel rate up to 85 MHz together with three control bits (VS, HS and DE) and three I2S-bus audio stream with an audio sampling rate up to 192 kHz. The included HDCP 1.3 compliant cipher block allows the authentication of the DS90UH926Q, which decrypts both video and audio contents. The keys are pre-loaded by TI into non-volatile memory (NVM) for maximum security.

8.1.1 Display Application

The deserializer is expected to be located close to its target device. The interconnect between the deserializer and the target device is typically in the 1-inch to 3-inch separation range. The input capacitance of the target device is expected to be in the 5-pF to 10-pF range. Take care of the PCLK output trace as this signal is edge-sensitive and strobes the data. It is also assumed that the fanout of the deserializer is up to three in the repeater mode. If additional loads need to be driven, a logic buffer or mux device is recommended.

8.2 Typical Application

Figure 24 shows a typical application of the DS90UH926Q-Q1 deserializer for an 85 MHz 24-bit color display application. Inputs utilize 0.1-μF coupling capacitors to the line and the deserializer provides internal termination. Bypass capacitors are placed near the power supply pins. At a minimum, seven 0.1-μF capacitors and two 4.7-μF capacitors should be used for local device bypassing. Ferrite beads are placed on the power lines for effective noise suppression. Because the device in the Pin/STRAP mode, two 10 kΩ pull-up resistors are used on the parallel output bus to select the desired device features.

The interface to the target display is with 3.3-V LVCMOS levels, thus the V_{DDIO} pins are connected to the 3.3-V rail. A delay cap is placed on the PDB signal to delay the enabling of the device until power is stable.

Typical Application (continued)

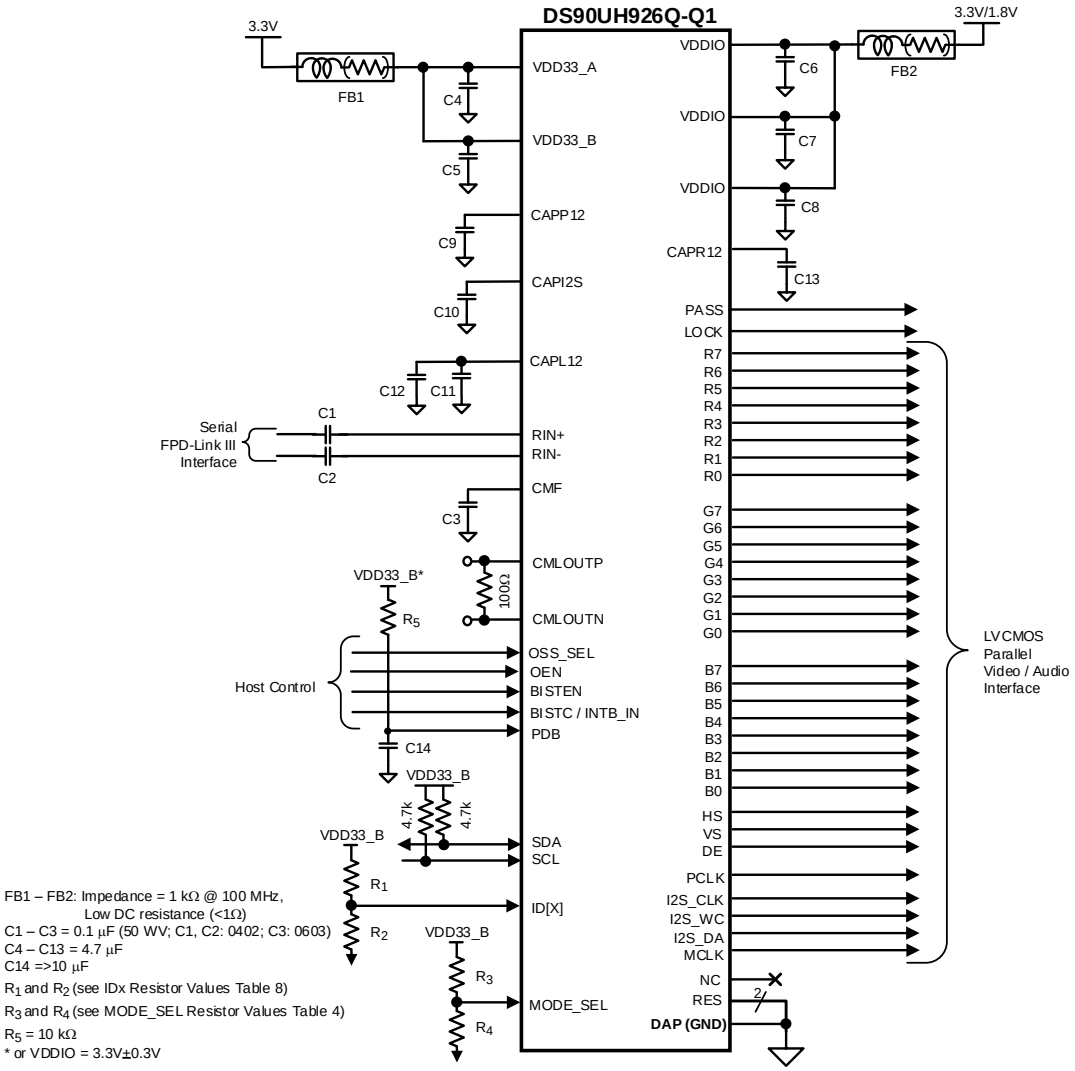


Figure 24. Typical Connection Diagram

Typical Application (continued)

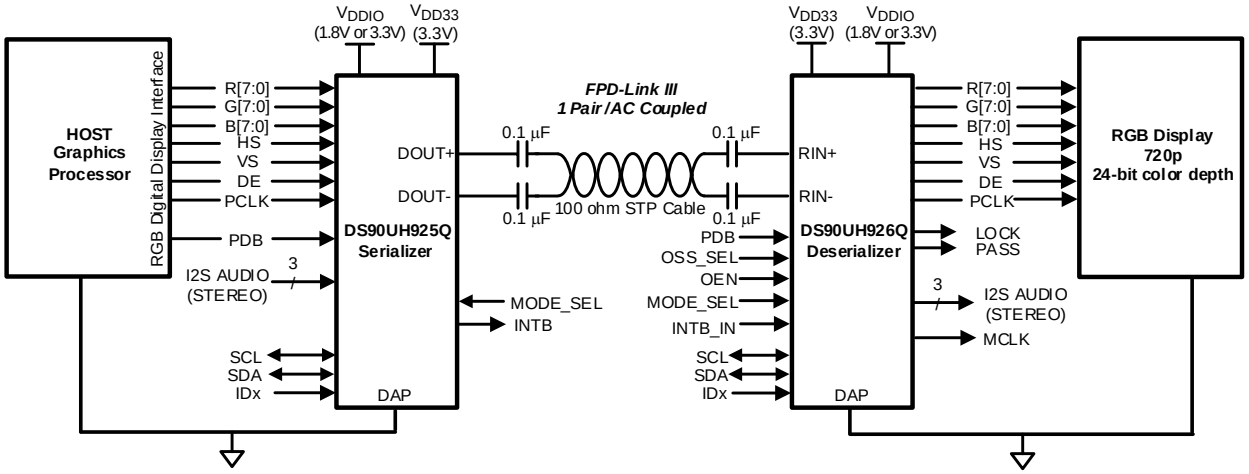


Figure 25. Typical Display System Diagram

8.2.1 Design Requirements

For the typical design application, use the following as input parameters:

Table 12. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VDDIO	1.8 V or 3.3 V
VDD33	3.3 V
AC-Coupling Capacitor for RIN±	100 nF
PCLK Frequency	78 MHz

8.2.2 Detailed Design Procedure

8.2.2.1 Transmission Media

The DS90UH925Q-Q1 and DS90UH926Q-Q1 chipset is intended to be used in a point-to-point configuration through a shielded twisted pair cable. The serializer and deserializer provide internal termination to minimize impedance discontinuities. The interconnect (cable and connector) between the serializer and deserializer should have a differential impedance of 100 Ω. The maximum length of cable that can be used is dependant on the quality of the cable (gauge, impedance), connector, board (discontinuities, power plane), the electrical environment (for example, power stability, ground noise, input clock jitter, PCLK frequency, etc.) and the application environment.

The resulting signal quality at the receiving end of the transmission media may be assessed by monitoring the differential eye opening of the serial data stream. The Receiver CML Monitor Driver Output Specifications define the acceptable data eye opening width and eye opening height. A differential probe should be used to measure across the termination resistor at the CMLOUT± pin Figure 2.

8.2.3 Application Curves

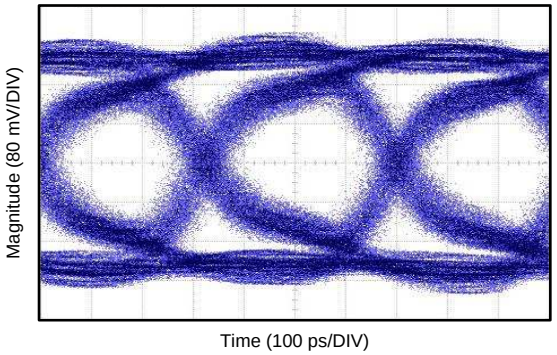


Figure 26. Deserializer CMLOUT Eye Diagram With 78-MHz TX Pixel Clock

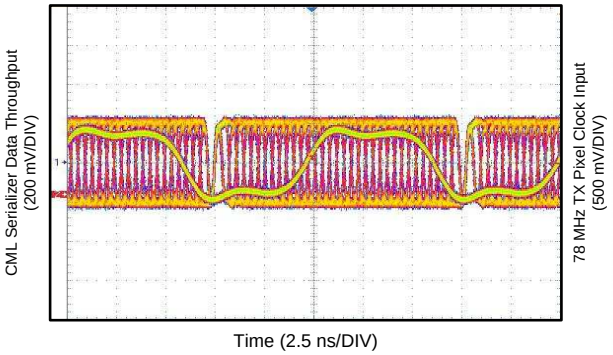


Figure 27. Deserializer FPD-Link III Input With 78-MHz TX Pixel Clock

9 Power Supply Recommendations

9.1 Power-Up Requirements and PDB Pin

When VDDIO and VDD33_X are powered separately, the VDDIO supply (1.8 V or 3.3 V) ramps up 100 µs before the other supply (VDD33_X) begins to ramp. If VDDIO is tied with VDD33_X, both supplies may ramp at the same time. The VDDs (VDD33_X and VDDIO) supply ramp must be faster than 1.5 ms with a monotonic rise. Use a large capacitor on the PDB pin to ensure PDB arrives after all the VDDs have settled to the recommended operating voltage. When PDB pin is pulled to VDDIO = 3 V to 3.6 V or VDD33_X, TI recommends using a 10-kΩ pullup and a > 10-µF cap to GND to delay the PDB input signal.

All inputs must not be driven until VDD33_X and VDDIO has reached its steady-state value.

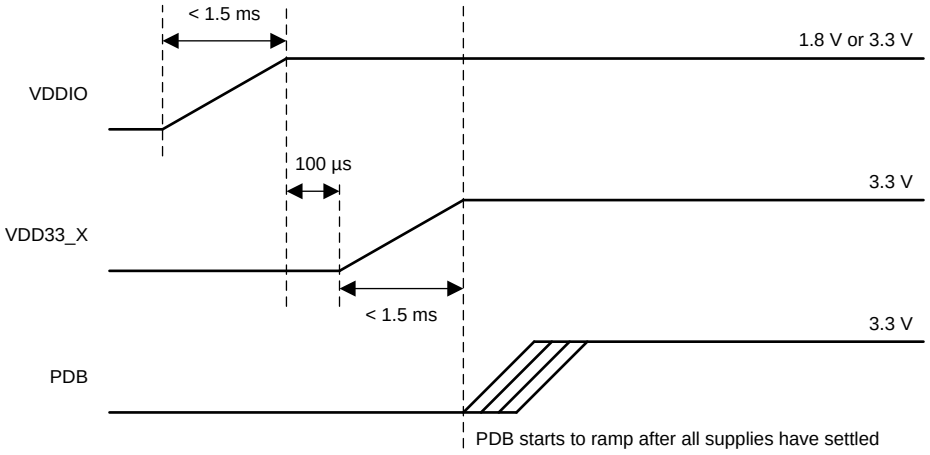


Figure 28. Power-Up Sequence of DS90UH926Q-Q1

10 Layout

10.1 Layout Guidelines

Design the circuit board layout and stack-up for the FPD-Link III devices to provide low-noise power feed to the device. Good layout practice also separates high-frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback, and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 µF to 0.1 µF. Tantalum capacitors may be in the 2.2-µF to 10-µF range. Voltage rating of the tantalum capacitors should be at least 5× the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50 µF to 100 µF range and will smooth low-frequency switching noise. TI recommends connecting the power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path.

TI recommends a small body size X7R chip capacitor, such as 0603 or 0402, for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20 to 30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter may be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the CML lines to prevent coupling from the LVCMOS lines to the CML lines. Closely-coupled differential lines of 100 Ω are typically recommended for CML interconnect. The closely coupled lines help to ensure that coupled noise will appear as common-mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

Information on the WQFN style package is provided in *AN-1187 Leadless Leadframe Package (LLP)* (SNOA401).

Stencil parameters such as aperture area ratio and the fabrication process have a significant impact on paste deposition. Inspection of the stencil prior to placement of the WQFN package is highly recommended to improve board assembly yields. If the via and aperture openings are not carefully monitored, the solder may flow unevenly through the DAP. Stencil parameters for aperture opening and via locations are shown in Table 13:

Table 13. No Pullback WQFN Stencil Aperture Summary

DEVICE	PIN COUNT	MKT Dwg	PCB I/O Pad Size (mm)	PCB PITCH (mm)	PCB DAP SIZE (mm)	STENCIL I/O APERTURE (mm)	STENCIL DAP Aperture (mm)	NUMBER of DAP APERTURE OPENINGS
DS90UH926Q-Q1	60	NKB0060B	0.25 × 0.6	0.5	6.3 × 6.3	0.25 × 0.8	6.3 × 6.3	1

Figure 29 shows the PCB layout example derived from the layout design of the DS90UH926QSEVB Evaluation Board. The graphic and layout description are used to determine both proper routing and proper solder techniques when designing the Serializer board.

10.1.1 CML Interconnect Guidelines

See *AN-1108 Channel-Link PCB and Interconnect Design-In Guidelines* (SNLA008) and *AN-905 Transmission Line RAPIDESIGNER® Operation and Applications Guide* (SNLA035) for full details.

- Use 100-Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  - S = space between the pair
  - 2S = space between pairs
  - 3S = space to LVCMOS signal
- Minimize the number of Vias
- Use differential connectors when operating above 500 Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair

Additional general guidance can be found in the LVDS Owner's Manual - available in PDF format from the TI web site at: www.ti.com/lvds.

10.2 Layout Examples

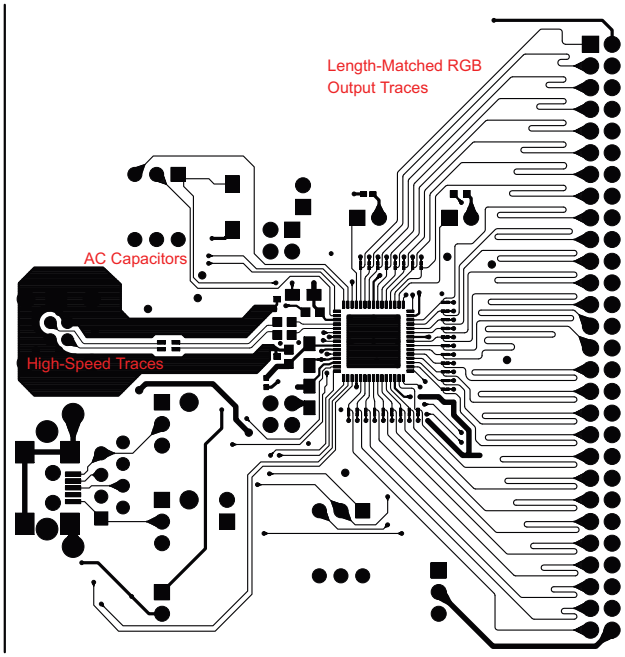


Figure 29. DS90UH926Q-Q1 Deserializer Example Layout

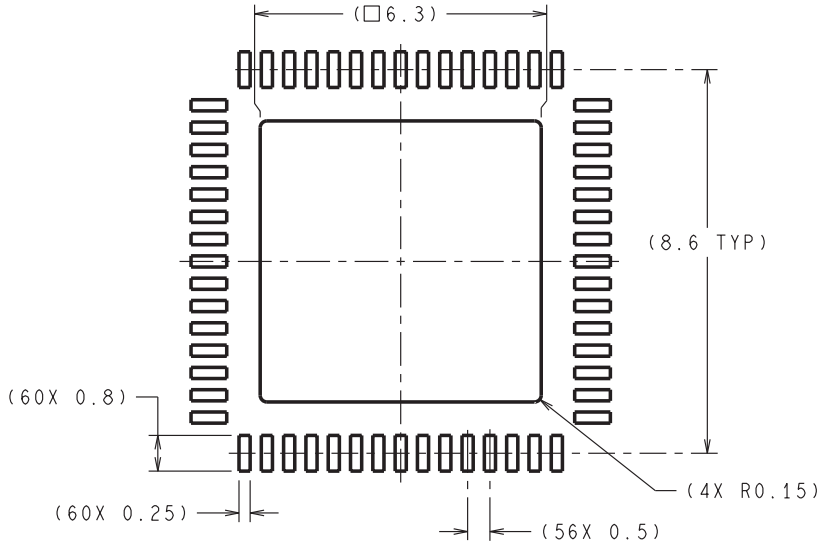


Figure 30. 60-Pin WQFN Stencil Example of Via and Opening Placement

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

- *AN-2198 Exploring the Internal Test Pattern Generation Feature of 720p FPD-Link III Devices* (SNLA132)
- *AN-1187 Leadless Leadframe Package (LLP)* (SNOA401)
- *AN-1108 Channel-Link PCB and Interconnect Design-In Guidelines* (SNLA008)
- *AN-905 Transmission Line RAPIDESIGNER® Operation and Applications Guide* (SNLA035)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90UH926QSQ/NOPB	ACTIVE	WQFN	NKB	60	1000	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 105	UH926QSQ	Samples
DS90UH926QSQE/NOPB	ACTIVE	WQFN	NKB	60	250	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 105	UH926QSQ	Samples
DS90UH926QSQX/NOPB	ACTIVE	WQFN	NKB	60	2000	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 105	UH926QSQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

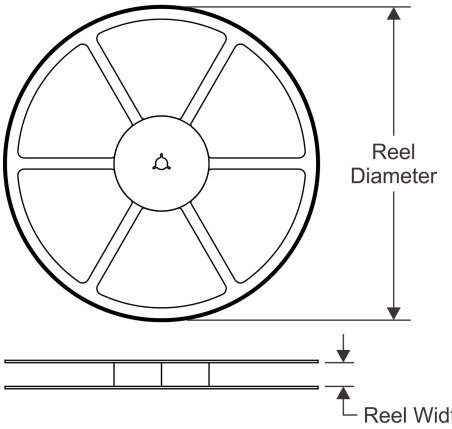
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

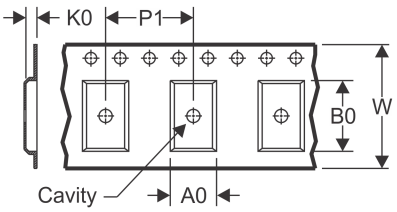
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

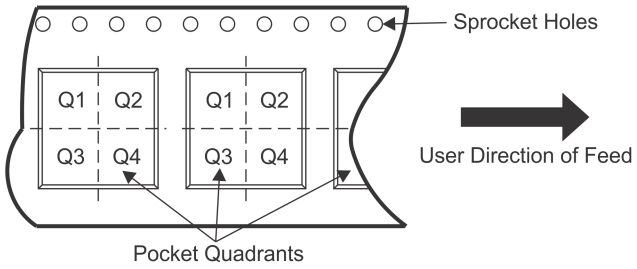


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

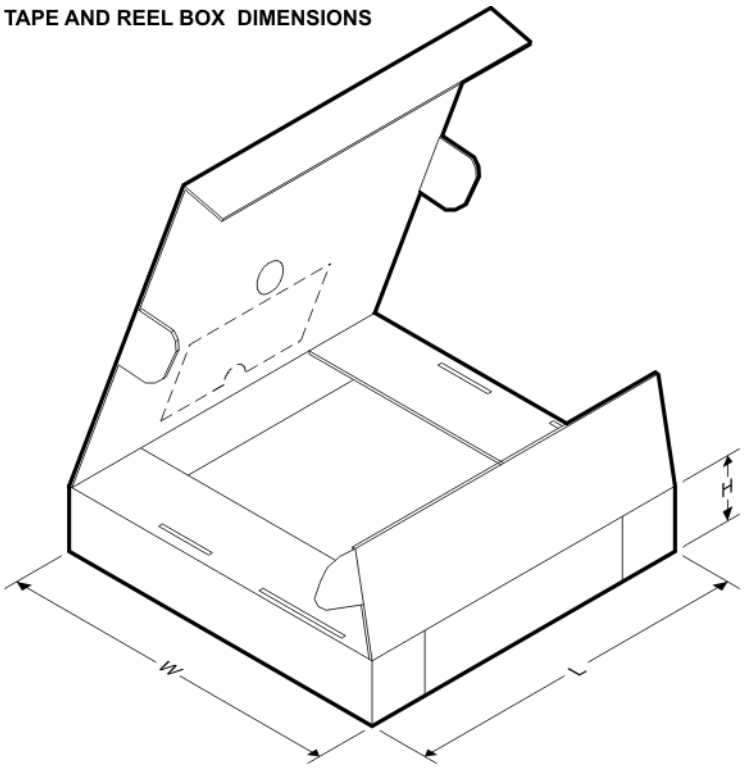
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90UH926QSQ/NOPB	WQFN	NKB	60	1000	330.0	16.4	9.3	9.3	1.3	12.0	16.0	Q1
DS90UH926QSQE/NOPB	WQFN	NKB	60	250	178.0	16.4	9.3	9.3	1.3	12.0	16.0	Q1
DS90UH926QSQX/NOPB	WQFN	NKB	60	2000	330.0	16.4	9.3	9.3	1.3	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

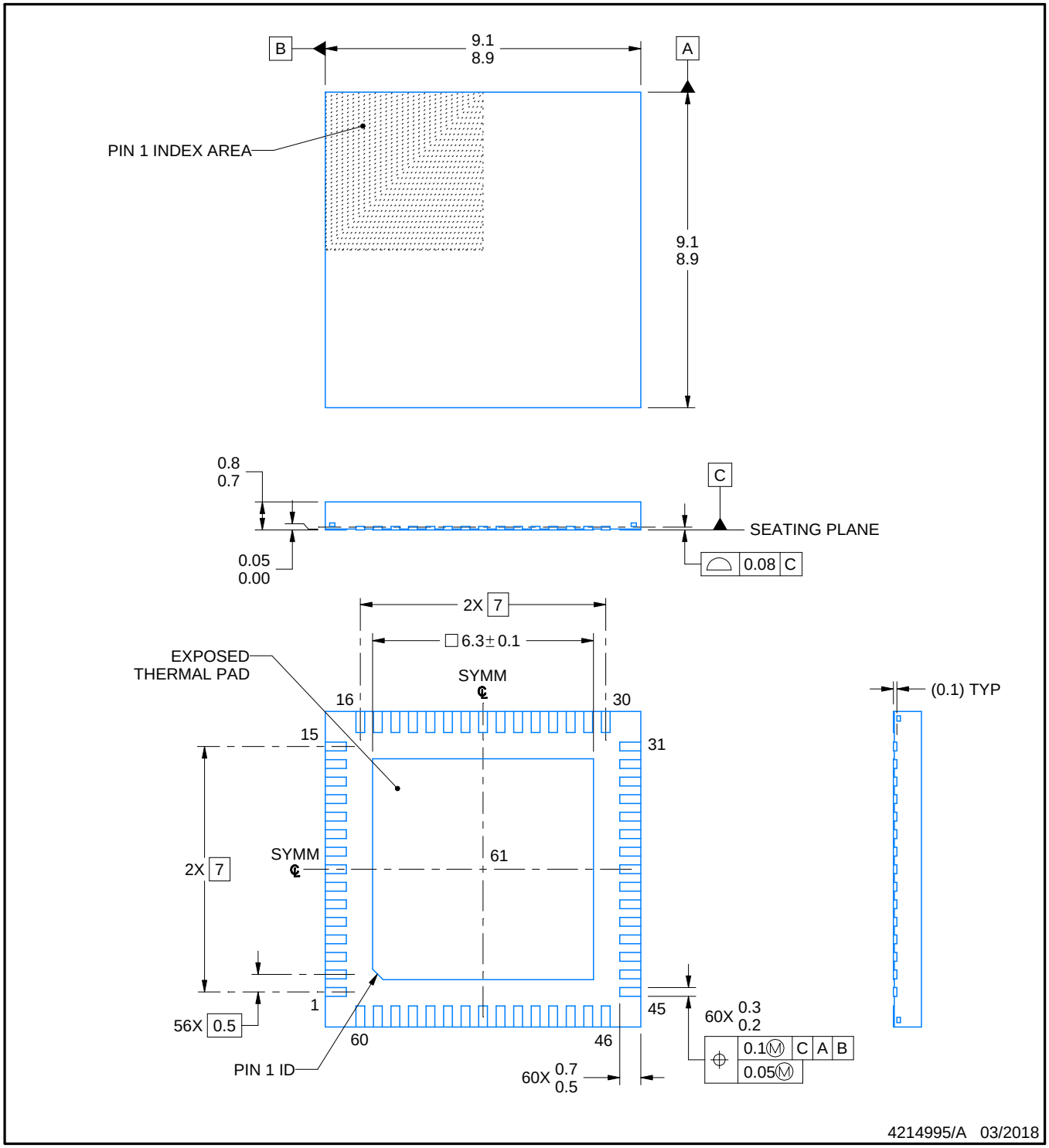
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90UH926QSQ/NOPB	WQFN	NKB	60	1000	367.0	367.0	38.0
DS90UH926QSQE/NOPB	WQFN	NKB	60	250	210.0	185.0	35.0
DS90UH926QSQX/NOPB	WQFN	NKB	60	2000	367.0	367.0	38.0

NKB0060B

PACKAGE OUTLINE

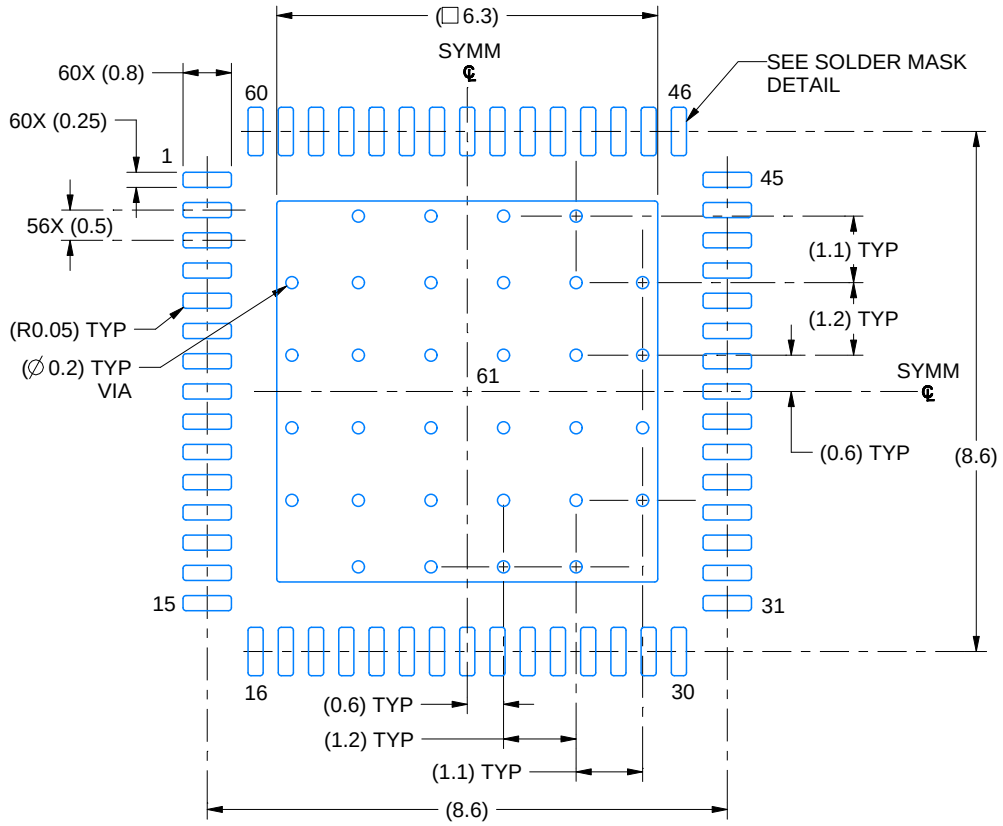
VQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

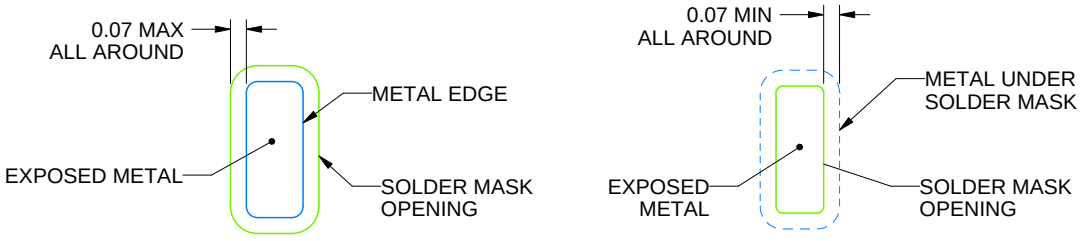


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

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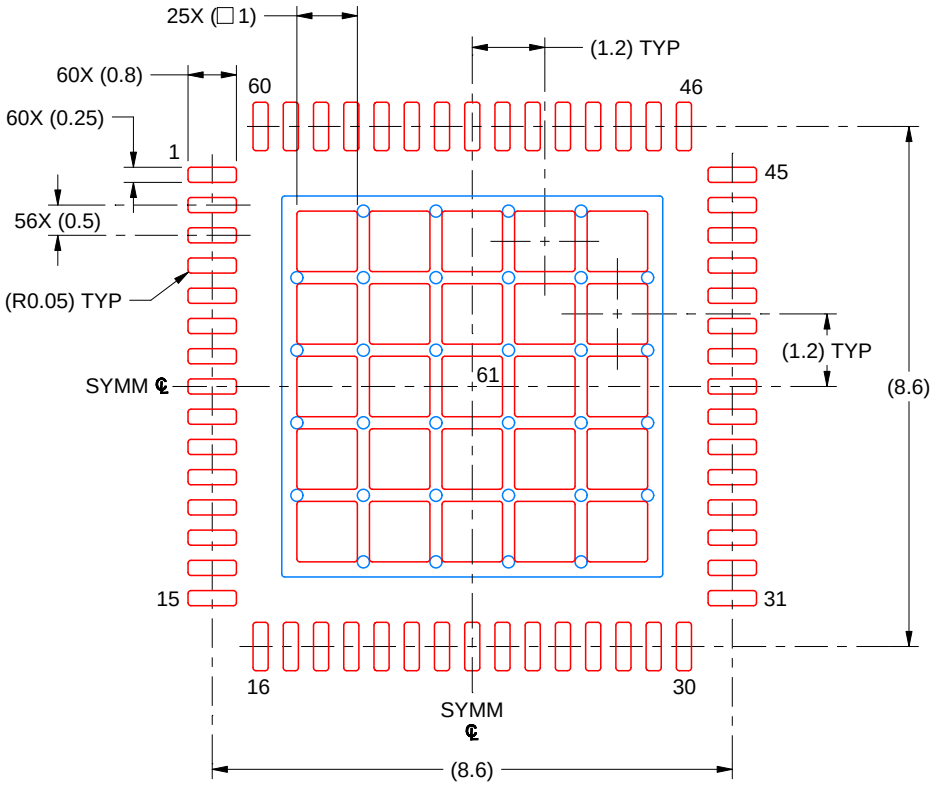
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 8X

EXPOSED PAD 61
63% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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