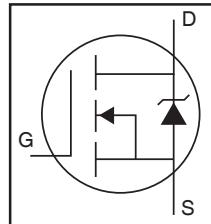


# AUIRFBA1405

## HEXFET® Power MOSFET

### Features

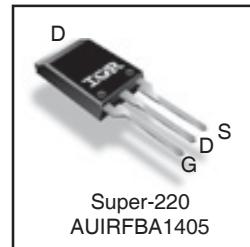
- Advanced Planar Technology
- Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Repetitive Avalanche Allowed up to  $T_{jmax}$
- Lead-Free, RoHS Compliant
- Automotive Qualified\*



$V_{(BR)DSS}$	<b>55V</b>
$R_{DS(on)}$ typ. max	<b>4.3mΩ</b>
	<b>5.0mΩ</b>
$I_D$ (Silicon Limited)	<b>174A<sup>⑥</sup></b>
$I_D$ (Package Limited)	<b>95A</b>

### Description

Specifically designed for Automotive applications, this Stripe Planar design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve low on-resistance per silicon area. This benefit combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in Automotive and a wide variety of other applications.



G	D	S
Gate	Drain	Source

### Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature ( $T_A$ ) is 25°C, unless otherwise specified.

	Parameter	Max.	Units
$I_D$ @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	174 <sup>⑥</sup>	A
$I_D$ @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	123 <sup>⑥</sup>	
$I_D$ @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Package Limited)	95	
$I_{DM}$	Pulsed Drain Current ①	680	
$P_D$ @ $T_C = 25^\circ\text{C}$	Power Dissipation	330	W
	Linear Derating Factor	2.2	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 20	V
$E_{AS}$	Single Pulse Avalanche Energy (Thermally Limited) ②	560	mJ
$I_{AR}$	Avalanche Current ①	See Fig.12a, 12b, 15, 16	A
$E_{AR}$	Repetitive Avalanche Energy ②		mJ
dv/dt	Peak Diode recovery dv/dt ③	5.0	V/ns
$T_J$	Operating Junction and	-40 to +175	°C
$T_{STG}$	Storage Temperature Range	-55 to +175	
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

### Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{θJC}$	Junction-to-Case ④	—	0.45	°C/W
$R_{θCS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{θJA}$	Junction-to-Ambient	—	58	

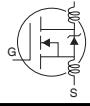
HEXFET® is a registered trademark of International Rectifier.

\*Qualification standards can be found at <http://www.irf.com/>

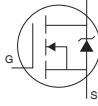
Static Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	55	—	—	V	$V_{\text{GS}} = 0\text{V}$ , $I_D = 250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}/\Delta T_J}$	Breakdown Voltage Temp. Coefficient	—	0.057	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D = 1\text{mA}$
$R_{\text{DS}(\text{on})}$	Static Drain-to-Source On-Resistance	—	4.3	5.0	$\text{m}\Omega$	$V_{\text{GS}} = 10\text{V}$ , $I_D = 101\text{A}$ ④
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{\text{DS}} = 10\text{V}$ , $I_D = 250\mu\text{A}$
$g_{\text{fs}}$	Forward Transconductance	69	—	—	S	$V_{\text{DS}} = 25\text{V}$ , $I_D = 110\text{A}$
$I_{\text{DSS}}$	Drain-to-Source Leakage Current	—	—	20	$\mu\text{A}$	$V_{\text{DS}} = 55\text{V}$ , $V_{\text{GS}} = 0\text{V}$
		—	—	250	$\mu\text{A}$	$V_{\text{DS}} = 44\text{V}$ , $V_{\text{GS}} = 0\text{V}$ , $T_J = 150^\circ\text{C}$
$I_{\text{GSS}}$	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{\text{GS}} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-200	nA	$V_{\text{GS}} = -20\text{V}$

Dynamic Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$Q_g$	Total Gate Charge	—	170	260	nC	$I_D = 101\text{A}$
$Q_{\text{gs}}$	Gate-to-Source Charge	—	44	66		$V_{\text{DS}} = 44\text{V}$
$Q_{\text{gd}}$	Gate-to-Drain ("Miller") Charge	—	62	93		$V_{\text{GS}} = 10\text{V}$ ④
$t_{\text{d}(\text{on})}$	Turn-On Delay Time	—	13	—	ns	$V_{\text{DD}} = 38\text{V}$
$t_r$	Rise Time	—	190	—		$I_D = 110\text{A}$
$t_{\text{d}(\text{off})}$	Turn-Off Delay Time	—	130	—		$R_G = 1.1\ \Omega$
$t_f$	Fall Time	—	110	—		$V_{\text{GS}} = 10\text{V}$ ④
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{\text{iss}}$	Input Capacitance	—	5480	—	pF	$V_{\text{GS}} = 0\text{V}$
$C_{\text{oss}}$	Output Capacitance	—	1210	—		$V_{\text{DS}} = 25\text{V}$
$C_{\text{rss}}$	Reverse Transfer Capacitance	—	280	—		$f = 1.0\text{MHz}$ , See Fig.5
$C_{\text{oss}}$	Output Capacitance	—	5210	—		$V_{\text{GS}} = 0\text{V}$ , $V_{\text{DS}} = 1.0\text{V}$ , $f = 1.0\text{MHz}$
$C_{\text{oss}}$	Output Capacitance	—	900	—		$V_{\text{GS}} = 0\text{V}$ , $V_{\text{DS}} = 44\text{V}$ , $f = 1.0\text{MHz}$
$C_{\text{oss eff.}}$	Effective Output Capacitance ⑤	—	1500	—		$V_{\text{GS}} = 0\text{V}$ , $V_{\text{DS}} = 0\text{V}$ to $44\text{V}$

## Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_s$	Continuous Source Current (Body Diode)	—	—	174 ⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
	Pulsed Source Current (Body Diode) ①	—	—	680		
$V_{\text{SD}}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}$ , $I_s = 101\text{A}$ , $V_{\text{GS}} = 0\text{V}$ ④
$t_{\text{rr}}$	Reverse Recovery Time	—	88	130	ns	$T_J = 25^\circ\text{C}$ , $I_F = 101\text{A}$
$Q_{\text{rr}}$	Reverse Recovery Charge	—	250	380	nC	$\text{di}/\text{dt} = 100\text{A}/\mu\text{s}$ ④
$t_{\text{on}}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

## Notes:

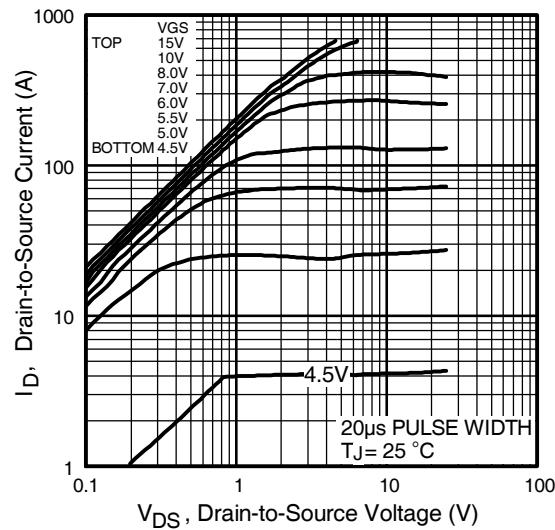
- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.11\text{mH}$   
 $R_G = 25\Omega$ ,  $I_{AS} = 101\text{A}$ . (See Figure 12).
- ③  $I_{SD} \leq 101\text{A}$ ,  $\text{di}/\text{dt} \leq 210\text{A}/\mu\text{s}$ ,  $V_{\text{DD}} \leq V_{(\text{BR})\text{DSS}}$ ,  $T_J \leq 175^\circ\text{C}$ .
- ④ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{\text{oss eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{\text{oss}}$  while  $V_{\text{DS}}$  is rising from 0 to 80%  $V_{\text{DSS}}$ . Refer to AN-1001.
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 95A.
- ⑦ Limited by  $T_{\text{Jmax}}$ , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑧  $R_\theta$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .

**Qualification Information<sup>†</sup>**

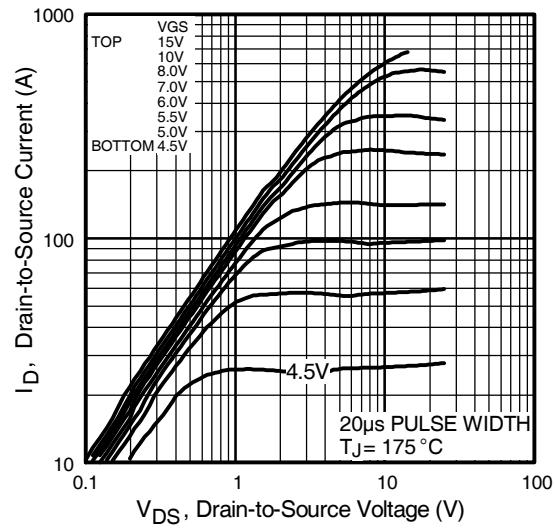
		Automotive (per AEC-Q101)	
<b>Qualification Level</b>		Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
<b>Moisture Sensitivity Level</b>		TO-220	N/A
<b>ESD</b>	Machine Model	Class M4 (+/- 600V) <sup>††</sup> AEC-Q101-002	
	Human Body Model	Class H2 (+/- 4000V) <sup>††</sup> AEC-Q101-001	
	Charged Device Model	Class C5 (+/- >2000V) <sup>††</sup> AEC-Q101-005	
<b>RoHS Compliant</b>		Yes	

<sup>†</sup> Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/>

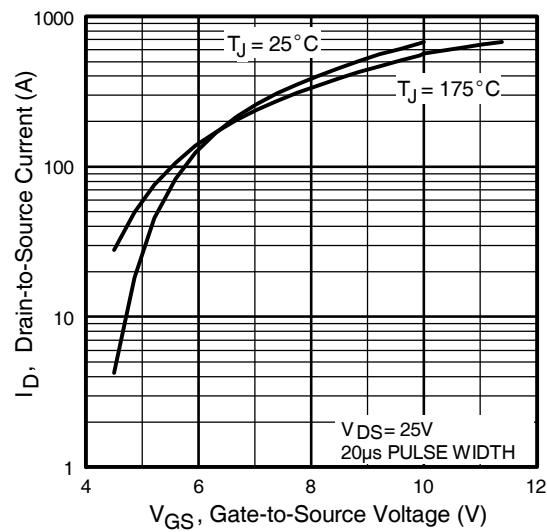
<sup>††</sup> Highest passing voltage.



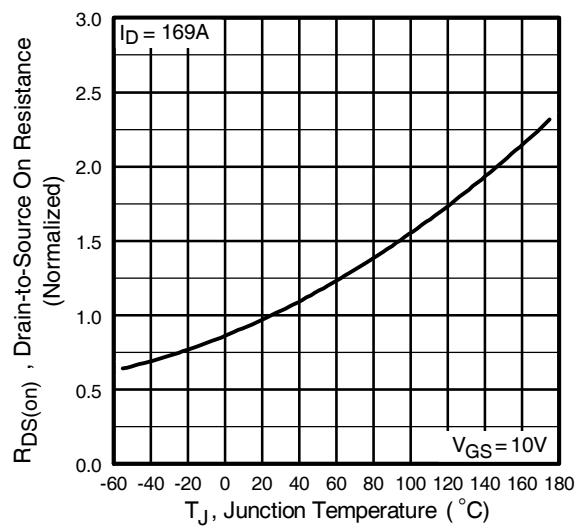
**Fig 1.** Typical Output Characteristics



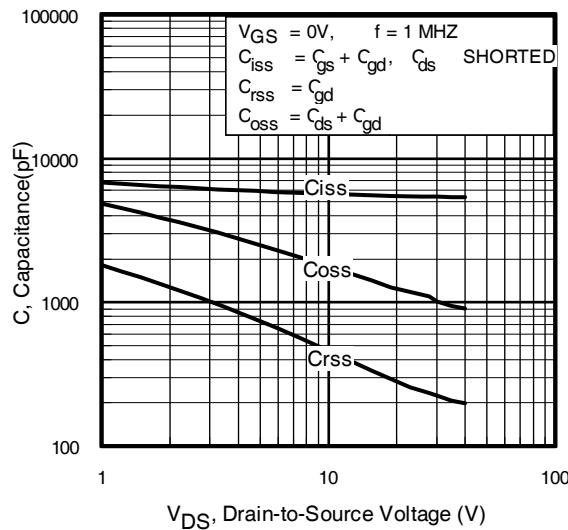
**Fig 2.** Typical Output Characteristics



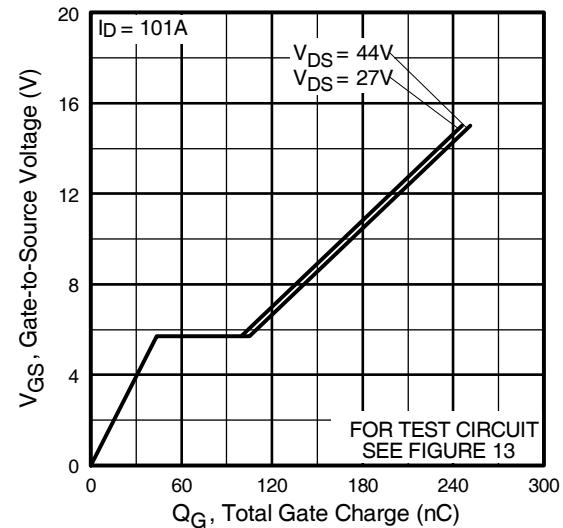
**Fig 3.** Typical Transfer Characteristics



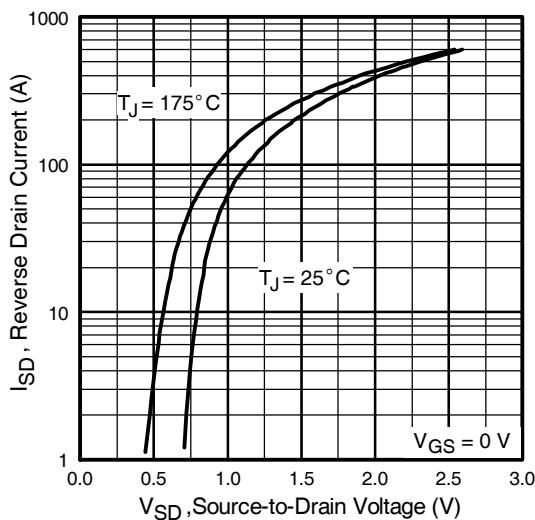
**Fig 4.** Normalized On-Resistance  
 Vs. Temperature



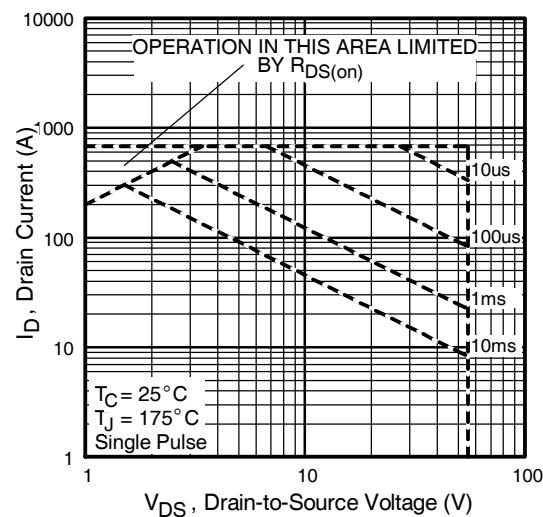
**Fig 5.** Typical Capacitance Vs.  
Drain-to-Source Voltage



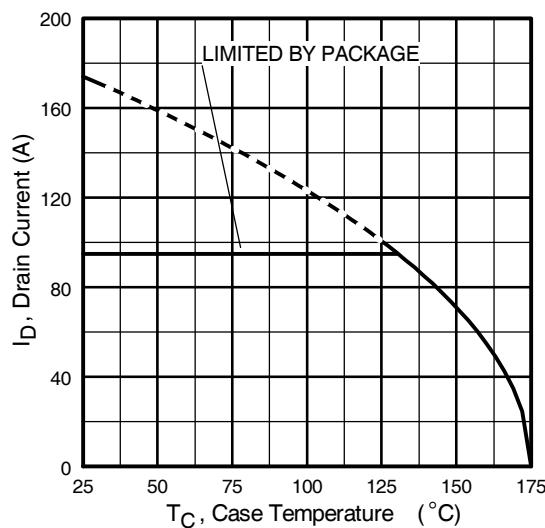
**Fig 6.** Typical Gate Charge Vs.  
Gate-to-Source Voltage



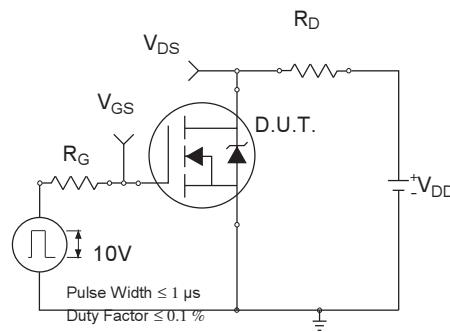
**Fig 7.** Typical Source-Drain Diode  
Forward Voltage



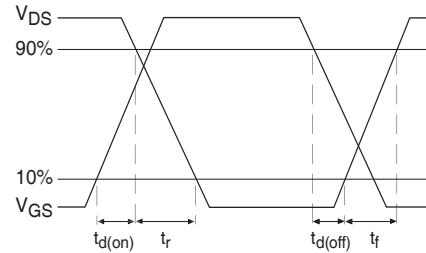
**Fig 8.** Maximum Safe Operating Area



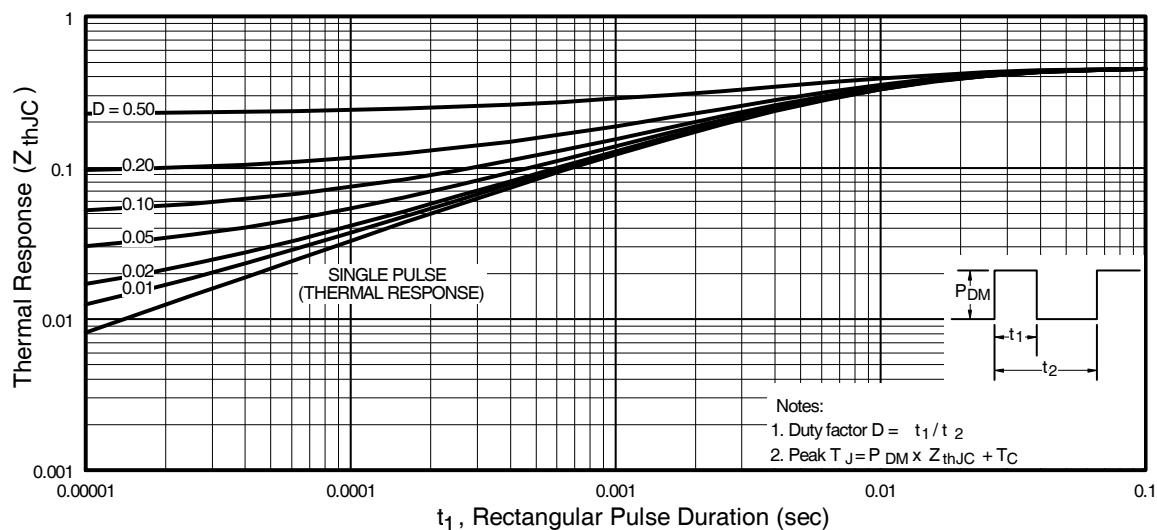
**Fig 9.** Maximum Drain Current Vs.  
Case Temperature



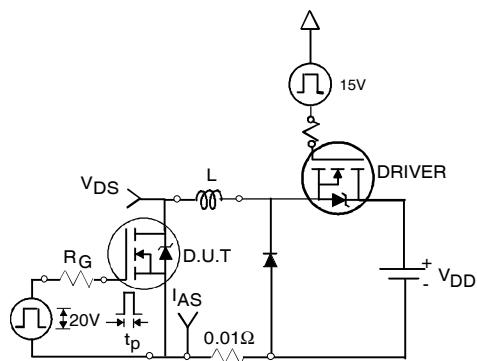
**Fig 10a.** Switching Time Test Circuit



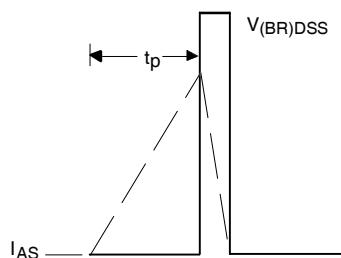
**Fig 10b.** Switching Time Waveforms



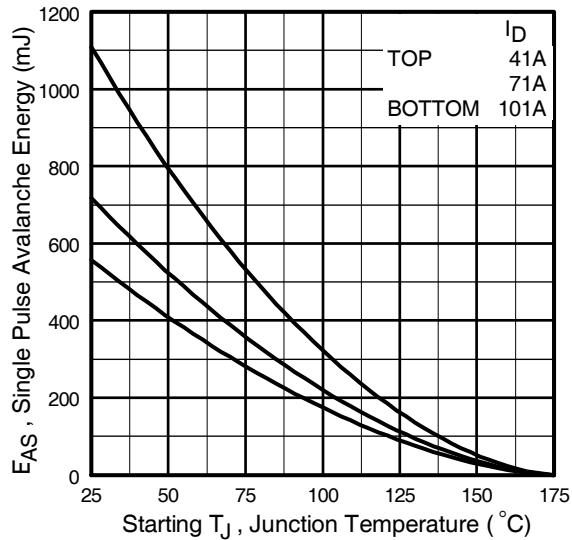
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



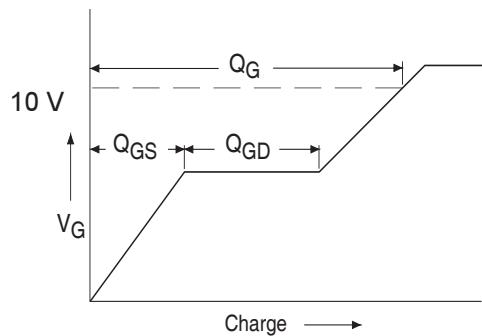
**Fig 12a.** Unclamped Inductive Test Circuit



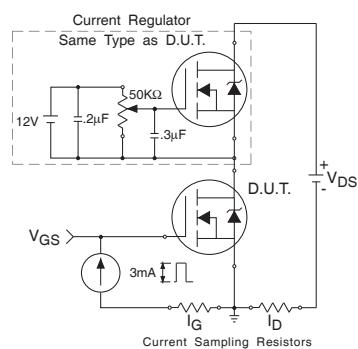
**Fig 12b.** Unclamped Inductive Waveforms



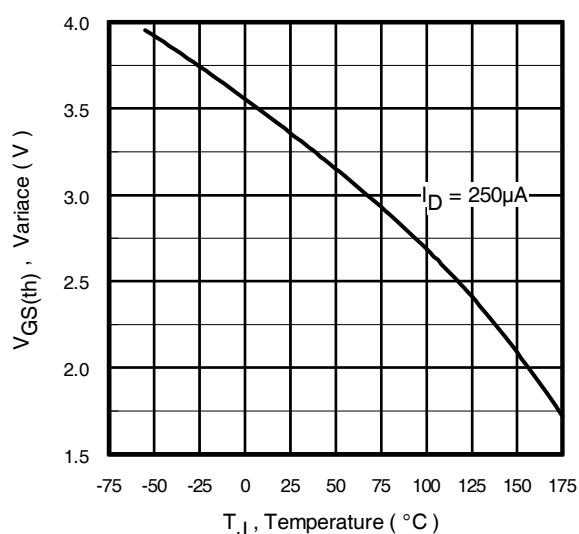
**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



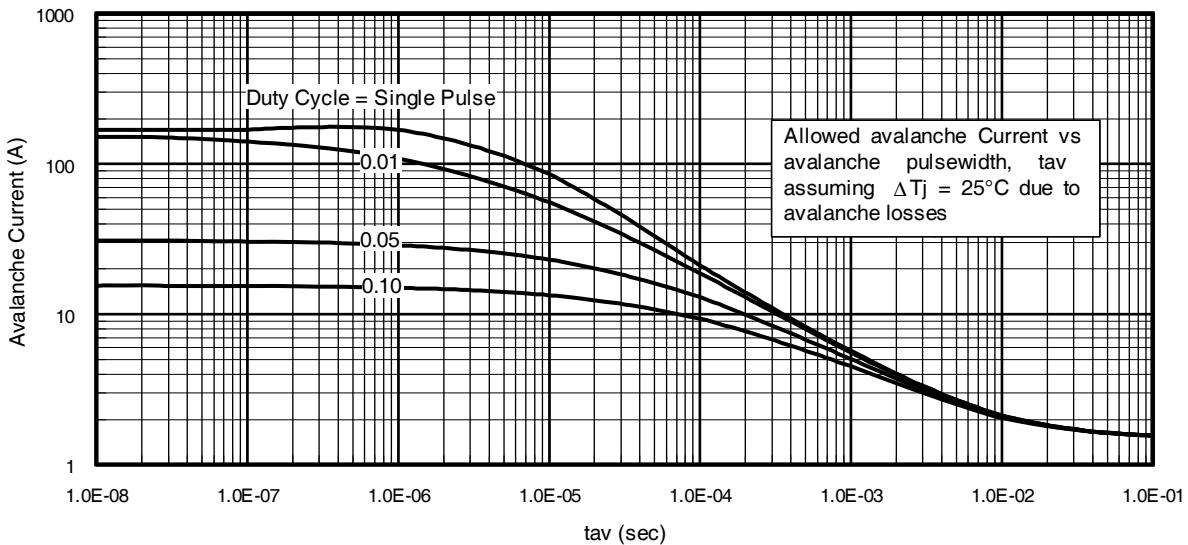
**Fig 13a.** Basic Gate Charge Waveform



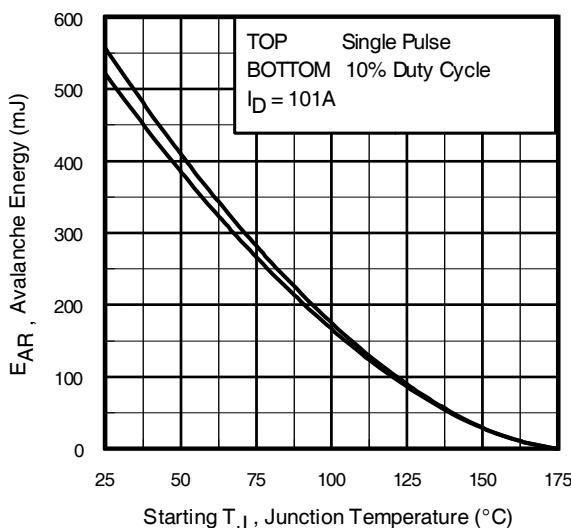
**Fig 13b.** Gate Charge Test Circuit  
[www.irf.com](http://www.irf.com)



**Fig 14.** Threshold Voltage Vs. Temperature



**Fig 15.** Typical Avalanche Current Vs.Pulsewidth



**Fig 16.** Maximum Avalanche Energy Vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 15, 16:**  
(For further info, see AN-1005 at [www.irf.com](http://www.irf.com))

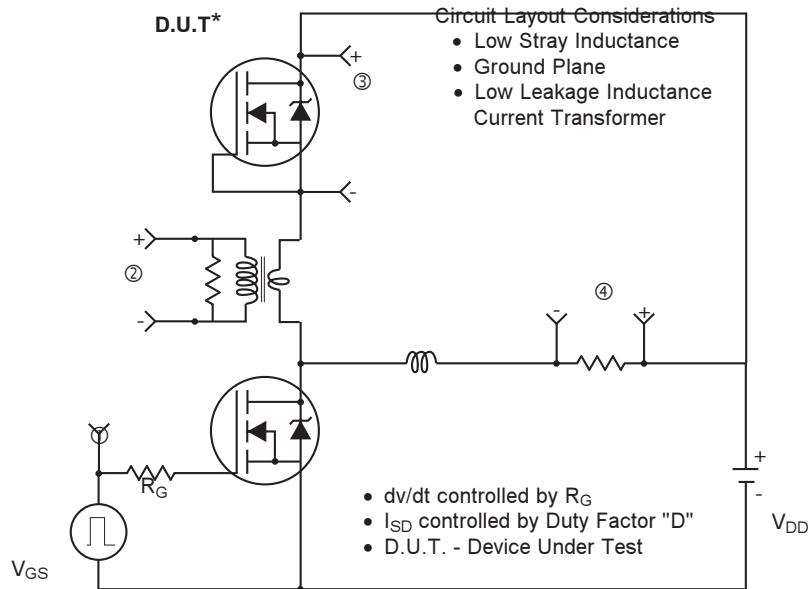
1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as  $25^\circ\text{C}$  in Figure 15, 16).
- $t_{av}$  = Average time in avalanche.
- $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$
- $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see figure 11)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

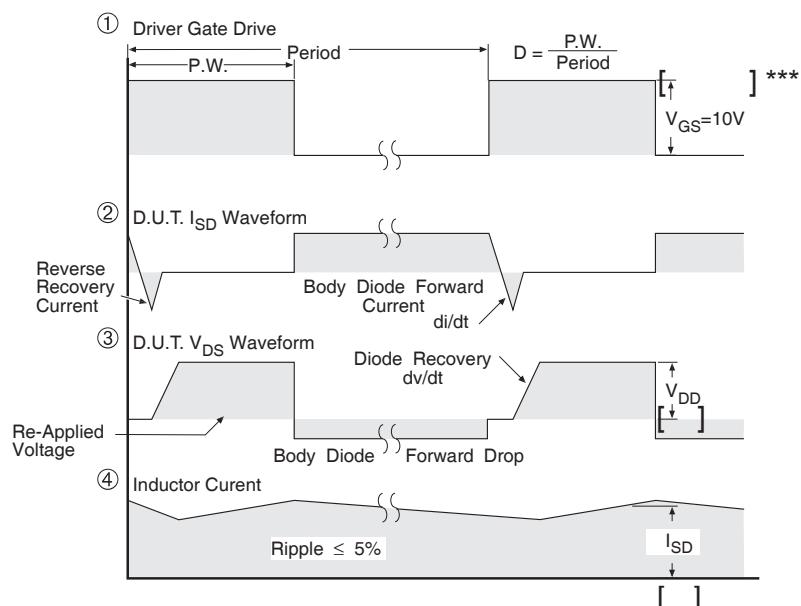
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

**Peak Diode Recovery dv/dt Test Circuit**



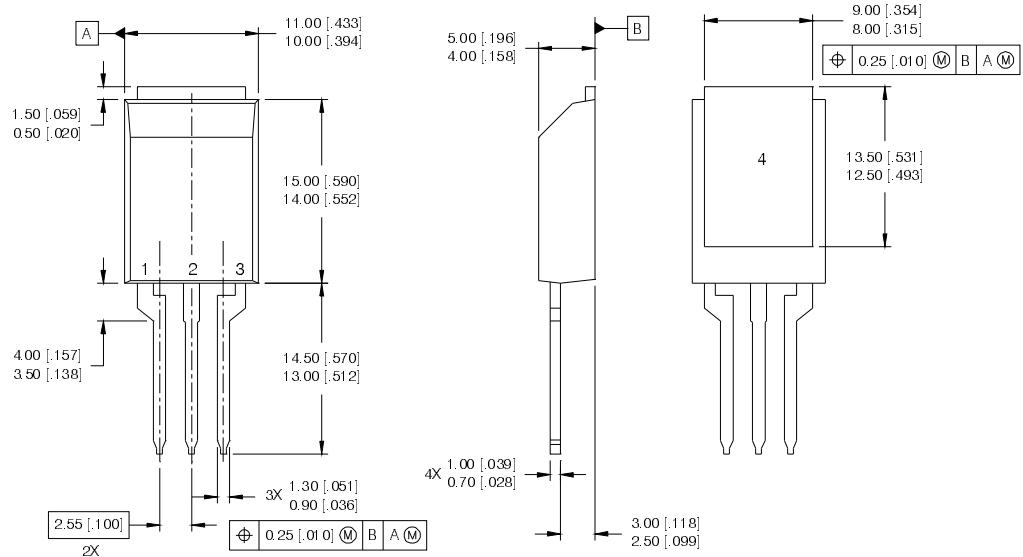
\* Reverse Polarity of D.U.T for P-Channel



\*\*\*  $V_{GS} = 5.0V$  for Logic Level and 3V Drive Devices

**Fig 17.** For N-channel HEXFET® power MOSFETs

## Super-220™ Package Outline



## NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-273AA.

## LEAD ASSIGNMENTS

## MOSFET

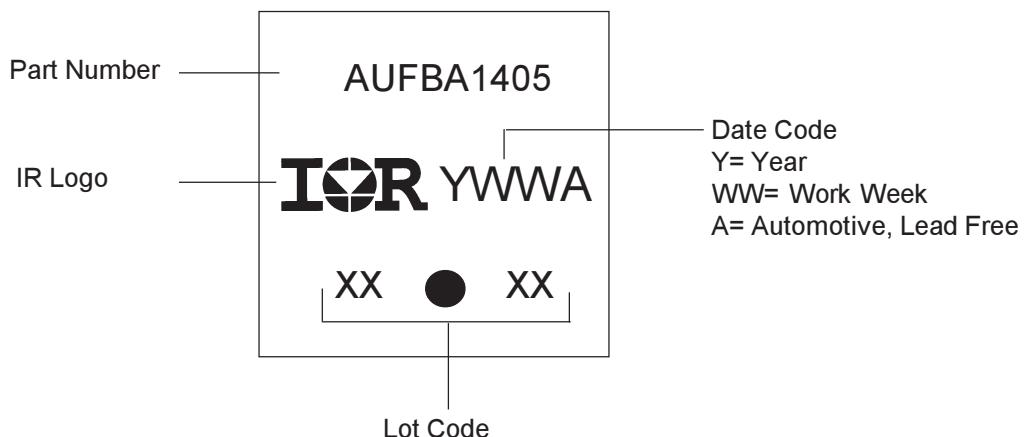
- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE
- 4 - DRAIN

## IGBT

- 1 - GATE
- 2 - COLLECTOR
- 3 - Emitter
- 4 - COLLECTOR

Super-220™ not recommended for surface mount application

## Super-220 Part Marking Information



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Ordering Information**

<b>Base part number</b>	<b>Package Type</b>	<b>Standard Pack</b>		<b>Complete Part Number</b>
		<b>Form</b>	<b>Quantity</b>	
AUIRFBA1405	Super-220	Tube	50	AUIRFBA1405

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