SaRonix-eCera™

ASSP XO™

Application Specific Crystal Oscillator 7.0 x 5.0mm

3.3V HCSL Low Jitter 100MHz PCIe® 2.0 XO

SHPCIE100

7.0 x 5.0mm Ceramic SMD

ASSP XO™ for Networking

Product Features

- Provides 100 MHz HCSL output for interfacing to standard PCIe® devices
- Very low PCIe 2.0 jitter - 1.8ps RMS (typ.)
- Thicker crystal for improved reliability
- Pb-free & RoHS compliant
- Industrial temperature range

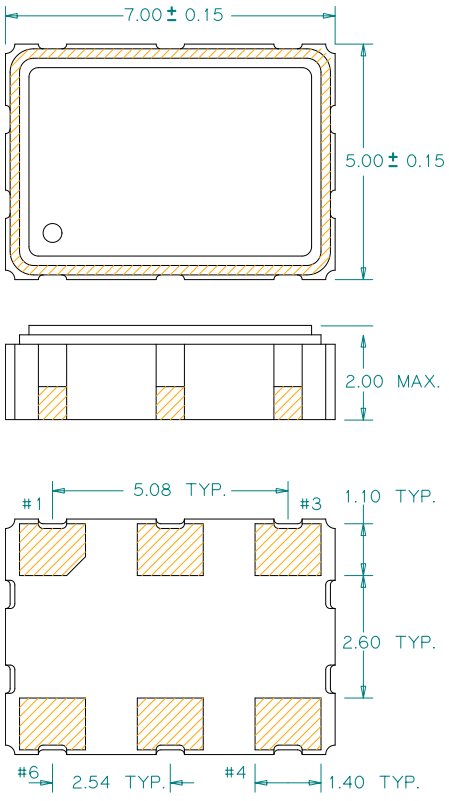
Product Description

The SHPCIE100 3.3V crystal clock oscillator achieves superb jitter for PCIe® 1.0 & 2.0 applications. The output clock signal, generated internally with a patented oscillator design, is compatible with HCSL logic levels. The device, available on tape and reel, is contained in a 7.0 x 5.0mm surface-mount ceramic package.

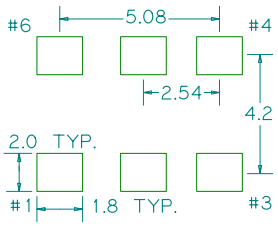
Applications

- Server
- Network Switch/Router
- Telecom Switch
- Media Box
- Graphics Card
- Host Bus Adapter

Package:



Recommended Land Pattern:



Pin Functions:

Pin	Function
1	OE Function
2	N/C
3	Ground
4	OUT
5	$\overline{\text{OUT}}$
6	V_{CC}

*Extended high frequency power decoupling is recommended (see test circuit for minimum recommendation). To ensure optimal performance, do not route RF traces beneath the package.

Part Ordering Information:

SHPCIE100

Electrical Performance

Parameter	Min.	Typ.	Max.	Units	Notes
Output Frequency		100		MHz	
Supply Voltage	2.97	3.30	3.63	V	
Supply Current, Output Enabled			40	mA	
Supply Current, Output Disabled			15	mA	
Frequency Stability			±50	ppm	See Note 1 below
Operating Temperature Range	-40		+85	°C	Industrial
Output Logic 0, V_{OL}	-0.15	0		V	
Output Logic 1, V_{OH}	0.66	0.7	0.9	V	
Output Load	R_s = 33Ω, R_p = 50Ω, C_L = 2pF				output requires termination
Duty Cycle	45		55	%	Measured 50% of waveform
Rise and Fall Time			0.7	ns	Maximum measured from V_{OL} = 0.175V to V_{OH} = 0.525V
Jitter, Phase RMS (1-σ)		1.8	2.5	ps	As defined by PCI-SIG for PCIe® 2.0 reference clock
Jitter, pk–pk		27	40	ps	100,000 random periods

Notes:
1. Stability includes all combinations of operating temperature, load changes, rated input (supply) voltage changes, initial calibration tolerance (25°C), aging (5 year at 40°C average effective ambient temperature), shock and vibration.
2. For specifications othere than those listed, please contact sales.

Output Enable / Disable Function

Parameter	Min.	Typ.	Max.	Units	Notes
Input Voltage (pin 1), Output Enable	2.2			V	or open
Input Voltage (pin 1), Output Disable (low power standby)			0.8	V	Outputs disabled to Hi-Z
Output Disable Delay			200	ns	
Output Enable Delay			10	ms	

Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Units	Notes
Storage Temperature	-55		+125	°C	

For the latest product information visit: http://www.pericom.com/products/timing/oscillators/SHPCIE100/

For test circuit go to: http://www.pericom.com/pdf/sre/tc_hcsl.pdf

For soldering reflow profile and reliability test ratings go to: http://www.pericom.com/pdf/sre/reflow.pdf

For typical phase noise go to: http://www.pericom.com/pdf/sre/pn_SHPCIE100.pdf

For tape and reel information go to: http://www.pericom.com/pdf/sre/tr_7050.pdf

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