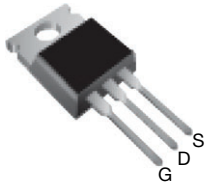
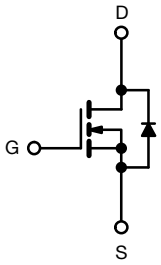
Power MOSFET

TO-220AB





N-Channel MOSFET

FEATURES

- Low figure-of-merit R_{on} x Q_g
- 100 % avalanche tested
- High peak current capability
- dv/dt ruggedness
- Improved t_{rr}/Q_{rr}
- Improved gate charge
- High power dissipations capability
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Available

RoHS*

Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	560	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.225
Q_g max. (nC)	76	
Q_{gs} (nC)	21	
Q_{gd} (nC)	29	
Configuration	Single	

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free and halogen-free	SiHP18N50C-E3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V_{DS}	500	V
Gate-source voltage			V_{GS}	± 30	
Continuous drain current (T_J = 150 °C) [a]	V_{GS} at 10 V	T_C = 25 °C	I_D	18	A
		T_C = 100 °C		11	
Pulsed drain current [b]			I_{DM}	72	
Linear derating factor				1.8	W/°C
Single pulse avalanche energy [c]			E_{AS}	361	mJ
Maximum power dissipation			P_D	223	W
Reverse diode dv/dt [d]			dv/dt	5	V/ns
Operating junction and storage temperature range			T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) [d]	For 10 s			300	

Notes

a. Drain current limited by maximum junction temperature
b. Repetitive rating; pulse width limited by maximum junction temperature
c. V_{DD} = 50 V, starting T_J = 25 °C, L = 2.5 mH, R_g = 25 Ω, I_{AS} = 17 A
d. $I_{SD} \leq$ 18 A, di/dt ≤ 380 A/µs, $V_{DD} \leq V_{DS}$, $T_J \leq$ 150 °C
e. 1.6 mm from case

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	62	°C/W
Maximum junction-to-case (drain)	R_{thJC}	-	0.56	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	500	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA	-	0.6	-	V/°C
Gate-source threshold voltage (N)	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	3.0	-	5.0	V
Gate-source leakage	I_{GSS}	V_{GS} = ± 30 V	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 500 V, V_{GS} = 0 V	-	-	25	µA
		V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125 °C	-	-	250	
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS} = 10 V; I_D = 10 A	-	0.225	0.270	Ω
Forward transconductance [a]	g_{fs}	V_{DS} = 50 V, I_D = 10 A	-	6.4	-	S
Dynamic						
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	-	2451	2942	pF
Output capacitance	C_{oss}		-	300	360	
Reverse transfer capacitance	C_{rss}		-	26	32	
Total gate charge	Q_g	V_{GS} = 10 V; I_D = 18 A, V_{DS} = 400 V	-	65	76	nC
Gate-source charge	Q_{gs}		-	21	-	
Gate-drain charge	Q_{gd}		-	29	-	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 250 V, I_D = 18 A, V_{GS} = 10 V, R_g = 7.5 Ω	-	80	-	ns
Rise time	t_r		-	27	-	
Turn-off delay time	$t_{d(off)}$		-	32	-	
Fall time	t_f		-	44	-	
Gate input resistance	R_g	f = 1 MHz, open drain	-	1.1	-	Ω
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	18	A
Pulsed diode forward current	I_{SM}		-	-	72	
Diode forward voltage	V_{SD}	T_J = 25 °C, I_S = 18 A, V_{GS} = 0 V	-	-	1.5	V
Reverse recovery time	t_{rr}	T_J = 25 °C, I_F = I_S, di/dt = 100 A/µs, V_R = 35 V	-	503	-	ns
Reverse recovery charge	Q_{rr}		-	6.7	-	µC
Reverse recovery current	I_{RRM}		-	30	-	A

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

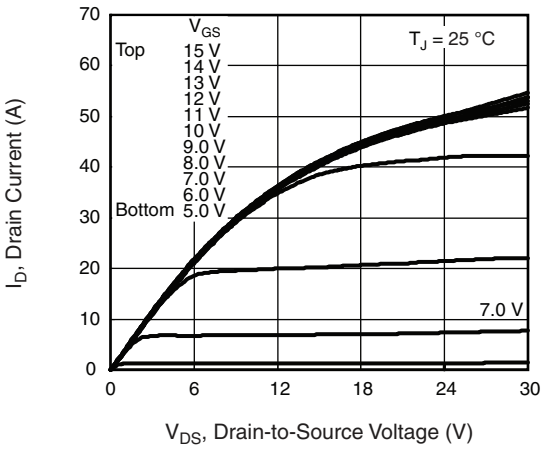


Fig. 1 - Typical Output Characteristics, T_C = 150 °C

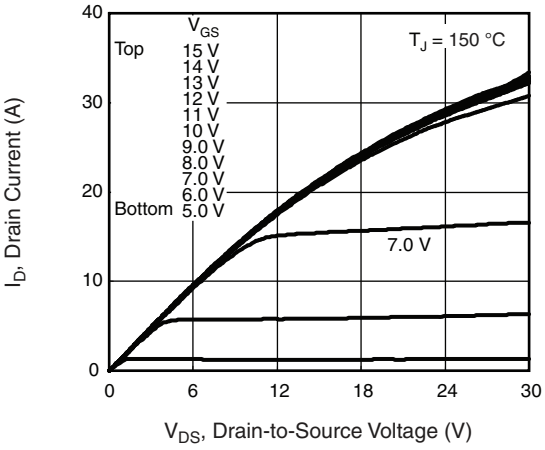


Fig. 2 - Typical Output Characteristics, T_C = 150 °C

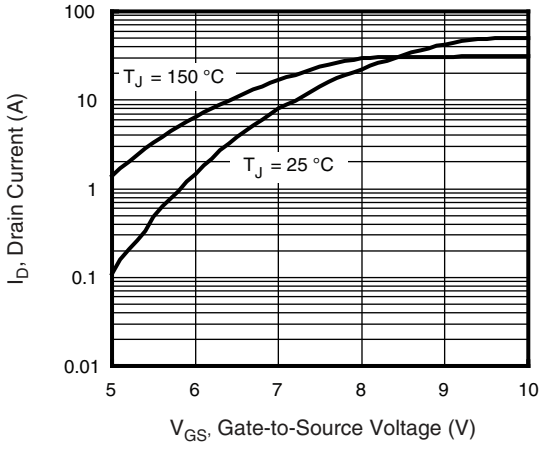


Fig. 3 - Typical Transfer Characteristics

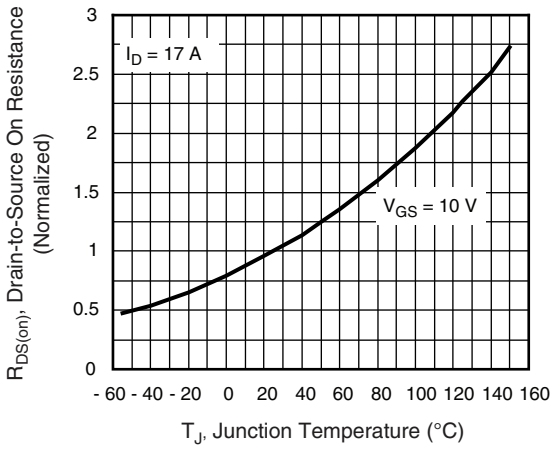


Fig. 4 - Normalized On-Resistance vs. Temperature

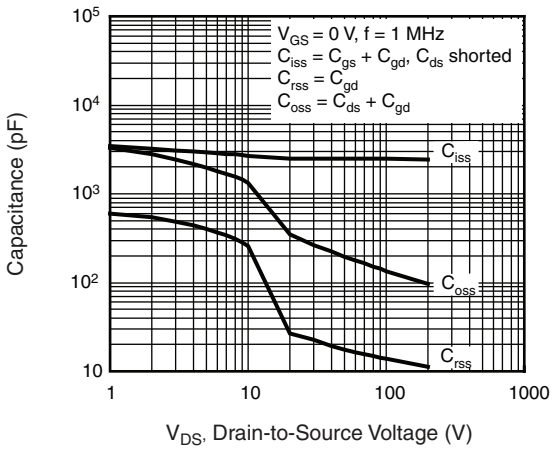


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

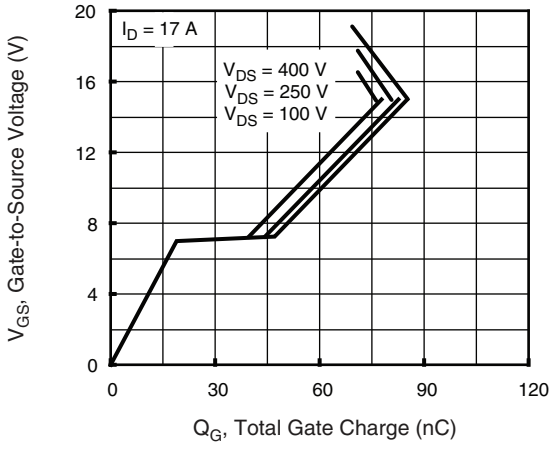


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

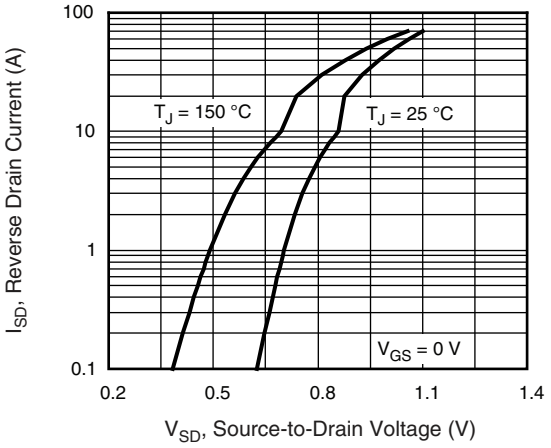


Fig. 7 - Typical Source-Drain Diode Forward Voltage

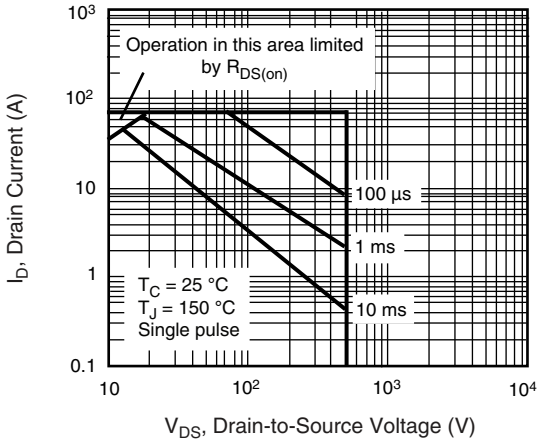


Fig. 8 - Maximum Safe Operating Area

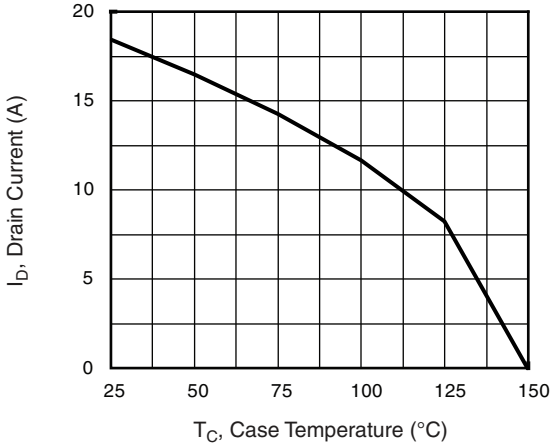


Fig. 9 - Maximum Drain Current vs. Case Temperature

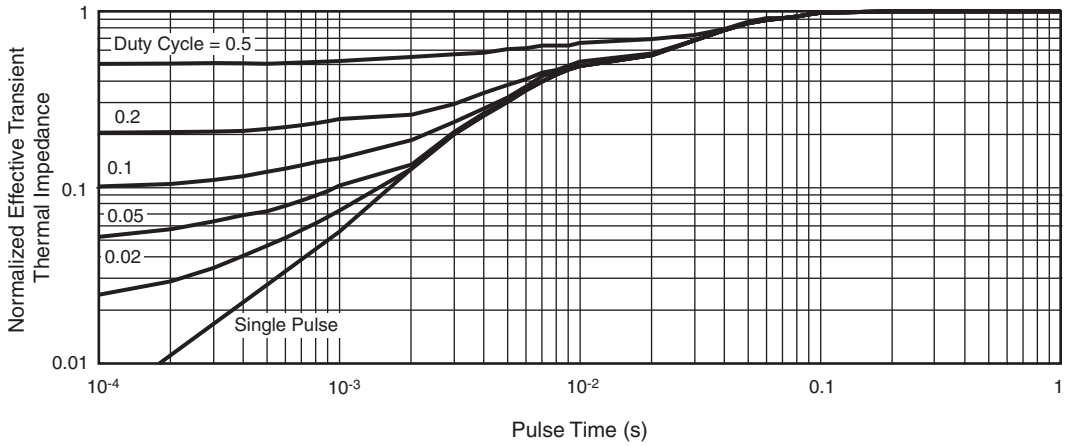


Fig. 10 - Normalized Thermal Transient Impedance, Junction-to-Case

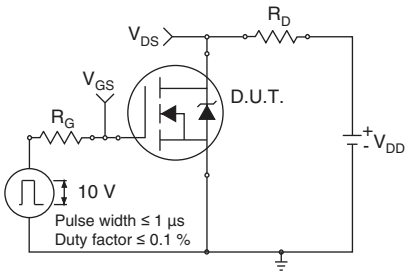


Fig. 11 - Switching Time Test Circuit

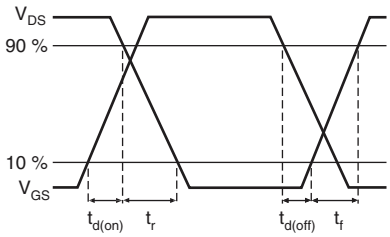


Fig. 12 - Switching Time Waveforms

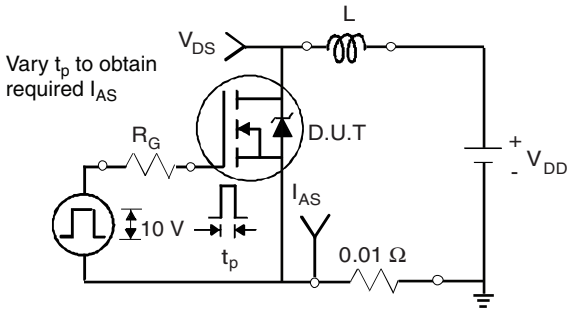


Fig. 13 - Unclamped Inductive Test Circuit

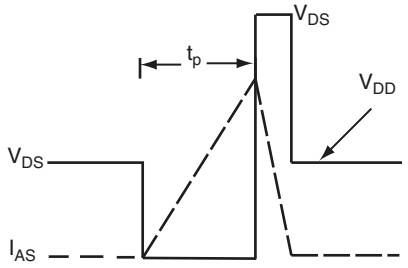


Fig. 14 - Unclamped Inductive Waveforms

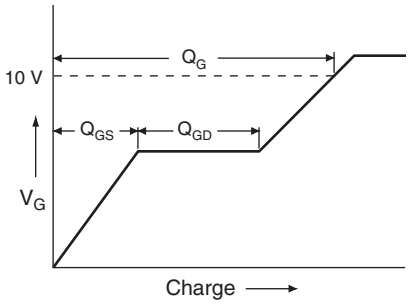


Fig. 15 - Basic Gate Charge Waveform

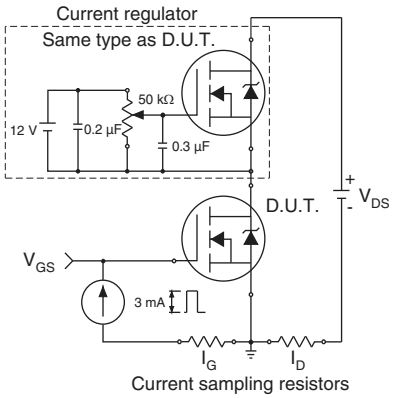
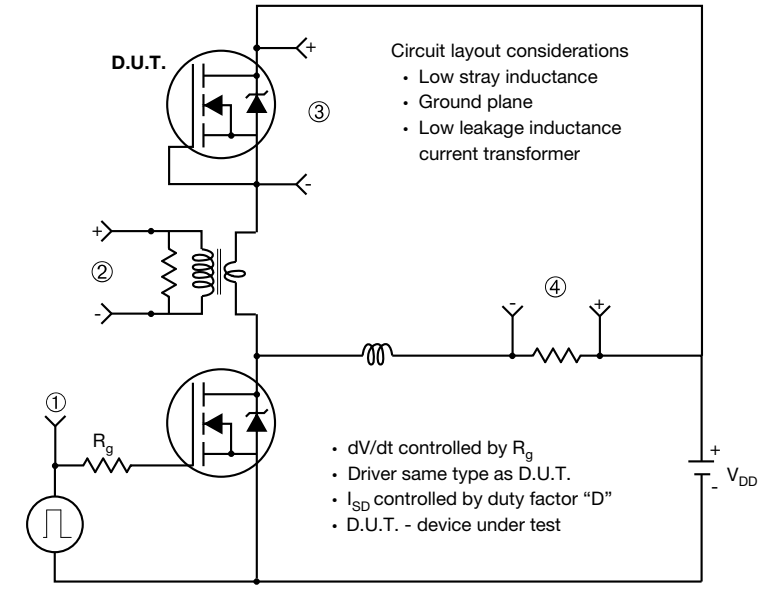
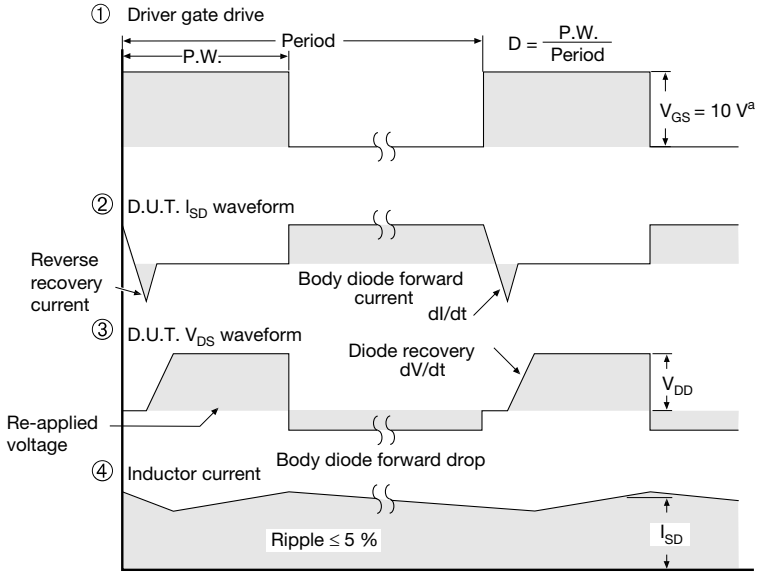


Fig. 16 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



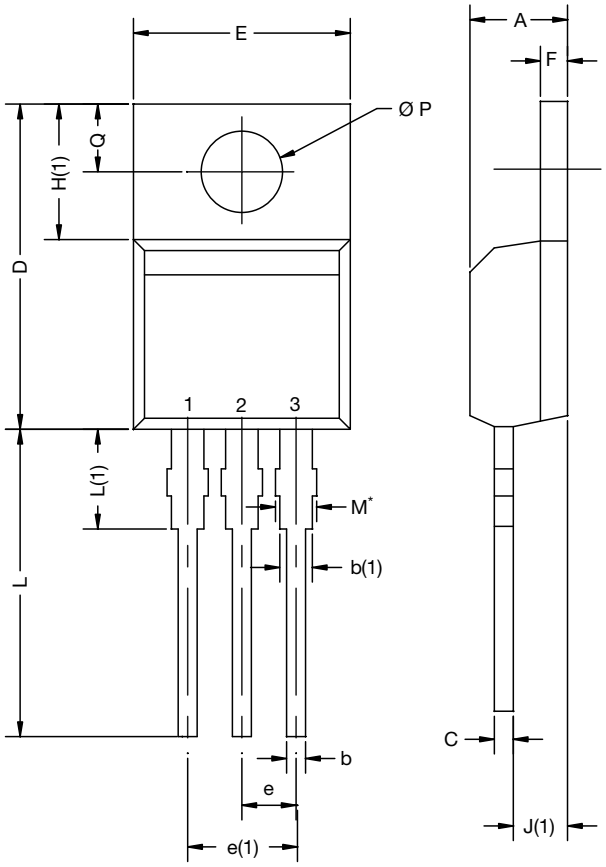


Note

a. V_{GS} = 5 V for logic level devices

Fig. 17 - For N-Channel

TO-220-1

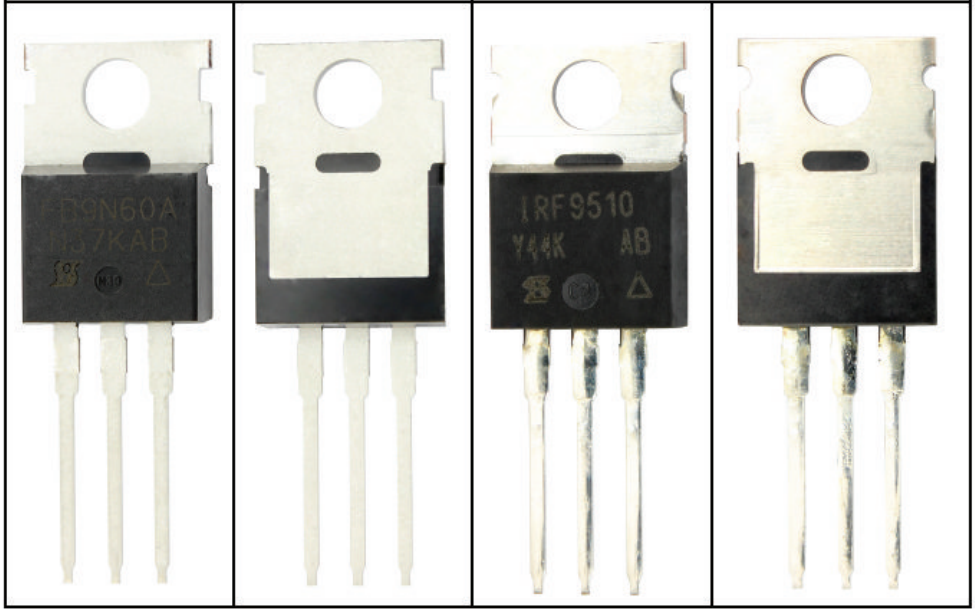


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
c	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
E	9.96	10.52	0.392	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
Ø P	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118
ECN: X15-0364-Rev. C, 14-Dec-15 DWG: 6031				

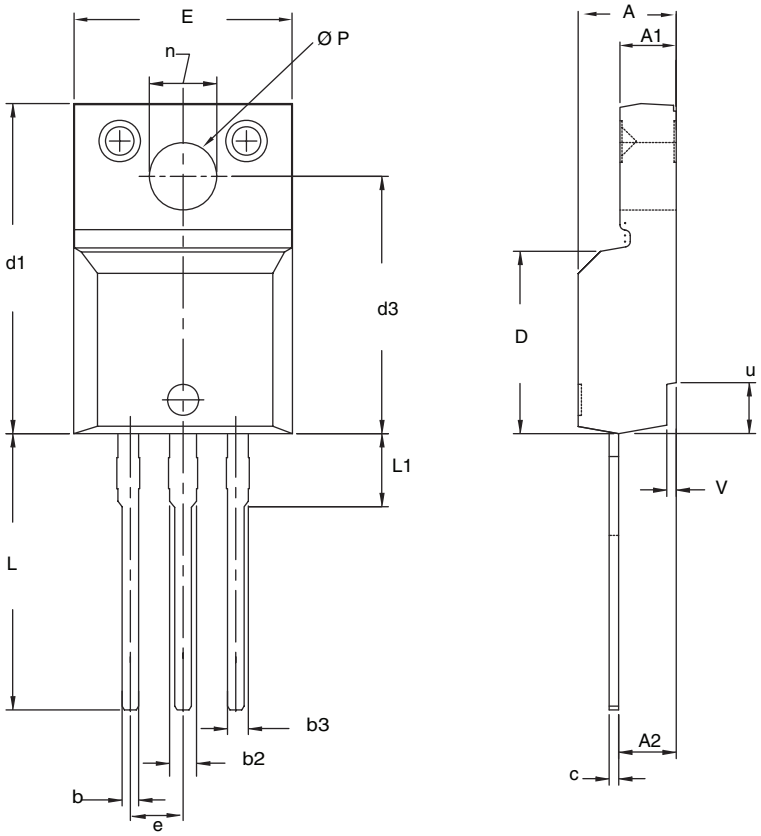
Note

- M* = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM

Package Picture	
ASE	Xi'an



TO-220 FULLPAK (HIGH VOLTAGE)



	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
Ø P	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
v	0.400	0.500	0.016	0.020
ECN: X09-0126-Rev. B, 26-Oct-09 DWG: 5972				

Notes

1. To be used only for process drawing.
2. These dimensions apply to all TO-220, FULLPAK leadframe versions 3 leads.
3. All critical dimensions should C meet $C_{pk} > 1.33$.
4. All dimensions include burrs and plating thickness.
5. No chipping or package damage.

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