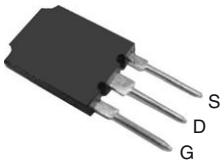
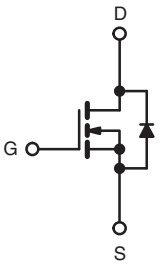
# D Series Power MOSFET

| PRODUCT SUMMARY | | |
|---|---|---|
| $V_{DS}$ (V) at $T_J$ max. | 550 | |
| $R_{DS(on)}$ max. at 25 °C (Ω) | $V_{GS}$ = 10 V | 0.130 |
| $Q_g$ max. (nC) | 125 | |
| $Q_{gs}$ (nC) | 23 | |
| $Q_{gd}$ (nC) | 37 | |
| Configuration | Single | |

Super-247




N-Channel MOSFET

## FEATURES

- Optimal Design
  - Low Area specific On-Resistance
  - Low Input Capacitance ($C_{iss}$)
  - Reduced Capacitive Switching Losses
  - High Body Diode Ruggedness
  - Avalanche Energy Rated ($U_{IS}$)
- Optimal Efficiency and Operation
  - Low Cost
  - Simple Gate Drive Circuitry
  - Low Figure-Of-Merit (FOM): $R_{on}$ x $Q_g$
  - Fast Switching
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT

## APPLICATIONS

- Consumer Electronics
  - Displays (LCD or Plasma TV
- Server and Telecom Power Supplies
  - SMPS
- Industrial
  - Welding, Induction Heating, Motor Drives
- Battery Chargers

| ORDERING INFORMATION | |
|---|---|
| Package | Super-247 |
| Lead (Pb)-free | SiHS36N50D-E3 |

**ABSOLUTE MAXIMUM RATINGS** ($T_C$ = 25 °C, unless otherwise noted)

| PARAMETER | | | SYMBOL | LIMIT | UNIT |
|---|---|---|---|---|---|
| Drain-Source Voltage | | | $V_{DS}$ | 500 | V |
| Gate-Source Voltage | | | $V_{GS}$ | ± 30 | |
| Gate-Source Voltage AC (f > 1 Hz) | | | | 30 | |
| Continuous Drain Current ($T_J$ = 150 °C) | $V_{GS}$ at 10 V | $T_C$ = 25 °C | $I_D$ | 36 | A |
| | | $T_C$ = 100 °C | | 23 | |
| Pulsed Drain Current[a] | | | $I_{DM}$ | 112 | |
| Linear Derating Factor | | | | 3.6 | W/°C |
| Single Pulse Avalanche Energy[b] | | | $E_{AS}$ | 332 | mJ |
| Maximum Power Dissipation | | | $P_D$ | 446 | W |
| Operating Junction and Storage Temperature Range | | | $T_J$, $T_{stg}$ | - 55 to + 150 | °C |
| Drain-Source Voltage Slope | $T_J$ = 125 °C | | dV/dt | 24 | V/ns |
| Reverse Diode dV/dt[d] | | | | 0.1 | |
| Soldering Recommendations (Peak Temperature) | for 10 s | | | 300[c] | °C |

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature.
b. $V_{DD}$ = 50 V, starting $T_J$ = 25 °C, L = 2.3 mH, $R_g$ = 25 Ω, $I_{AS}$ = 17 A.
c. 1.6 mm from case.
d. $I_{SD} \leq I_D$, starting $T_J$ = 25 °C.

| THERMAL RESISTANCE RATINGS | | | | |
|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TYP.** | **MAX.** | **UNIT** |
| Maximum Junction-to-Ambient | $R_{thJA}$ | - | 40 | °C/W |
| Maximum Junction-to-Case (Drain) | $R_{thJC}$ | - | 0.28 | |

| SPECIFICATIONS ($T_J$ = 25 °C, unless otherwise noted) | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $V_{DS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 500 | - | - | V |
| $V_{DS}$ Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to 25 °C, $I_D$ = 250 µA | - | 0.52 | - | V/°C |
| Gate Threshold Voltage (N) | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 3.0 | - | 5.0 | V |
| Gate-Source Leakage | $I_{GSS}$ | $V_{GS}$ = ± 30 V | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 500 V, $V_{GS}$ = 0 V | - | - | 1 | µA |
| | | $V_{DS}$ = 400 V, $V_{GS}$ = 0 V, $T_J$ = 125 °C | - | - | 10 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 18 A | - | 0.105 | 0.130 | Ω |
| Forward Transconductance[a] | $g_{fs}$ | $V_{DS}$ = 50 V, $I_D$ = 18 A | - | 12.8 | - | S |
| **Dynamic** | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 100 V, f = 1 MHz | - | 3233 | - | pF |
| Output Capacitance | $C_{oss}$ | | - | 285 | - | |
| Reverse Transfer Capacitance | $C_{rss}$ | | - | 25 | - | |
| Effective Output Capacitance, Energy Related[a] | $C_{o(er)}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 0 V to 400 V | - | 240 | - | |
| Effective Output Capacitance, Time Related[b] | $C_{o(tr)}$ | | - | 352 | - | |
| Total Gate Charge | $Q_g$ | $V_{GS}$ = 10 V; $I_D$ = 18 A, $V_{DS}$ = 400 V | - | 83 | 125 | nC |
| Gate-Source Charge | $Q_{gs}$ | | - | 23 | - | |
| Gate-Drain Charge | $Q_{gd}$ | | - | 37 | - | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 400 V, $I_D$ = 18 A, $V_{GS}$ = 10 V, $R_g$ = 9.1 Ω | - | 33 | 66 | ns |
| Rise Time | $t_r$ | | - | 89 | 134 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 79 | 119 | |
| Fall Time | $t_f$ | | - | 68 | 102 | |
| Gate Input Resistance | $R_g$ | f = 1 MHz, open drain | - | 1.8 | - | Ω |
| **Drain-Source Body Diode Characteristics** | | | | | | |
| Continuous Source-Drain Diode Current | $I_S$ | MOSFET symbol showing the integral reverse p - n junction diode  | - | - | 36 | A |
| Pulsed Diode Forward Current | $I_{SM}$ | | - | - | 144 | |
| Diode Forward Voltage | $V_{SD}$ | $T_J$ = 25 °C, $I_S$ = 18 A, $V_{GS}$ = 0 V | - | - | 1.2 | V |
| Reverse Recovery Time | $t_{rr}$ | $T_J$ = 25 °C, $I_F$ = $I_S$ = 18 A, dI/dt = 100 A/µs, $V_R$ = 20 V | - | 490 | - | ns |
| Reverse Recovery Charge | $Q_{rr}$ | | - | 8.2 | - | µC |
| Reverse Recovery Current | $I_{RRM}$ | | - | 31 | - | A |

**Notes**

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as $C_{oss}$ while $V_{DS}$ is rising from 0 % to 80 % $V_{DSS}$.

b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 % to 80 % $V_{DSS}$.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

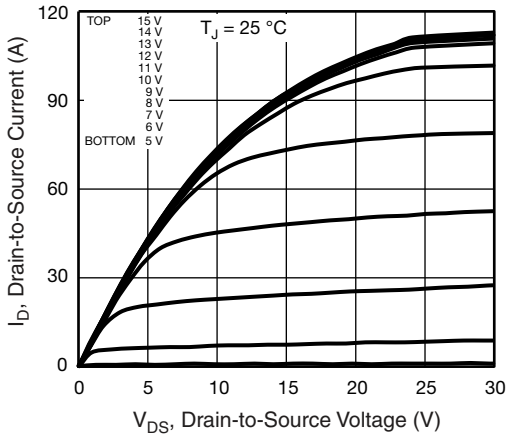



**Fig. 1 - Typical Output Characteristics**

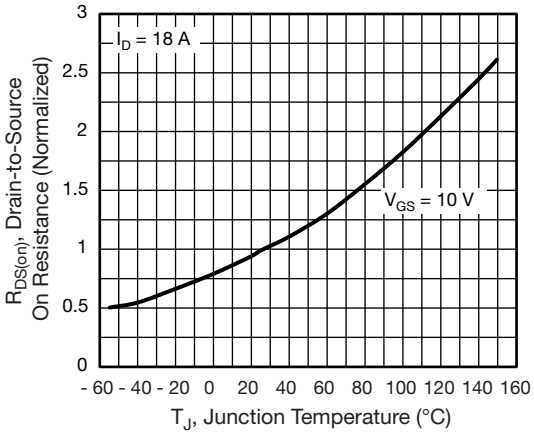



**Fig. 4 - Normalized On-Resistance vs. Temperature**

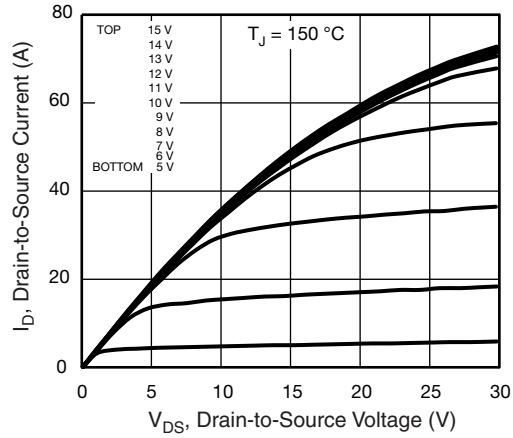



**Fig. 2 - Typical Output Characteristics**

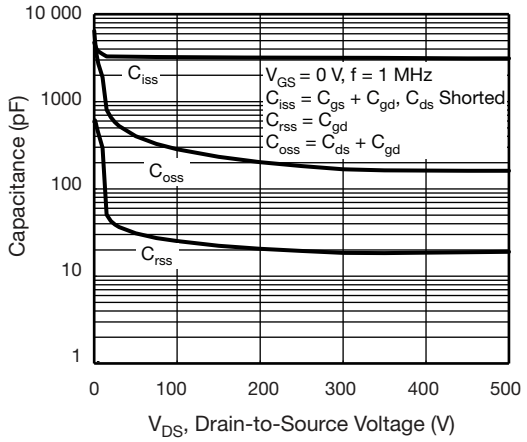



**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

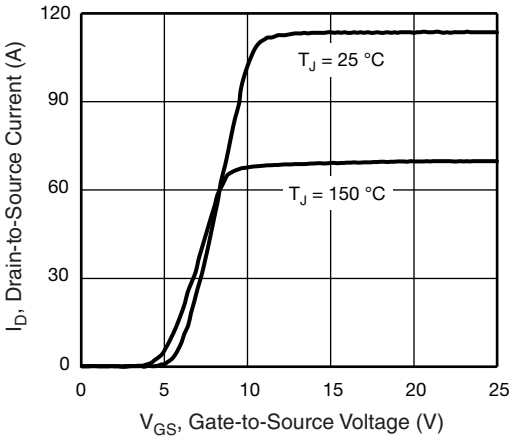



**Fig. 3 - Typical Transfer Characteristics**

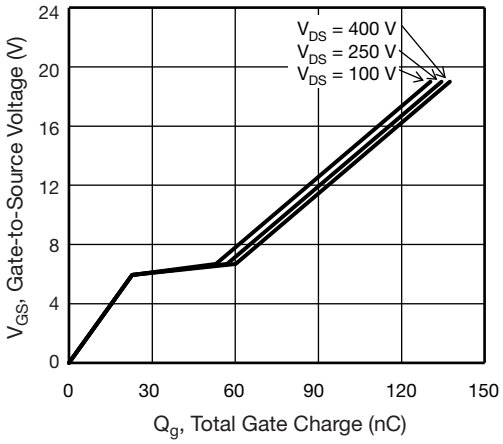



**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**

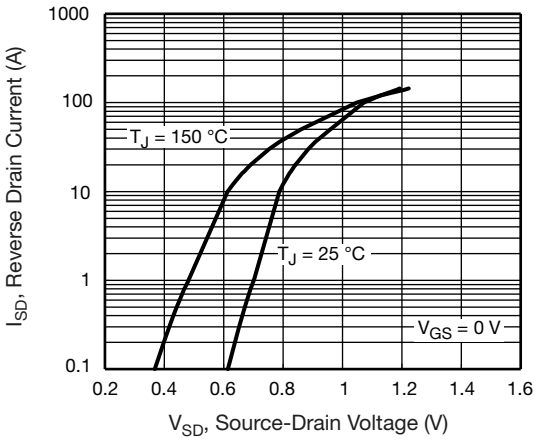



**Fig. 7 - Typical Source-Drain Diode Forward Voltage**

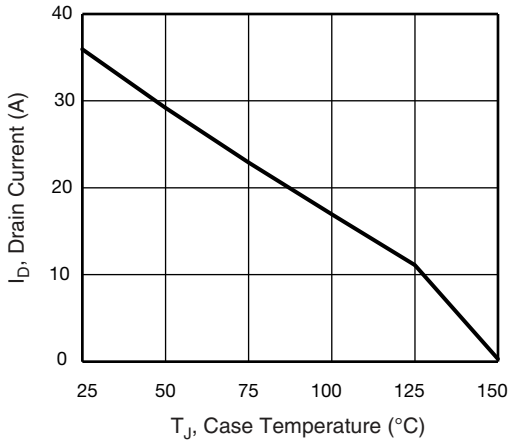



**Fig. 9 - Maximum Drain Current vs. Case Temperature**

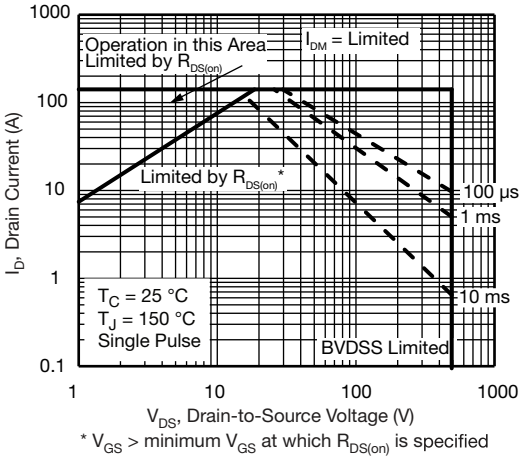



**Fig. 8 - Maximum Safe Operating Area**

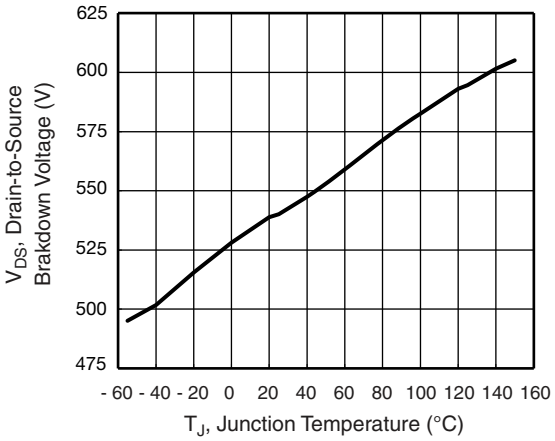



**Fig. 10 - Temperature vs. Drain-to-Source Voltage**

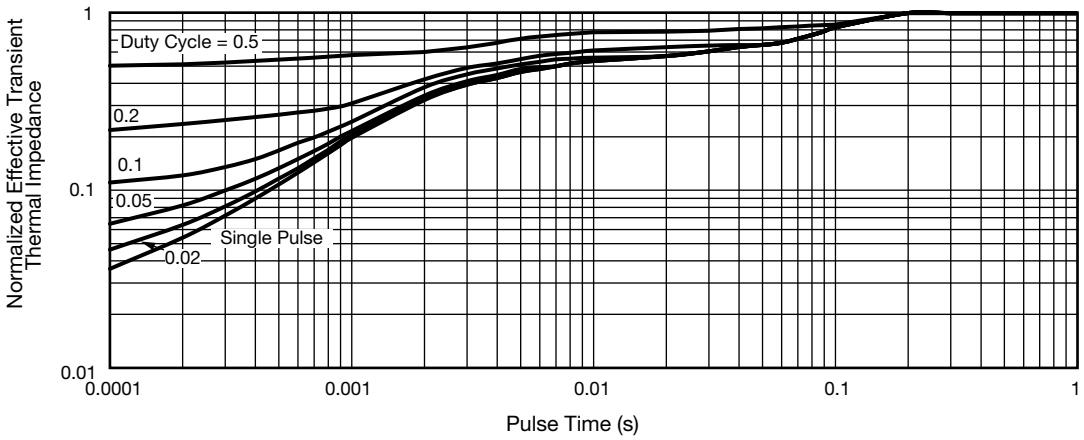



**Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case**

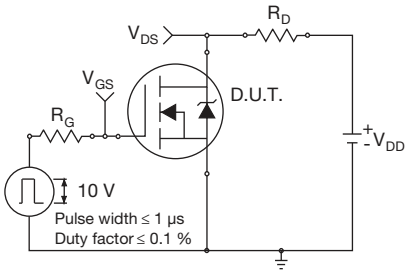



**Fig. 12 - Switching Time Test Circuit**

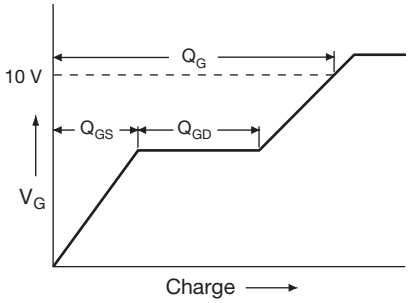



**Fig. 16 - Basic Gate Charge Waveform**

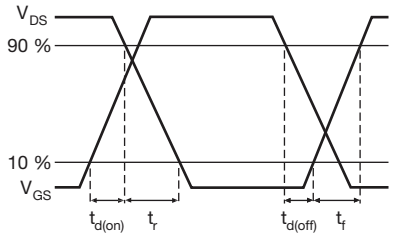



**Fig. 13 - Switching Time Waveforms**

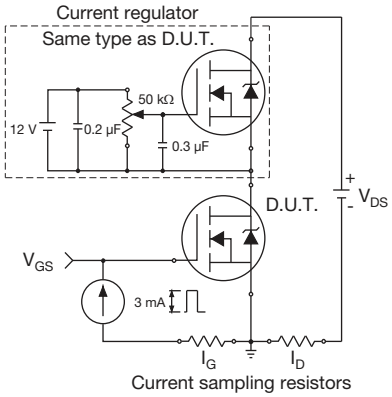



**Fig. 17 - Gate Charge Test Circuit**

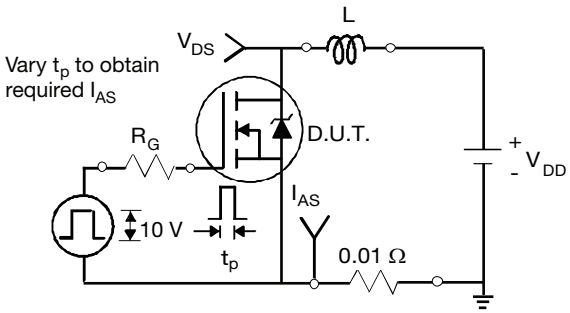



**Fig. 14 - Unclamped Inductive Test Circuit**

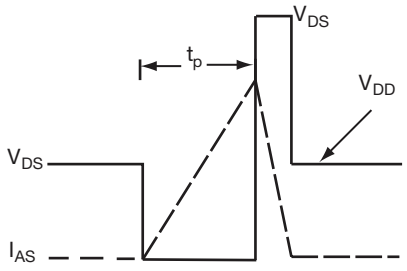
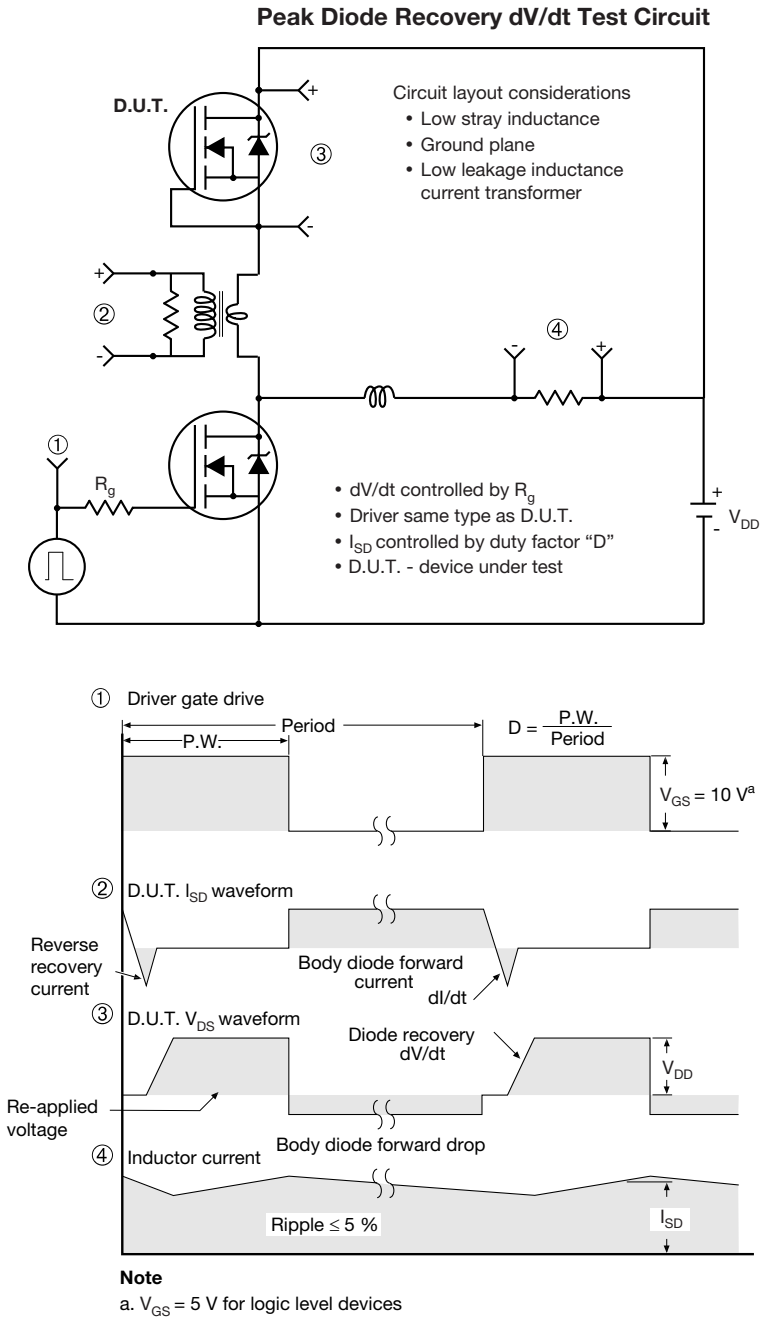



**Fig. 15 - Unclamped Inductive Waveforms**



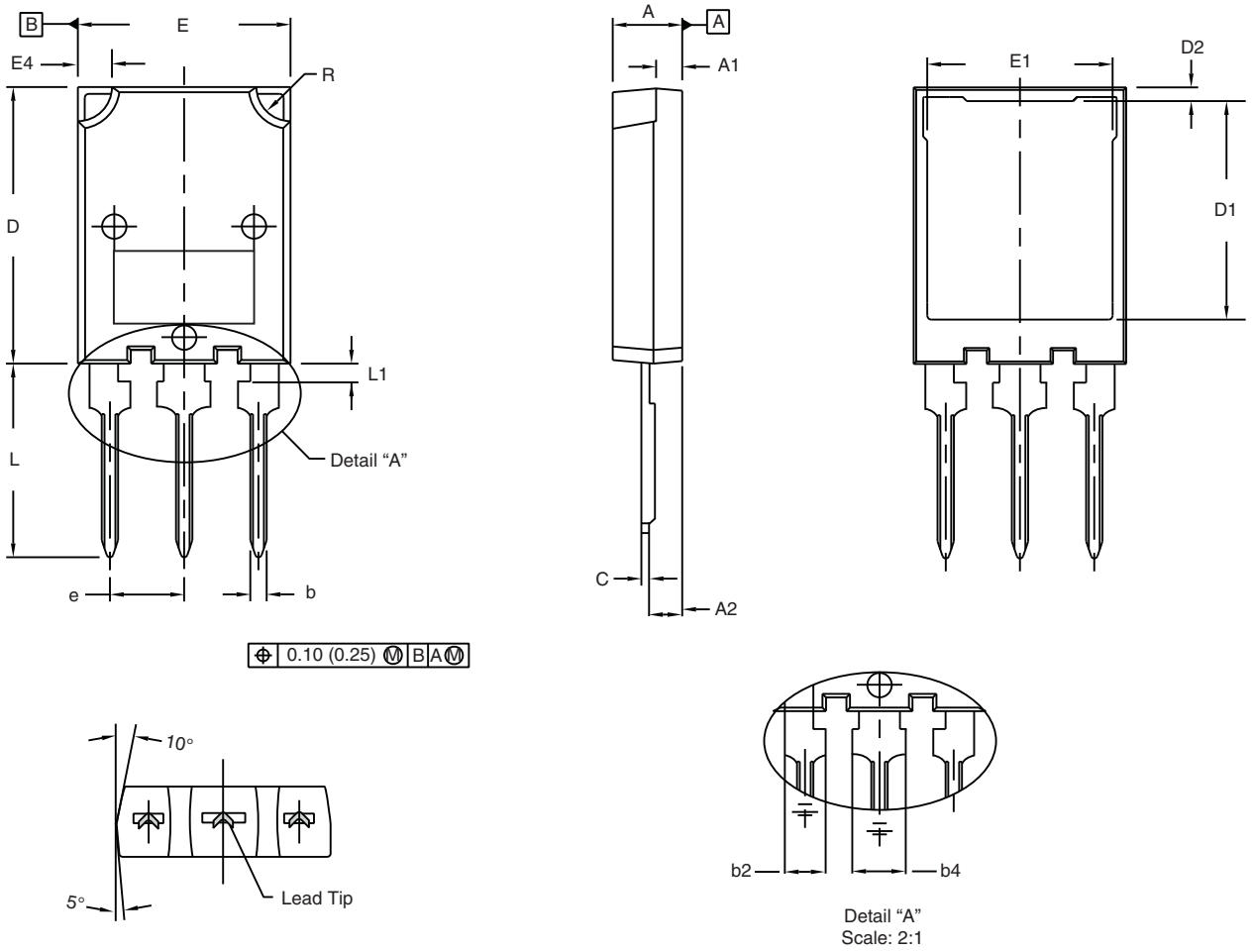

**Note**

a. $V_{GS}$ = 5 V for logic level devices

**Fig. 18 - For N-Channel**

*Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91514.*

# TO-274AA (High Voltage)




| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM. | MIN. | MAX. | MIN. | MAX. |
| A | 4.70 | 5.30 | 0.185 | 0.209 |
| A1 | 1.50 | 2.50 | 0.059 | 0.098 |
| A2 | 2.25 | 2.65 | 0.089 | 0.104 |
| b | 1.30 | 1.60 | 0.051 | 0.063 |
| b2 | 1.80 | 2.20 | 0.071 | 0.087 |
| b4 | 3.00 | 3.25 | 0.118 | 0.128 |
| c (1) | 0.38 | 0.89 | 0.015 | 0.035 |
| D | 19.80 | 20.80 | 0.780 | 0.819 |

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM. | MIN. | MAX. | MIN. | MAX. |
| D1 | 15.50 | 16.10 | 0.610 | 0.634 |
| D2 | 0.70 | 1.30 | 0.028 | 0.051 |
| E | 15.10 | 16.10 | 0.594 | 0.634 |
| E1 | 13.30 | 13.90 | 0.524 | 0.547 |
| e | 5.45 BSC | | 0.215 BSC | |
| L | 13.70 | 14.70 | 0.539 | 0.579 |
| L1 | 1.00 | 1.60 | 0.039 | 0.063 |
| R | 2.00 | 3.00 | 0.079 | 0.118 |

ECN: X17-0056-Rev. B, 27-Mar-17
DWG: 5975

**Notes**

- Dimensioning and tolerancing per ASME Y14.5M-1994
- Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outer extremes of the plastic body
- Outline conforms to JEDEC® outline to TO-274AA

(1) Dimension measured at tip of lead

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