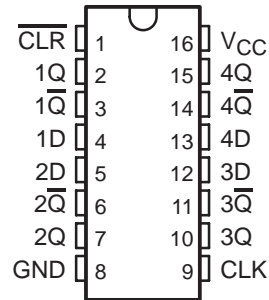


SN54LV175A, SN74LV175A QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

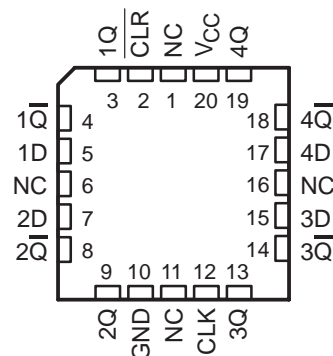
SCLS400G – APRIL 1998 – REVISED APRIL 2005

- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 7.5 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- Contain Four Flip-Flops With Double-Rail Outputs
- Applications Include:
 - Buffer/Storage Registers
 - Shift Registers
 - Pattern Generators
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

SN54LV175A . . . J OR W PACKAGE
SN74LV175A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV175A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The 'LV175A devices are quadruple D-type flip-flops designed for 2-V to 5.5-V V_{CC} operation.

These devices have a direct clear ($\overline{\text{CLR}}$) input and feature complementary outputs from each flip-flop.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SOIC – D	Tube of 40	SN74LV175AD	LV175A
		Reel of 2500	SN74LV175ADR	
	SOP – NS	Reel of 2000	SN74LV175ANSR	74LV175A
	SSOP – DB	Reel of 2000	SN74LV175ADBR	LV175A
	TSSOP – PW	Tube of 90	SN74LV175APW	LV175A
		Reel of 2000	SN74LV175APWR	
		Reel of 250	SN74LV175APWT	
TVSOP – DGV	Reel of 2000	SN74LV175ADGVR	LV175A	
-55°C to 125°C	CDIP – J	Tube of 25	SNJ54LV175AJ	SNJ54LV175AJ
	CFP – W	Tube of 150	SNJ54LV175AW	SNJ54LV175AW
	LCCC – FK	Tube of 55	SNJ54LV175AFK	SNJ54LV175AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2005, Texas Instruments Incorporated

SN54LV175A, SN74LV175A QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

SCLS400G – APRIL 1998 – REVISED APRIL 2005

description/ordering information (continued)

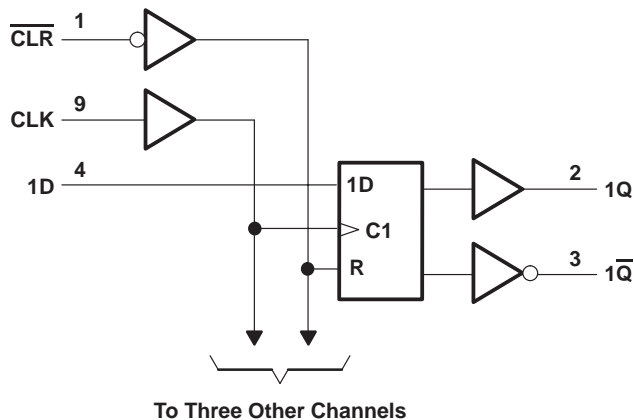
Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock (CLK) pulse.

Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of CLK. When CLK is at either the high or low level, the D input has no effect at the output.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUTS	
$\overline{\text{CLR}}$	CLK	D	Q	$\overline{\text{Q}}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q_0}$

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

SN54LV175A, SN74LV175A QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

SCLS400G – APRIL 1998 – REVISED APRIL 2005

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	73°C/W
DB package	82°C/W
DGV package	20°C/W
NS package	64°C/W
PW package	108°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 5.5 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.



SN54LV175A, SN74LV175A QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

SCLS400G – APRIL 1998 – REVISED APRIL 2005

recommended operating conditions (see Note 4)

		SN54LV175A		SN74LV175A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2	5.5	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5	1.5		V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$		
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage	$V_{CC} = 2\text{ V}$		0.5	0.5	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		$V_{CC} \times 0.3$	$V_{CC} \times 0.3$	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$		$V_{CC} \times 0.3$	$V_{CC} \times 0.3$	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		$V_{CC} \times 0.3$	$V_{CC} \times 0.3$	
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2\text{ V}$		-50	-50	μA
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		-2	-2	mA
		$V_{CC} = 3\text{ V to }3.6\text{ V}$		-6	-6	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		-12	-12	
I_{OL}	Low-level output current	$V_{CC} = 2\text{ V}$		50	50	μA
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		2	2	mA
		$V_{CC} = 3\text{ V to }3.6\text{ V}$		6	6	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		12	12	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		200	200	ns/V
		$V_{CC} = 3\text{ V to }3.6\text{ V}$		100	100	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		20	20	
T_A	Operating free-air temperature	-55	125	-40	85	$^{\circ}\text{C}$

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN54LV175A			SN74LV175A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	$I_{OH} = -50\ \mu\text{A}$	2 V to 5.5 V	$V_{CC}-0.1$			$V_{CC}-0.1$			V
	$I_{OH} = -2\ \text{mA}$	2.3 V	2			2			
	$I_{OH} = -6\ \text{mA}$	3 V	2.48			2.48			
	$I_{OH} = -12\ \text{mA}$	4.5 V	3.8			3.8			
V_{OL}	$I_{OL} = 50\ \mu\text{A}$	2 V to 5.5 V				0.1			V
	$I_{OL} = 2\ \text{mA}$	2.3 V				0.4			
	$I_{OL} = 6\ \text{mA}$	3 V				0.44			
	$I_{OL} = 12\ \text{mA}$	4.5 V				0.55			
I_I	$V_I = 5.5\text{ V or GND}$	0 to 5.5 V				± 1			μA
I_{CC}	$V_I = V_{CC}\text{ or GND, } I_O = 0$	5.5 V				20			μA
I_{off}	$V_I\text{ or }V_O = 0\text{ to }5.5\text{ V}$	0				5			μA
C_i	$V_I = V_{CC}\text{ or GND}$	3.3 V	1.4			1.4			pF

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54LV175A, SN74LV175A QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

SCLS400G – APRIL 1998 – REVISED APRIL 2005

timing requirements over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

			$T_A = 25^\circ\text{C}$		SN54LV175A		SN74LV175A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{\text{CLR}}$ low	6		6		6		ns
		CLK high or low	6.5		7		7		
t_{su}	Setup time before CLK \uparrow	Data	7		7.5		7.5		ns
		$\overline{\text{CLR}}$ inactive	7		7.5		7.5		
t_h	Hold time, data after CLK \uparrow		0.5		1		1		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

			$T_A = 25^\circ\text{C}$		SN54LV175A		SN74LV175A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{\text{CLR}}$ low	5		5		5		ns
		CLK high or low	5		5		5		
t_{su}	Setup time before CLK \uparrow	Data	5		5		5		ns
		$\overline{\text{CLR}}$ inactive	5		5		5		
t_h	Hold time, data after CLK \uparrow		1		1		1		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

			$T_A = 25^\circ\text{C}$		SN54LV175A		SN74LV175A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{\text{CLR}}$ low	5		5		5		ns
		CLK high or low	5		5		5		
t_{su}	Setup time before CLK \uparrow	Data	4		4		4		ns
		$\overline{\text{CLR}}$ inactive	5		5		5		
t_h	Hold time, data after CLK \uparrow		1		1		1		ns

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV175A		SN74LV175A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	50*	105*		45*		45	MHz	
			$C_L = 50\text{ pF}$	40	80		35		35		
t_{pd}	$\overline{\text{CLR}}$	Any	$C_L = 15\text{ pF}$	7.9*	16.6*		1*	20*	1	20	ns
	CLK	Any		9.3*	18.8*		1*	22*	1	22	
t_{pd}	$\overline{\text{CLR}}$	Any	$C_L = 50\text{ pF}$	10.4	21.6		1	25.5	1	25.5	ns
	CLK	Any		12	23.3		1	27	1	27	
$t_{sk(o)}$			$C_L = 50\text{ pF}$			2				2	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54LV175A, SN74LV175A QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

SCLS400G – APRIL 1998 – REVISED APRIL 2005

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV175A		SN74LV175A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{\max}			$C_L = 15\text{ pF}$	90*	155*		75*		75		MHz
			$C_L = 50\text{ pF}$	50	120		45		45		
t_{pd}	$\overline{\text{CLR}}$	Any	$C_L = 15\text{ pF}$		5.5*	10.1*	1*	12*	1	12	ns
	CLK	Any			6.5*	11.5*	1*	13.5*	1	13.5	
t_{pd}	$\overline{\text{CLR}}$	Any	$C_L = 50\text{ pF}$		7.4	13.6	1	15.5	1	15.5	ns
	CLK	Any			8.4	15	1	17	1	17	
$t_{sk(o)}$			$C_L = 50\text{ pF}$			1.5			1.5		ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV175A		SN74LV175A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{\max}			$C_L = 15\text{ pF}$	150*	215*		125*		125		MHz
			$C_L = 50\text{ pF}$	85	165		75		75		
t_{pd}	$\overline{\text{CLR}}$	Any	$C_L = 15\text{ pF}$		3.7*	6.4*	1*	7.5*	1	7.5	ns
	CLK	Any			4.6*	7.3*	1*	8.5*	1	8.5	
t_{pd}	$\overline{\text{CLR}}$	Any	$C_L = 50\text{ pF}$		5.3	8.4	1	9.5	1	9.5	ns
	CLK	Any			6	9.3	1	10.5	1	10.5	
$t_{sk(o)}$			$C_L = 50\text{ pF}$			1			1		ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER		SN74LV175A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.3	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.3	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage		0.99		V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

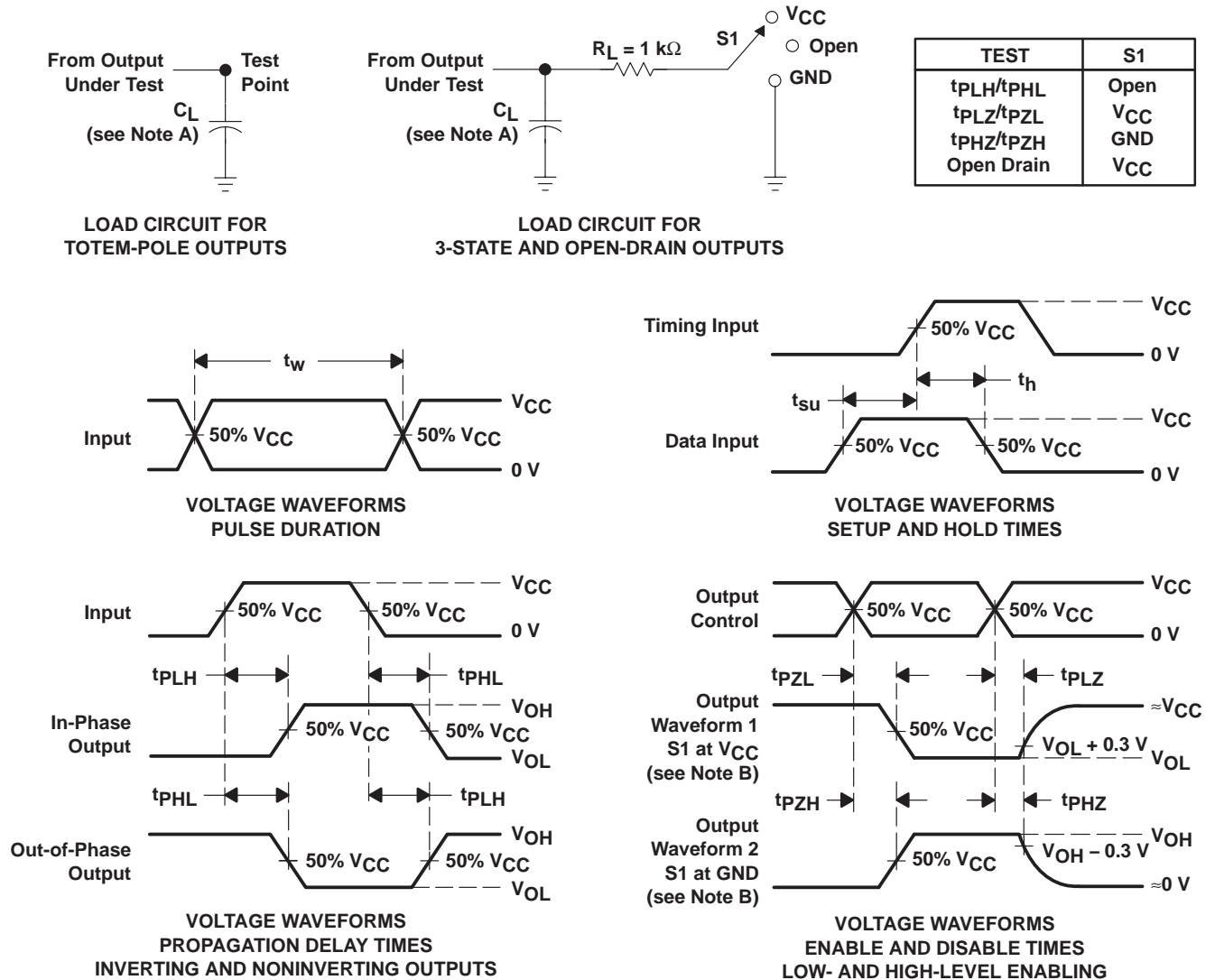
PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V	13.6	pF
			5 V	14.5	

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time, with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV175AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV175A	Samples
SN74LV175ADGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV175A	Samples
SN74LV175ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV175A	Samples
SN74LV175ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV175A	Samples
SN74LV175APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV175A	Samples
SN74LV175APWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV175A	Samples
SN74LV175APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV175A	Samples
SN74LV175APWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV175A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=100ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV175ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV175ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV175ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV175APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV175APWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV175ADGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
SN74LV175ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LV175ANSR	SO	NS	16	2000	367.0	367.0	38.0
SN74LV175APWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LV175APWT	TSSOP	PW	16	250	367.0	367.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated