

# DS8830, SN55183, SN75183 DUAL DIFFERENTIAL LINE DRIVERS

SLLS093D – OCTOBER 1972 – REVISED APRIL 1998

- Single 5-V Supply
- Differential Line Operation
- Dual Channels
- TTL Compatibility
- Short-Circuit Protection of Outputs
- Output Clamp Diodes to Terminate Line Transients
- High-Current Outputs
- Quad Inputs
- Single-Ended or Differential AND/NAND Outputs
- Designed for Use With Dual Differential Drivers SN55182 and SN75182
- Designed to Be Interchangeable With National Semiconductor DS7830 and DS8830

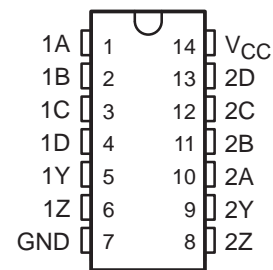
## description

The DS8830, SN55183, and SN75183 dual differential line drivers are designed to provide differential output signals with high current capability for driving balanced lines, such as twisted pair, at normal line impedances without high power dissipation. These devices can be used as TTL expander/phase splitters, because the output stages are similar to TTL totem-pole outputs.

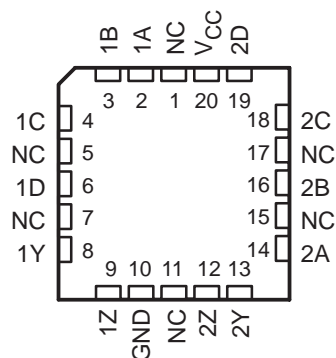
The driver is of monolithic single-chip construction, and both halves of the dual circuits use common power supply and ground terminals.

The SN55183 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The DS8830 and SN75183 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN55183 . . . J OR W PACKAGE  
SN75183 . . . D OR N PACKAGE  
DS8830 . . . N PACKAGE  
(TOP VIEW)



SN55183 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

**THE DS8830 AND SN55183 ARE  
NOT RECOMMENDED FOR NEW DESIGNS**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

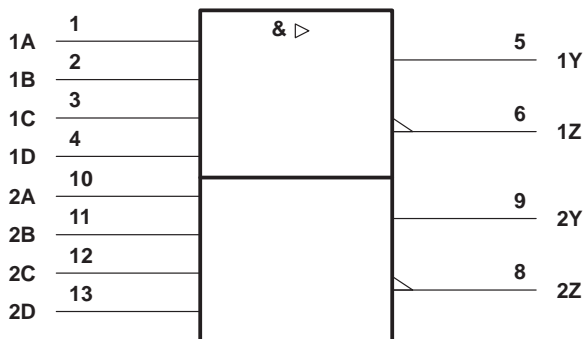
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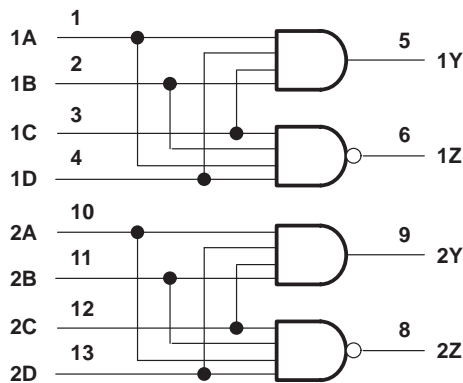
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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, N, and W packages.

## logic diagram (positive logic)



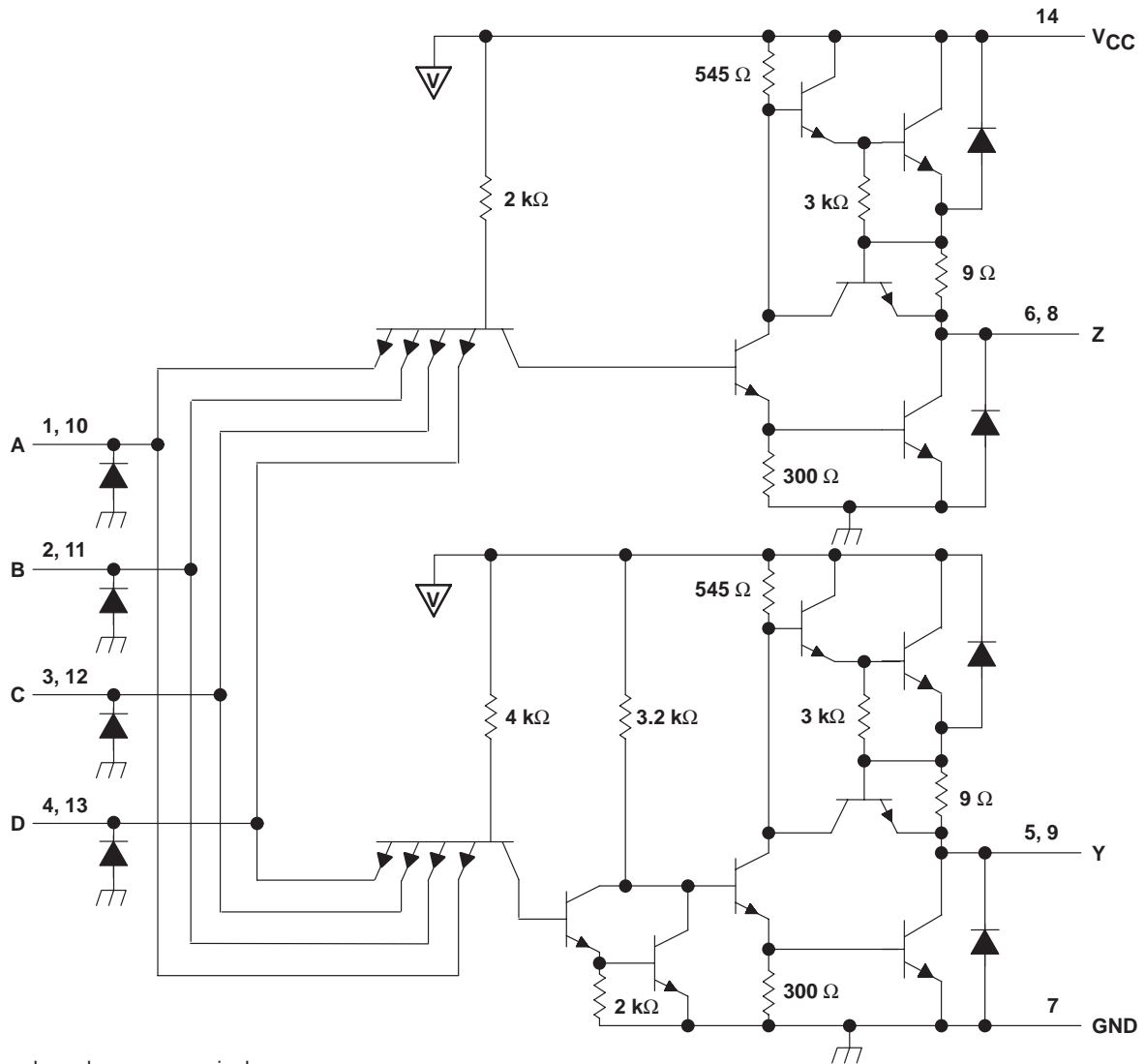
Positive logic:  $y = ABCD$ ,  $Z = \overline{ABCD}$

Pin numbers shown are for the D, J, N, and W packages.

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## schematic (each driver)



Resistor values shown are nominal.  
Pin numbers shown are for the D, J, N, and W packages.

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage, $V_I$	5.5 V
Duration of output short circuit (see Note 2)	1 s
Continuous total power dissipation	See Dissipation Rating Table
Storage temperature range, $T_{stg}$	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C
Case temperature for 60 seconds, $T_C$ : FK package	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.  
2. Not more than one output should be shorted to ground at any one time.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$	$T_A = 125^\circ\text{C}$
	POWER RATING		POWER RATING	POWER RATING
D	950 mW	7.6 mW/°C	608 mW	–
FK‡	1375 mW	11.0 mW/°C	880 mW	275 mW
J‡	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	–
W‡	1000 mW	8.0 mW/°C	640 mW	200 mW

‡ In the FK, J, and W packages, SN55183 chips are alloy mounted and SN75183 chips are glass mounted.

## recommended operating conditions

	SN55183			DS8830, SN75183			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, $V_{IH}$	2			2			V
Low-level input voltage, $V_{IL}$			0.8			0.8	V
High-level output current, $I_{OH}$			-40			-40	mA
Low-level output current, $I_{OL}$			40			40	mA
Operating free-air temperature, $T_A$	-55		125	0		70	°C



**electrical characteristics over recommended ranges of  $V_{CC}$  and operating free-air temperature (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT	
VOH	High-level output voltage	Y (AND) outputs	VIH = 2 V	IOH = -0.8 mA	2.4		V	
				IOH = -40 mA	1.8	3.3		
VOL	Low-level output voltage	Y (AND) outputs	VIL = 0.8 V	IOL = 32 mA	0.2		V	
				IOL = 40 mA	0.22	0.4		
VOH	High-level output voltage	Z (NAND) outputs	VIL = 0.8 V	IOH = -0.8 mA	2.4		V	
				IOH = -40 mA	1.8	3.3		
VOL	Low-level output voltage	Z (NAND) outputs	VIH = 2 V	IOL = 32 mA	0.2		V	
				IOL = 40 mA	0.22	0.4		
IiH	High-level input current	VIH = 2.4 V				120	μA	
Ii	Input current at maximum input voltage	VIH = 5.5 V				2	mA	
IiL	Low-level input current	VIL = 0.4 V				-4.8	mA	
Ios	Short-circuit output current‡	VCC = 5 V, TA = 125°C§		-40	-100	-120	mA	
Icc	Supply current (average per driver)	VCC = 5 V, All inputs at 5 V, No load				10	18	mA

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Not more than one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.

§  $T_A = 125^\circ\text{C}$  is applicable to SN55183 only.

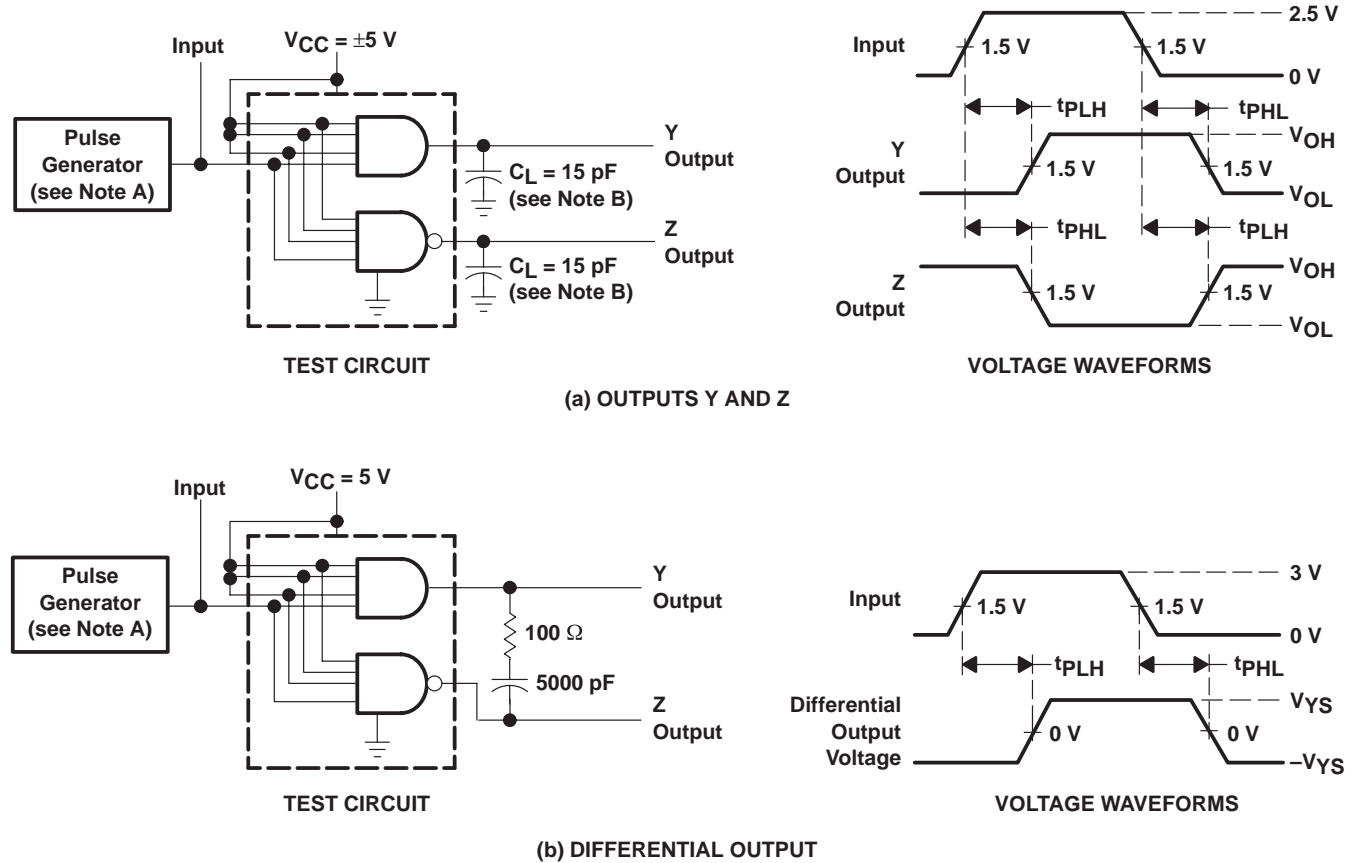
**switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$**

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
tPLH	Propagation delay time, low- to high-level Y output	AND gates	CL = 15 pF, See Figure 1(a)		8	12	ns
tPHL	Propagation delay time, high- to low-level Y output	AND gates	CL = 15 pF, See Figure 1(a)		12	18	ns
tPLH	Propagation delay time, low- to high-level Z output	NAND gates	CL = 15 pF, See Figure 1(a)		6	12	ns
tPHL	Propagation delay time, high- to low-level Z output	NAND gates	CL = 15 pF, See Figure 1(a)		6	8	ns
tPLH	Propagation delay time, low- to high-level differential output	Y output with respect to Z output, RL = 100 Ω in series with 5000 pF, See Figure 1(b)			9	16	ns
tPHL	Propagation delay time, high- to low-level differential output	Y output with respect to Z output, RL = 100 Ω in series with 5000 pF, See Figure 1(b)			8	16	ns

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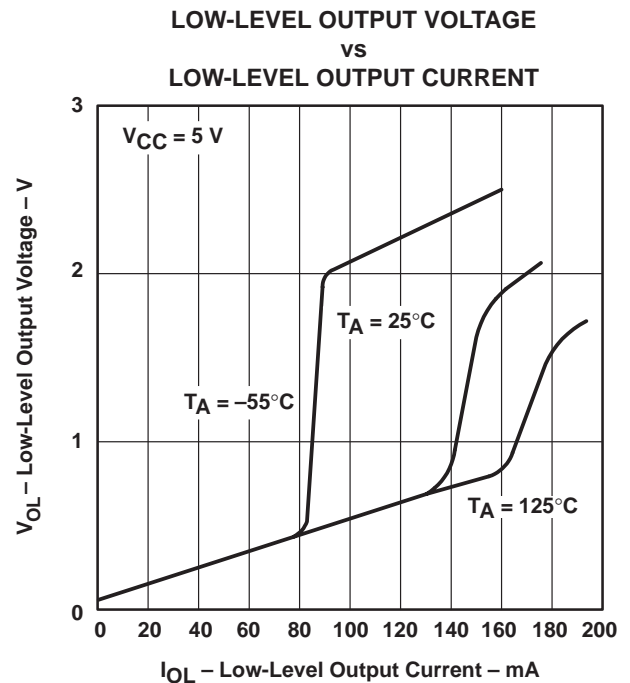
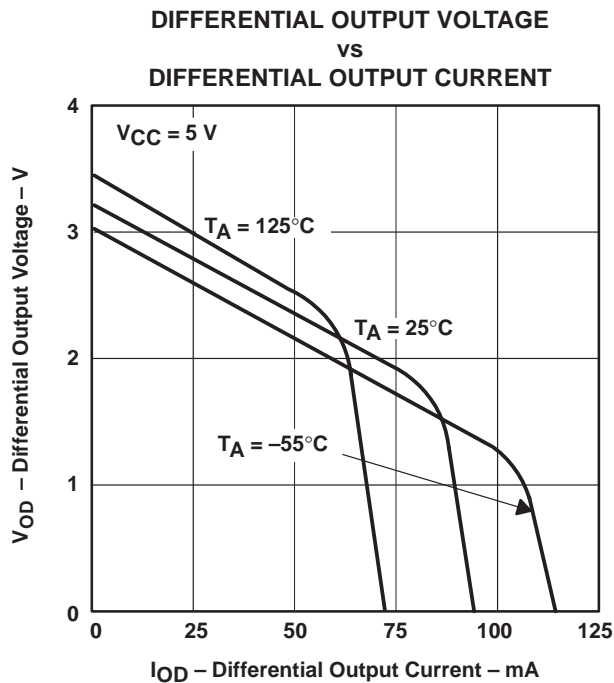
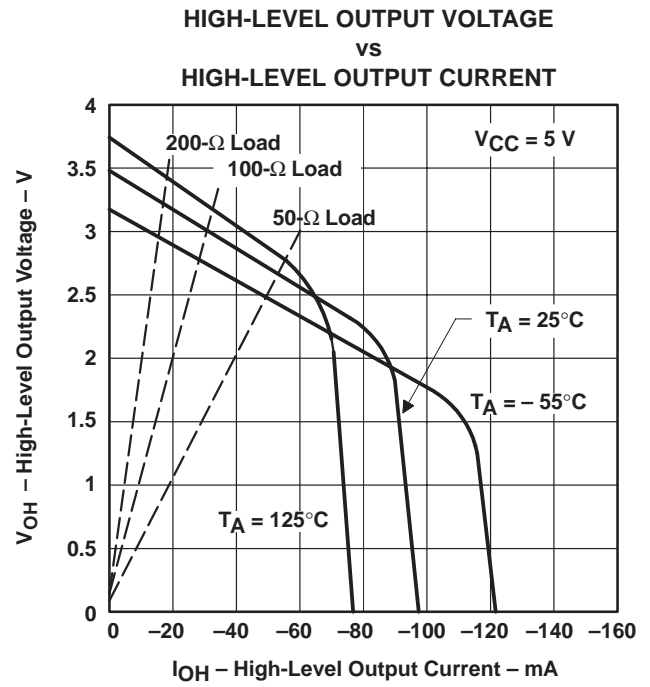
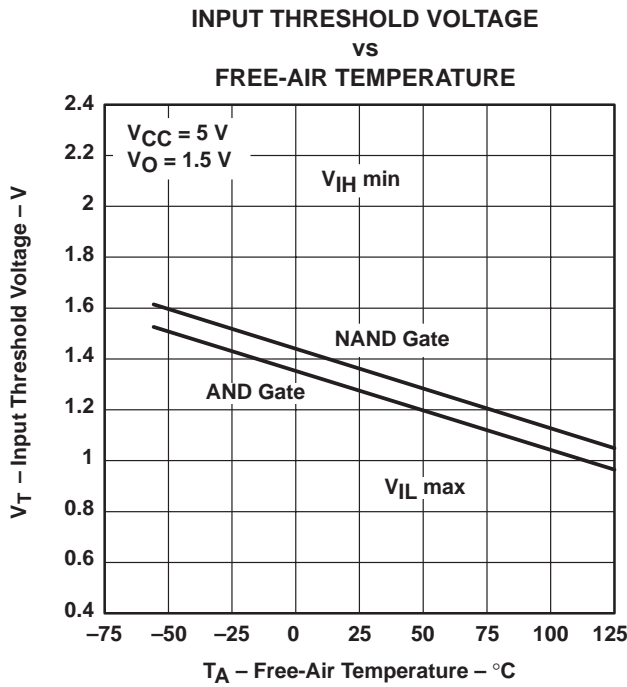
## PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The pulse generators have the following characteristics:  $Z_O = 50\ \Omega$ ,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$ ,  $t_w = 0.5\ \mu\text{s}$ ,  $\text{PRR} \leq 1\text{ MHz}$ .  
 B.  $C_L$  includes probe and jig capacitance.  
 C. Waveforms are monitored on an oscilloscope with  $r_i \geq 1\text{ M}\Omega$ .

Figure 1. Test Circuits and Voltage Waveforms

TYPICAL CHARACTERISTICS†

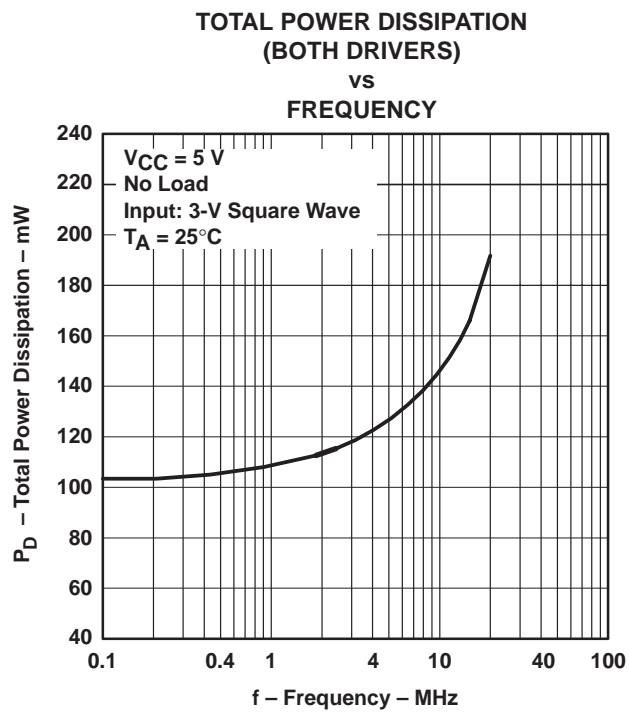
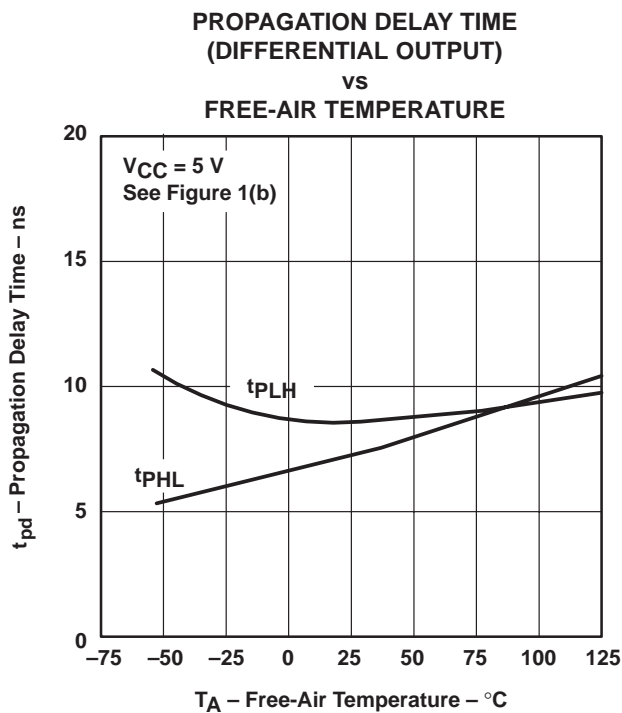


† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

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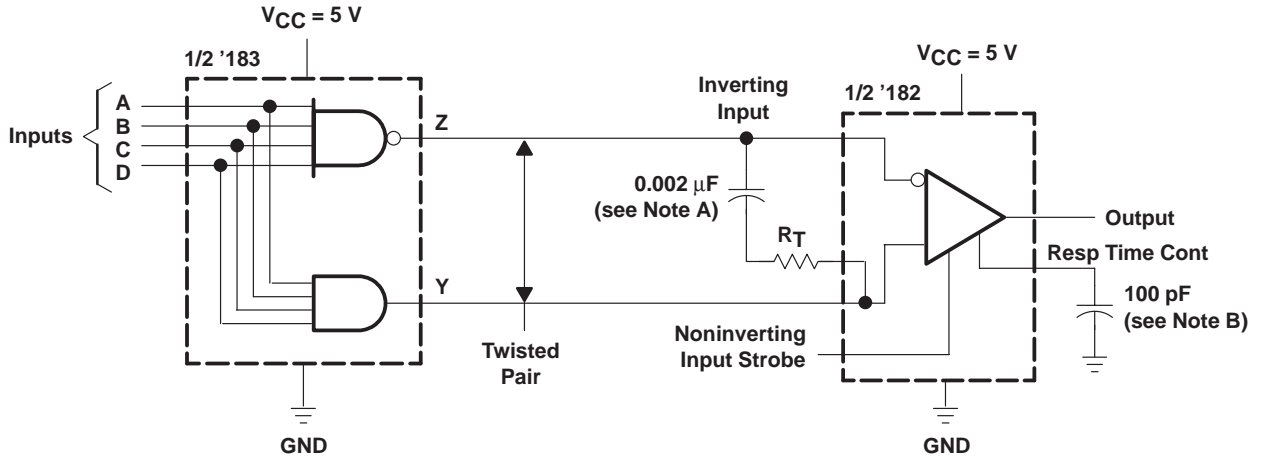
## TYPICAL CHARACTERISTICS†



† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.



APPLICATION INFORMATION



NOTES: A. When the inputs are open circuited, the output is high. A capacitor may be used for dc isolation of the line-terminating resistor. At the frequency of operation, the impedance of the capacitor should be relatively small.

Example: let  $f = 5 \text{ MHz}$   
 $C = 0.002 \mu\text{F}$

$$Z_{(\text{circuit})} = \frac{1}{2\pi f C} = \frac{1}{2\pi(5 \times 10^6)(0.002 \times 10^{-6})}$$

$$Z_{(\text{circuit})} \approx 16\Omega$$

B. Use of a capacitor to control response time is optional.

Figure 8. Transmission of Digital Data Over Twisted-Pair Line

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-7900901VCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-7900901VC A SNV55183J	<a href="#">Samples</a>
7900901CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	7900901CA SNJ55183J	<a href="#">Samples</a>
SN55183J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN55183J	<a href="#">Samples</a>
SN75183D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75183	<a href="#">Samples</a>
SN75183DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75183	<a href="#">Samples</a>
SN75183N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75183N	<a href="#">Samples</a>
SN75183NE4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75183N	<a href="#">Samples</a>
SN75183NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75183	<a href="#">Samples</a>
SNJ55183J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	7900901CA SNJ55183J	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN55183, SN55183-SP, SN75183 :**

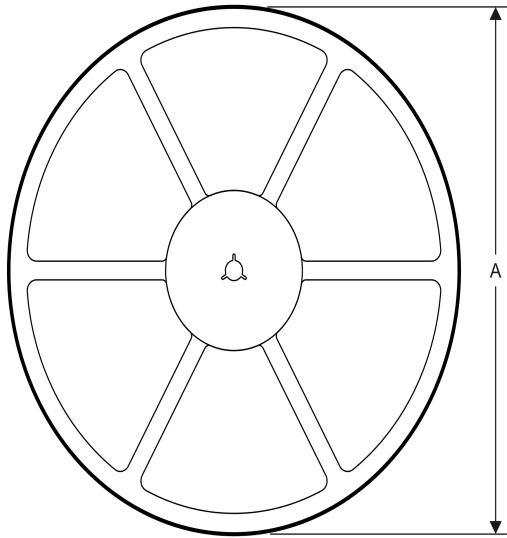
- Catalog: [SN75183](#), [SN55183](#)
- Military: [SN55183](#)
- Space: [SN55183-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75183NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75183NSR	SO	NS	14	2000	367.0	367.0	38.0

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J 14

**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

# J0014A



## PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

### NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



# EXAMPLE BOARD LAYOUT

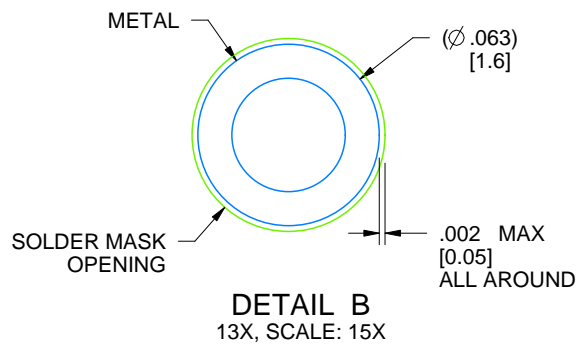
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



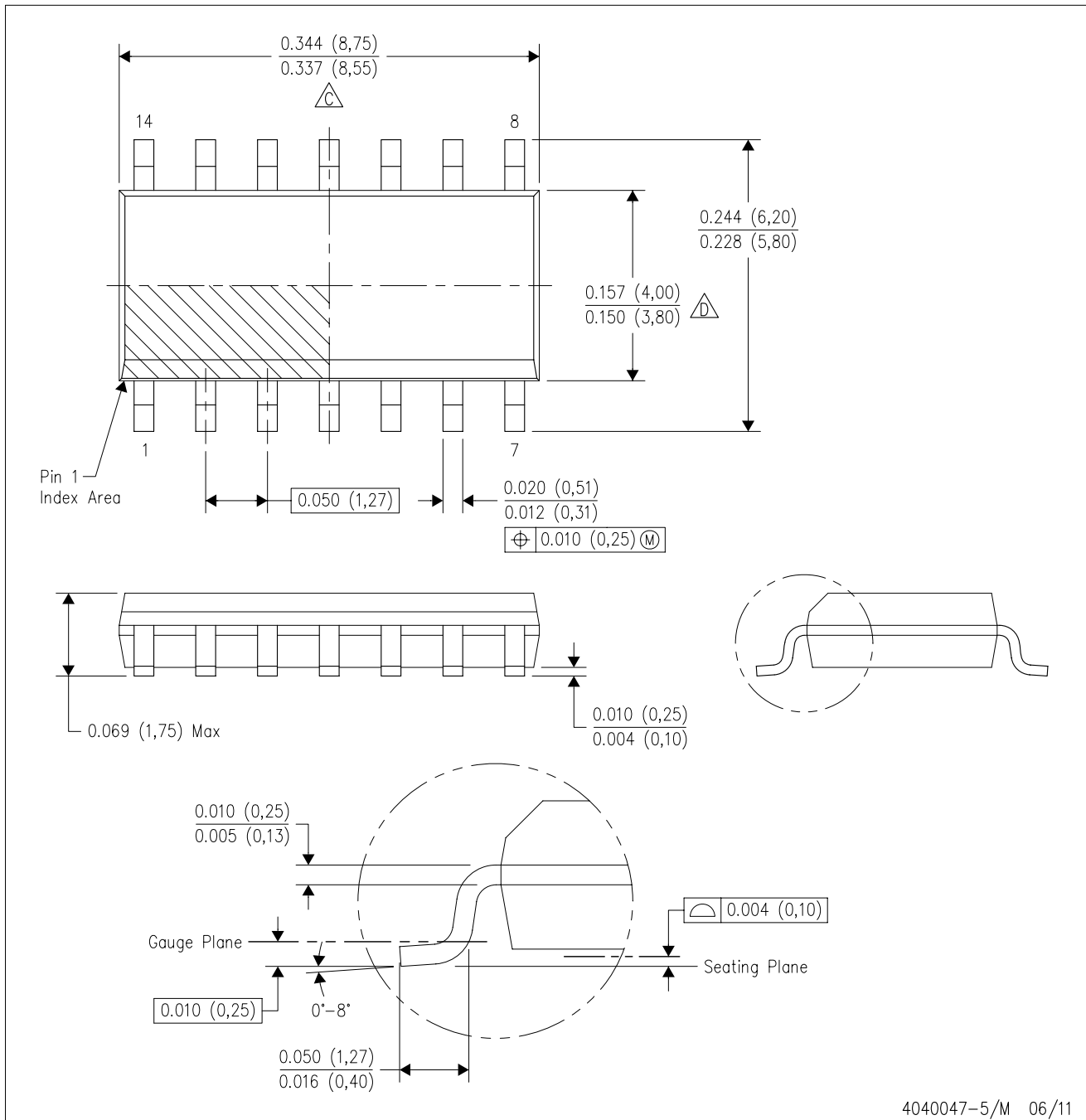
LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X





4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

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