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FAIRCHILD SEMICONDUCTOR®

November 2012

FSA3200 —Two-Port, High-Speed USB2.0 Switch with Mobile High-Definition Link (MHL™)

Features

- Low On Capacitance: 2.7 pF / 3.1 pF MHL / USB (Typical)
- Low Power Consumption: 30μA Maximum
- Supports MHL Rev. 2.0
- MHL Data Rate: 4.68 Gbps
- V_{BUS} Powers Device with No V_{CC}
- Packaged in 16-Lead UMLP (1.8 x 2.6 mm)
- Over-Voltage Tolerance (OVT) on all USB Ports Up to 5.25 V without External Components

Applications

- Cell Phones and Digital Cameras

Description

The FSA3200 is a bi-directional, low-power, two-port, high-speed, USB2.0 and video data switch. Configured as a double-pole, double-throw (DPDT) switch for data and a single-pole, double-throw (SPDT) switch for ID; it is optimized for switching between high- or full-speed USB and Mobile Digital Video sources (MDV), including supporting the MHL™ Rev. 2.0 specification.

The FSA3200 contains special circuitry on the switch I/O pins, for applications where the V_{CC} supply is powered off (V_{CC}=0), that allows the device to withstand an over-voltage condition. This switch is designed to minimize current consumption even when the control voltage applied to the control pins is lower than the supply voltage (V_{CC}). This feature is especially valuable to mobile applications, such as cell phones, allowing direct interface with the general-purpose I/Os of the baseband processor. Other applications include switching and connector sharing in portable cell phones, digital cameras, and notebook computers.

Ordering Information

Part Number	Top Mark	Operating Temperature Range	Package
FSA3200UMX	GB	-40 to +85°C	16-Lead, Ultrathin Molded Leadless Package (UMLP), 1.8 x 2.6 mm

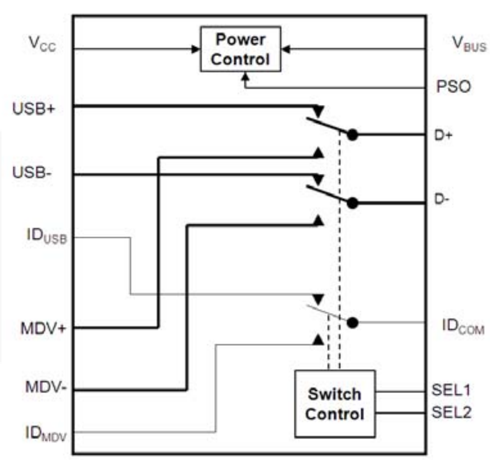

Figure 1. Analog Symbol

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Switch Power Operation

In normal operation, the FSA3200 is powered from the V_{CC} pin, which typically is derived from a regulated power management device. In special circumstances, such as production test or system firmware upgrade, the device can be powered from the V_{BUS} pin. In this mode of operation, a valid V_{BUS} voltage is present (per USB2.0 specification) and V_{CC}=0 V, typically due to a no-battery condition. With the SELn pins strapped LOW (via external resistor), the FSA3200 closes the USB path, enabling the initial programming of the system directly from the USB connector. Once the system has normal operating supply power with V_{CC} present, the V_{BUS} supply is not utilized and normal switch operation commences. Optionally, the Power Select Override (PSO) pin can be set HIGH to force the device to be powered from V_{BUS}.

The V_{BUS} / V_{CC} detection capability is not intended to be an accurate determination of the voltages present, rather a state condition detection to determine which supply should be used. These state determinations rely on the voltage conditions as described in the Electrical Characterization tables below.

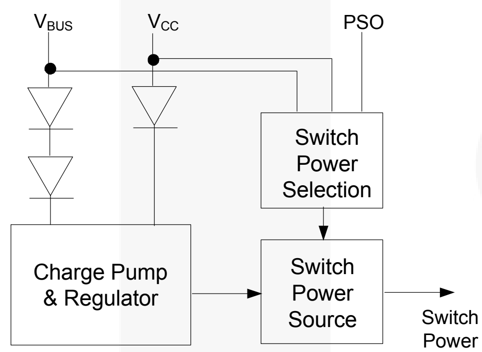


Figure 2. Simplified Logic of Switch Power Selection Circuit

Table 1. Switch Power Selection Truth Table

V_{CC}	V_{BUS}	PSO[1]	Switch Power Source
0	0	0	No switch power, switch paths high-Z
0	1	0	V_{BUS}
1	0	0	V_{CC}
1	1	0	V_{CC}
0	0	1	No switch power, switch paths high-Z
0	1	1	V_{BUS}
1	0	1	V_{CC}[2]
1	1	1	V_{BUS}

Notes:
1. Control inputs should never be left floating or unconnected. If the PSO function is used, a weak pull-up resistor (3 MΩ) should be used to minimize static current draw. If the PSO function is not used, tie directly to GND.
2. PSO control is overridden with no V_{BUS} and the power selection is switched to V_{CC}.

Table 2. Data Switch Select Truth Table

SEL1[3]	SEL2[3]	Function
0	0	D+/D- connected to USB+/USB-, ID_{CO} connected to ID_{USB}
0	1	D+/D- connected to USB+/USB-, ID_{COM} connected to ID_{MDV}
1	0	D+/D- connected to MDV+/MDV-, ID_{COM} connected to ID_{USB}
1	1	D+/D- connected to MDV+/MDV-, ID_{COM} connected to ID_{MDV}

Note:
3. Control inputs should never be left floating or unconnected. To guarantee default switch closure to the USB position, the SEL pins should be tied to GND with a weak pull- down resistor (3 MΩ) to minimize static current draw.

Pin Configuration

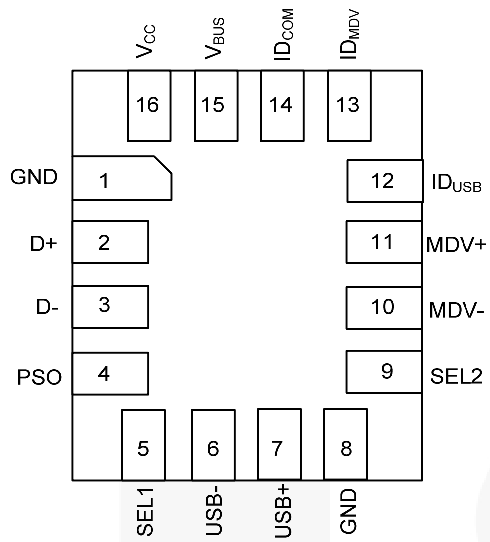


Figure 3. Pin Assignments (Top-Through View)

Pin Definitions

Pin#	Name	Description
1	GND	Ground
2	D+	Data Switch Output (Positive)
3	D-	Data Switch Output (Negative)
4	PSO	Power Select Override
5	SEL1	Data Switch Select
6	USB-	USB Differential Data (Negative)
7	USB+	USB Differential Data (Positive)
8	GND	Ground
9	SEL2	ID Switch Select
10	MDV-	MDV Differential Data (Negative)
11	MDV+	MDV Differential Data (Positive)
12	ID_{USB}	ID Switch MUX Output for USB
13	ID_{MDV}	ID Switch MUX Output for MDV
14	ID_{COM}	ID Switch Common
15	V_{BUS}	Device Power when V_{CC} Not Available
16	V_{CC}	Device Power from System[4]

Note:

4. Device automatically switches from V_{BUS} when valid V_{CC} minimum voltage is present.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}, V_{BUS}	Supply Voltage		-0.5	5.5	V
V_{CNTRL}	DC Input Voltage (SELn, PSO)[5]		-0.5	V_{CC}	V
V_{SW}[6]	DC Switch I/O Voltage[5]		-0.50	5.25	V
I_{IK}	DC Input Diode Current		-50		mA
I_{OUT}	DC Output Current			100	mA
T_{STG}	Storage Temperature		-65	+150	°C
MSL	Moisture Sensitivity Level (JEDEC J-STD-020A)			1	
ESD	Human Body Model, JEDEC: JESD22-A114	All Pins		3.5	kV
	IEC 61000-4-2, Level 4, for D+/D- and V_{CC} Pins[7]	Contact		8.0	
	IEC 61000-4-2, Level 4, for D+/D- and V_{CC} Pins[7]	Air		15.0	
	Charged Device Model, JESD22-C101			2.0	

Notes:

5. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.
6. V_{SW} refers to analog data switch paths (USB, MDV, and ID).
7. Testing performed in a system environment using TVS diodes.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{BUS}	Supply Voltage Running from V_{BUS} Voltage	4.20	5.25	V
V_{CC}	Supply Voltage Running from V_{CC}	2.7	4.5	V
$t_{RAMP(VBUS)}$	Power Supply Slew Rate from V_{BUS}	100	1000	µs/V
$t_{RAMP(VCC)}$	Power Supply Slew Rate from V_{CC}	100	1000	µs/V
Θ_{JA}	Thermal Resistance		336	C°/W
V_{CNTRL}	Control Input Voltage (SELn, PSO)[8]	0	4.5	V
$V_{SW(USB)}$	Switch I/O Voltage (USB and ID Switch Paths)	-0.5	3.6	V
$V_{SW(MDV)}$	Switch I/O Voltage (MDV Switch Path)	1.65	3.45	V
T_A	Operating Temperature	-40	+85	°C

Note:

8. The control inputs must be held HIGH or LOW; they must not float.

DC Electrical Characteristics

All typical value are at T_A=25°C unless otherwise specified.

Symbol	Parameter	Condition	V_{CC} (V)	T_A=- 40ºC to +85ºC			Unit
				Min.	Typ.	Max.	
V_{IK}	Clamp Diode Voltage	I_{IN}=-18 mA	2.7			-1.2	V
V_{IH}	Control Input Voltage High	SELn, PSO	2.7 to 4.3	1.25			V
V_{IL}	Control Input Voltage Low	SELn, PSO	2.7 to 4.3			0.6	V
I_{IN}	Control Input Leakage	V_{SW}=0 V to 3.6 V, V_{CNTRL}=0 V to 1.98 V	4.3	-1		1	µA
$I_{OZ(MDV)}$	Off-State Leakage for Open MDV Data Paths	V_{SW}=1.65 V ≤ MDV ≤ 3.45 V	4.3	-1		1	µA
$I_{OZ(USB)}$	Off-State Leakage for Open USB Data Paths	V_{SW}=0 V ≤ USB ≤ 3.6 V	4.3	-1		1	µA
$I_{OZ(ID)}$	Off-State Leakage for Open ID Data Path	V_{SW}=0 V ≤ ID ≤ 3.6 V	4.3	-0.5		0.5	µA
$I_{CL(MDV)}$	On-State Leakage for Closed MDV Data Paths(9)	V_{SW}=1.65 V ≤ MDV ≤ 3.45 V	4.3	-1		1	µA
$I_{CL(USB)}$	On-State Leakage for Closed USB Data Paths(9)	V_{SW}=0 V ≤ USB ≤ 3.6 V	4.3	-1		1	µA
$I_{CL(ID)}$	On-State Leakage for Closed(9) ID Data Path	V_{SW}=0 V ≤ ID ≤ 3.6 V	4.3	-0.5		0.5	µA
I_{OFF}	Power-Off Leakage Current (All I/O Ports)	V_{SW}=0 V or 3.6 V, Figure 5	0	-1		1	µA
$R_{ON(USB)}$	HS Switch On Resistance (USB to D Path)	V_{SW}=0.4 V, I_{ON}=-8 mA Figure 4	2.7		3.9	6.5	Ω
$R_{ON(MDV)}$	HS Switch On Resistance (MDV to D Path)	V_{SW}=V_{CC}-1050mV, I_{ON}=-8mA, Figure 4	2.7		5		Ω
$R_{ON(ID)}$	LS Switch On Resistance (ID Path)	V_{SW}=3V, I_{ON}=-8mA Figure 4	2.7		12		Ω
$\Delta R_{ON(MDV)}$	Difference in R_{ON} Between MDV Positive-Negative	V_{SW}=V_{CC}-1050 mV, I_{ON}=-8 mA, Figure 4,	2.7		0.03		Ω
$\Delta R_{ON(USB)}$	Difference in R_{ON} Between USB Positive-Negative	V_{SW}=0.4 V, I_{ON}=-8 mA Figure 4	2.7		0.18		Ω
$\Delta R_{ON(ID)}$	Difference in R_{ON} Between ID Switch Paths	V_{SW}=3 V, I_{ON}=-8 mA Figure 4	2.7		0.4		Ω
$R_{ONF(MDV)}$	Flatness for R_{ON} MDV Path	V_{SW}=1.65 V to 3.45 V, I_{ON}=-8 mA, Figure 4	2.7		1		Ω
I_{VBUS}	V_{BUS} Quiescent Current	V_{BUS}=5.25 V, V_{CNTRL}=0 V or 1.98 V, I_{OUT}=0	4.3			100	µA
I_{CC}	V_{CC} Quiescent Current	V_{BUS}=0 V, V_{CNTRL}=0 V or 1.98 V, I_{OUT}=0	4.3			30	µA

Note:

9. For this test, the data switch is closed with the respective switch pin floating.

AC Electrical Characteristics

All typical value are for V_{CC}=3.3 V and T_A=25°C unless otherwise specified.

Symbol	Parameter	Condition	V_{CC} (V)	T_A=- 40ºC to +85ºC			Unit
				Min.	Typ.	Max.	
t_{ON}	Turn-On Time, SELn to Output	R_L=50 Ω, C_L=5 pF, $V_{SW(USB)}$=0.8 V, $V_{SW(MDV)}$=3.3 V, Figure 6, Figure 7	2.7 to 3.6		445	600	ns
t_{OFF}	Turn-Off Time, SELn to Output	R_L=50 Ω, C_L=5 pF, $V_{SW(USB)}$=0.8 V, $V_{SW(MDV)}$=3.3V, Figure 6, Figure 7	2.7 to 3.6		125	300	ns
t_{PD}	Propagation Delay(10)	C_L=5 pF, R_L=50 Ω, Figure 6, Figure 8	2.7 to 3.6		0.25		ns
t_{BBM}	Break-Before-Make(10)	R_L=50 Ω, C_L=5 pF, V_{ID}=V_{MDV}=3.3 V, V_{USB}=0.8 V, Figure 10	2.7 to 3.6	2.0		13	ns
$O_{IRR(MDV)}$	Off Isolation(10)	V_S=1 V_{pk-pk}, R_L=50 Ω, f=240 MHz, Figure 12	2.7 to 3.6		-45		dB
$O_{IRR(USB)}$		V_S=400m V_{pk-pk}, R_L=50Ω, f=240MHz, Figure 12	2.7 to 3.6		-38		dB
$Xtalk_{MDV}$	Non-Adjacent Channel(10) Crosstalk	V_S=1 V_{pk-pk}, R_L=50 Ω, f=240 MHz, Figure 13	2.7 to 3.6		-44		dB
$Xtalk_{USB}$		V_S=400 mV_{pk-pk}, R_L=50 Ω, f=240 MHz, Figure 13	2.7 to 3.6		-39		dB
BW	Differential -3 db Bandwidth(10)	V_{IN}=1 V_{pk-pk}, MDV Path, R_L=50 Ω, C_L=0 pF, Figure 11, Figure 16	2.7 to 3.6		2.34		GHz
		V_{IN}=400 mV_{pk-pk}, USB Path, R_L=50 Ω, C_L=0 pF, Figure 11, Figure 17			1.59		
		ID Path, R_L=50 Ω, C_L=0 pF, Figure 11			100		MHz

Note:

10. Guaranteed by characterization.

USB High-Speed AC Electrical Characteristics

Typical values are at T_A= -40ºC to +85ºC.

Symbol	Parameter	Condition	V_{CC} (V)	Typ.	Unit
$t_{SK(P)}$	Skew of Opposite Transitions of the Same Output(11)	C_L=5 pF, R_L=50 Ω, Figure 9	3.0 to 3.6	3	ps
t_J	Total Jitter(11)	R_L=50 Ω, C_L=5 pf, t_R=t_F=500 ps (10-90%) at 480 Mbps, PN7	3.0 to 3.6	15	ps

Note:
11. Guaranteed by characterization.

MDV AC Electrical Characteristics

Typical values are at T_A= -40ºC to +85ºC.

Symbol	Parameter	Condition	V_{CC} (V)	Typ.	Unit
$t_{SK(P)}$	Skew of Opposite Transitions of the Same Output(12)	R_{PU}=50 Ω to V_{CC}, C_L=0 pF	3.0 to 3.6	3	ps
t_J	Total Jitter(12)	f=2.25 Gbps, PN7, R_{PU}=50 Ω to V_{CC}, C_L=0 pF	3.0 to 3.6	15	ps

Note:
12. Guaranteed by characterization.

Capacitance

Typical values are at T_A= -40ºC to +85ºC.

Symbol	Parameter	Condition	Typ.	Unit
C_{IN}	Control Pin Input Capacitance(13)	V_{CC}=0 V, f= 1 MHz	1.5	pF
$C_{ON(USB)}$	USB Path On Capacitance(13)	V_{CC}=3.3 V, f=240 MHz, Figure 15	3.1	
$C_{OFF(USB)}$	USB Path Off Capacitance(13)	V_{CC}=3.3 V, f=240 MHz, Figure 14	1.6	
$C_{ON(MDV)}$	MDV Path On Capacitance(13)	V_{CC}=3.3 V, f=240 MHz, Figure 15	2.7	
$C_{OFF(MDV)}$	MDV Path Off Capacitance(13)	V_{CC}=3.3 V, f=240 MHz, Figure 14	1.1	

Note:
13. Guaranteed by characterization.

Test Diagrams

Note:

14. HSD refers to the high-speed data USB or MDV paths.

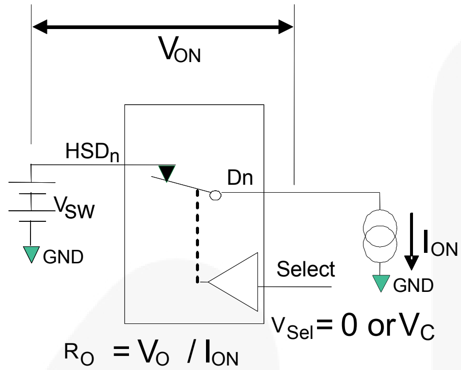


Figure 4. On Resistance

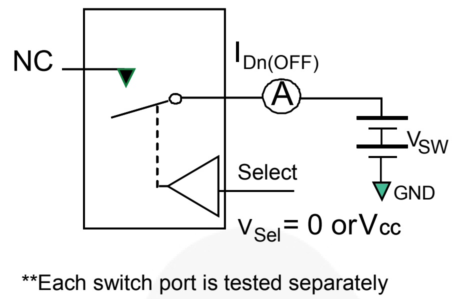


Figure 5. Off Leakage

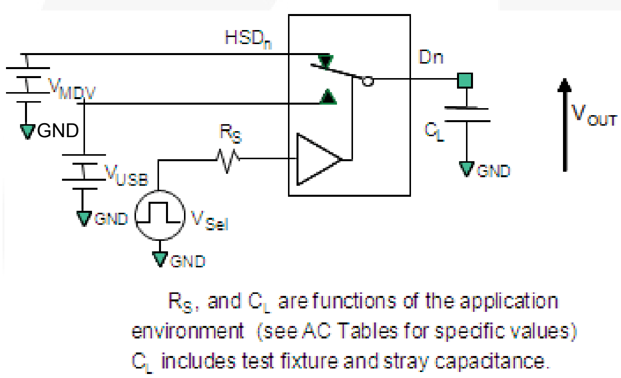


Figure 6. AC Test Circuit Load

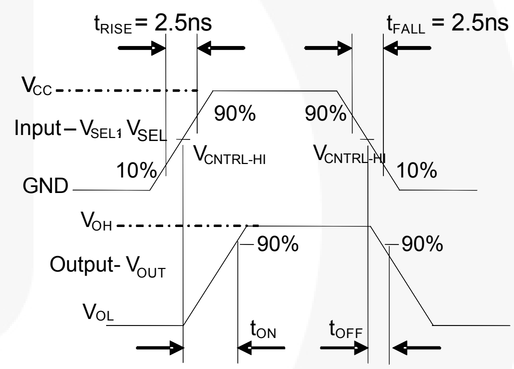


Figure 7. Turn-On / Turn-Off Waveforms

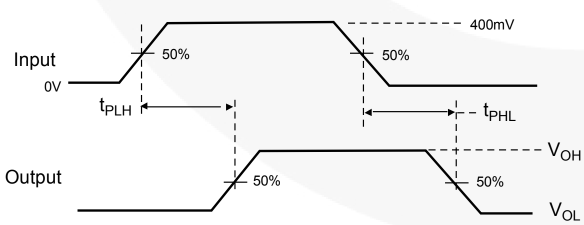


Figure 8. Propagation Delay (t_Rt_F – 500 ps)

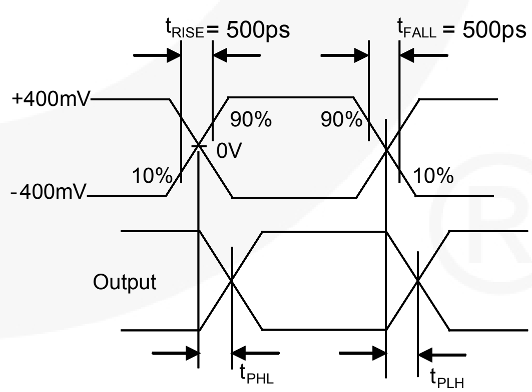
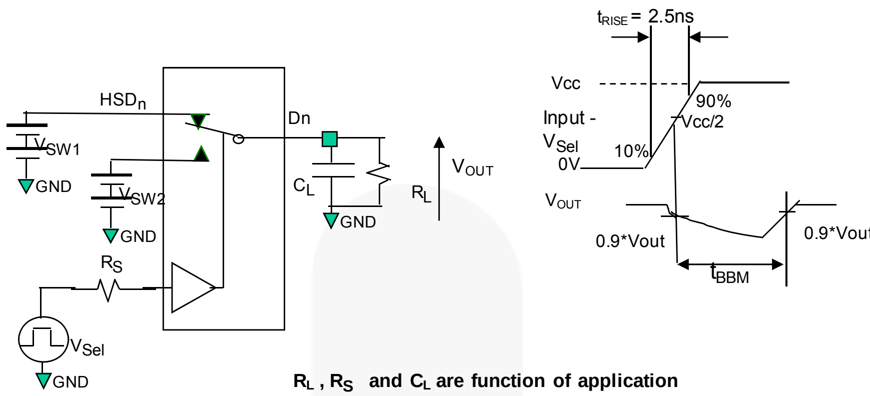


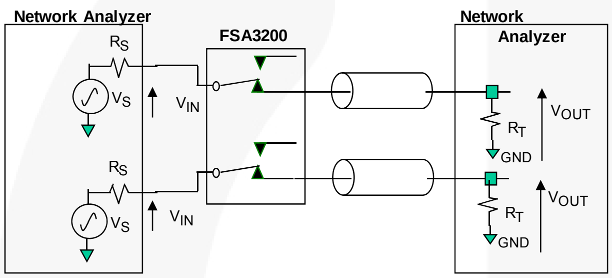
Figure 9. Intra-Pair Skew Test $t_{SK(P)}$

Test Diagrams (Continued)



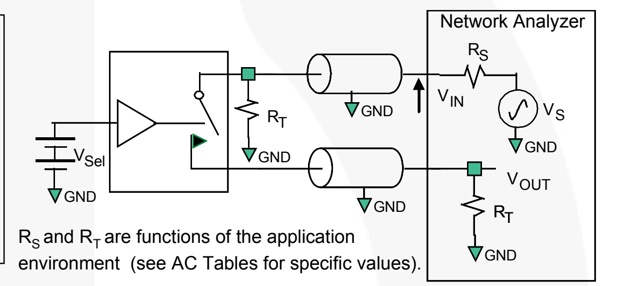
R_L, R_S and C_L are function of application environment (see AC Tables for specific values)
C_L includes test fixture and stray capacitance

Figure 10. Break-Before-Make Interval Timing



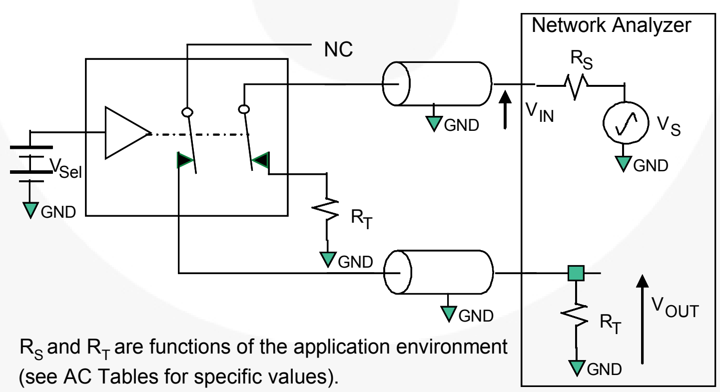
V_S, R_S and R_T are function of application environment (see AC/DC Tables for values)

Figure 11. Insertion Loss



Off isolation = 20 Log (V_{OUT} / V_{IN})

Figure 12. Channel Off Isolation



Crosstalk = 20 Log (V_{OUT} / V_{IN})

Figure 13. Non-Adjacent Channel-to-Channel Crosstalk

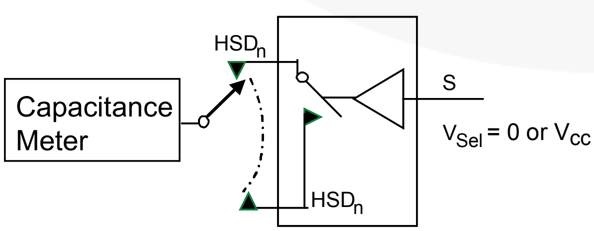


Figure 14. Channel Off Capacitance

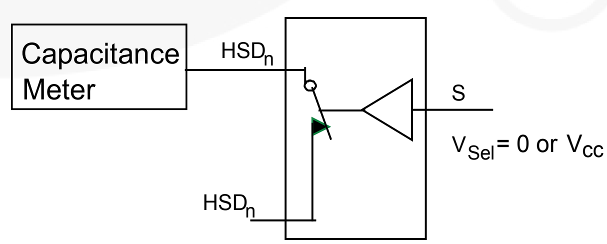


Figure 15. Channel On Capacitance

Insertion Loss

One of the key factors for using the FSA3200 in mobile digital video applications is the small amount of insertion loss experienced by the received signal as it passes through the switch. This results in minimal degradation of the received eye. One of the ways to measure the quality of the high data rate channels is using balanced ports and 4-port differential S-parameter analysis, particularly SDD21.

Bandwidth is measured using the S-parameter SDD21 methodology. Figure 16 shows the bandwidth (GHz) for the MDV path and Figure 17 the bandwidth curve for the USB path.

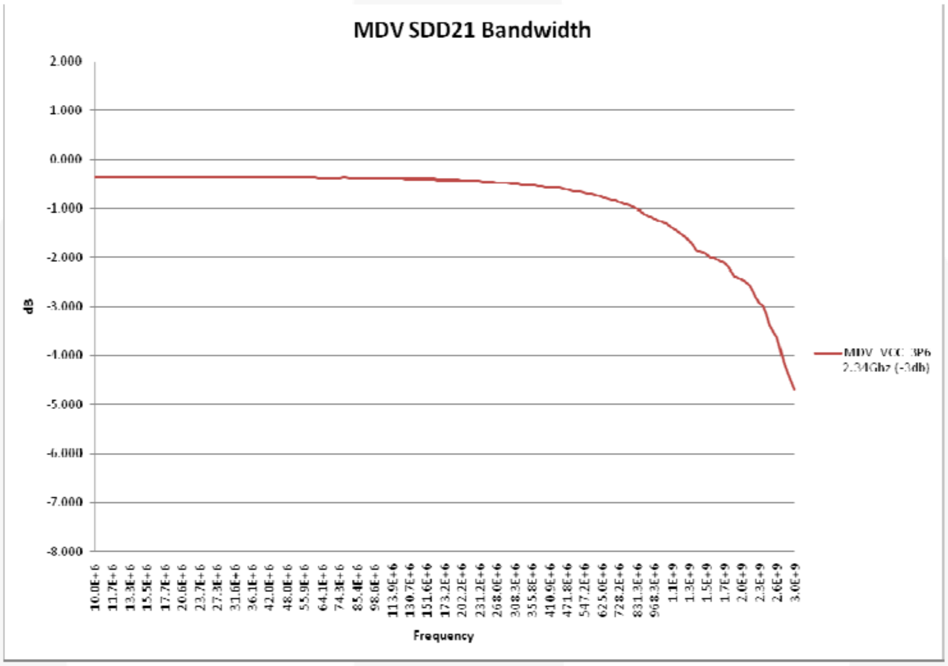


Figure 16. MDV Path SDD21 Insertion Loss Curve

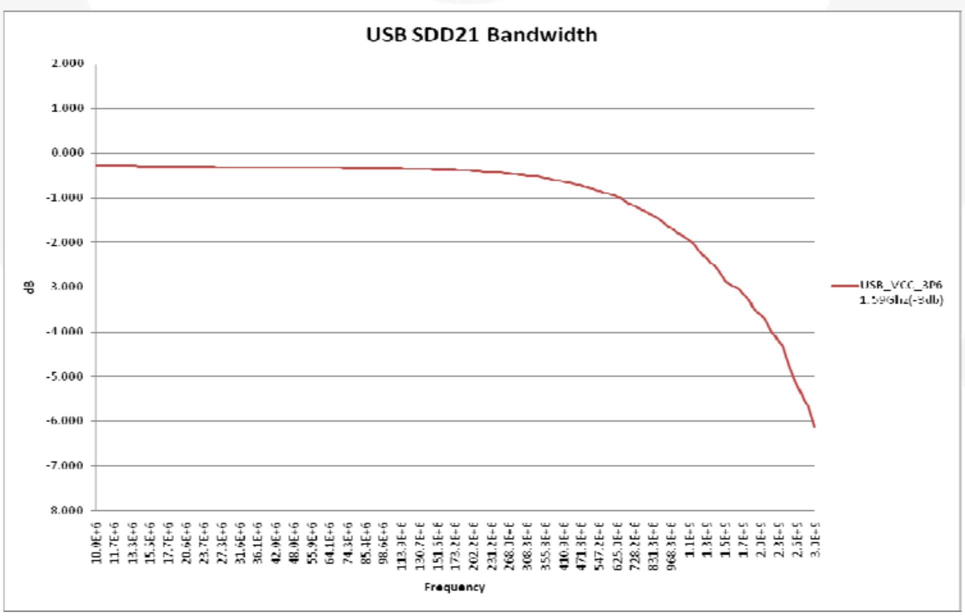


Figure 17. USB Path SDD21 Insertion Loss Curve

Typical Applications

Figure 18 shows the FSA3200 utilizing the V_{BUS} connection from the micro-USB connector. The 3M resistor is used to ensure, for manufacturing test via the micro-USB connector, that the FSA3200 configures for connectivity through the FSA9280A accessory switch. Figure 19 shows the configuration for the FSA3200 "self powered" by the battery only.

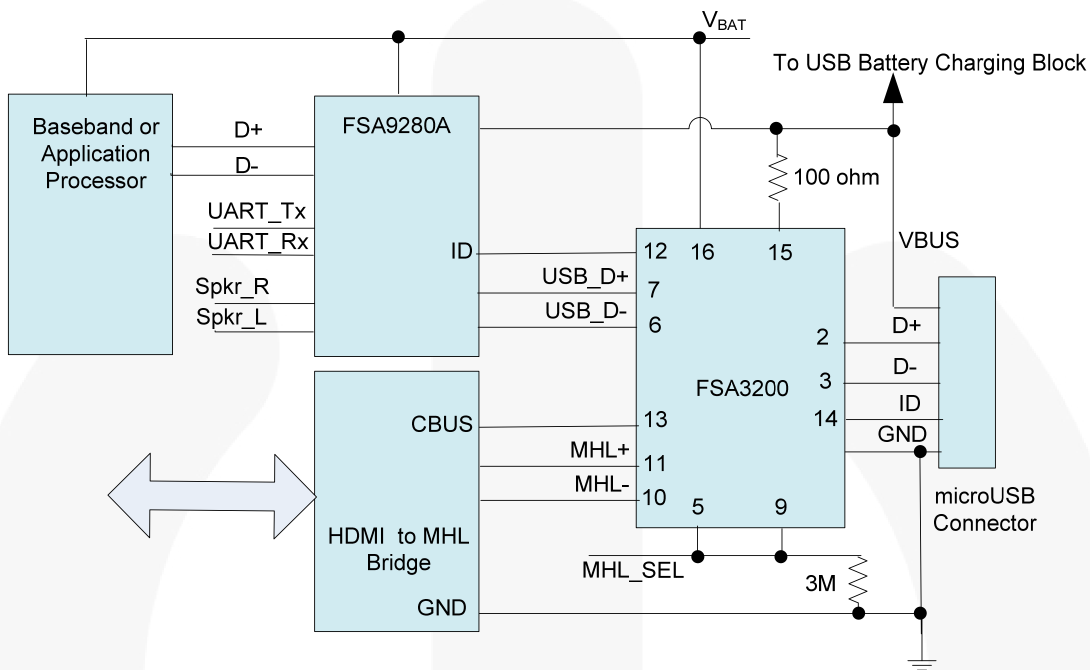


Figure 18. Typical FSA3200 Application Using V_{BUS}

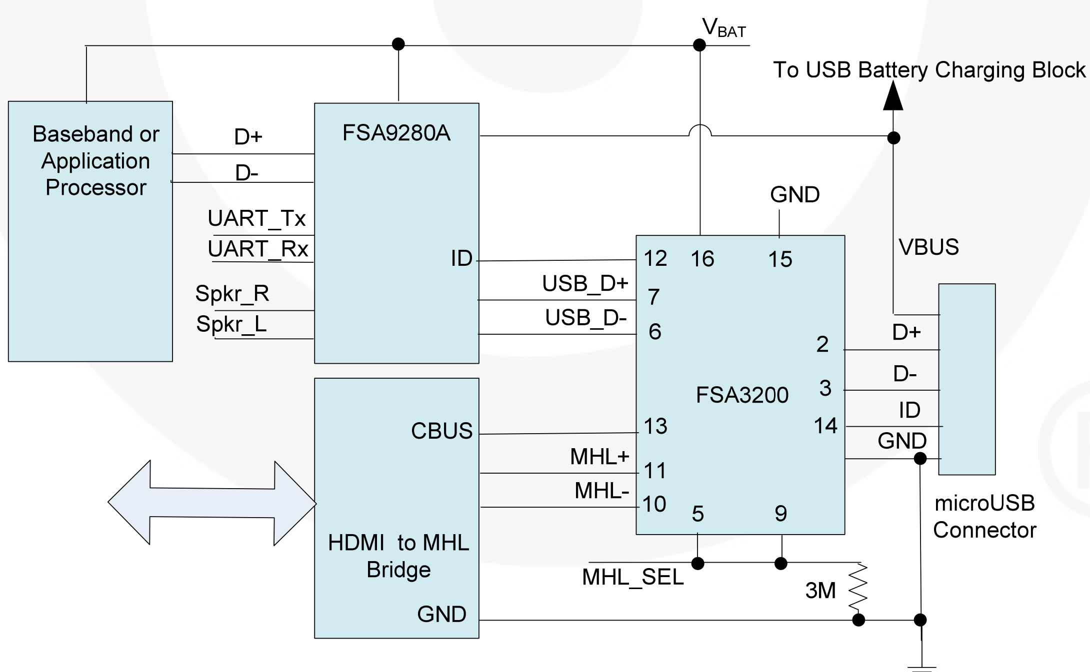
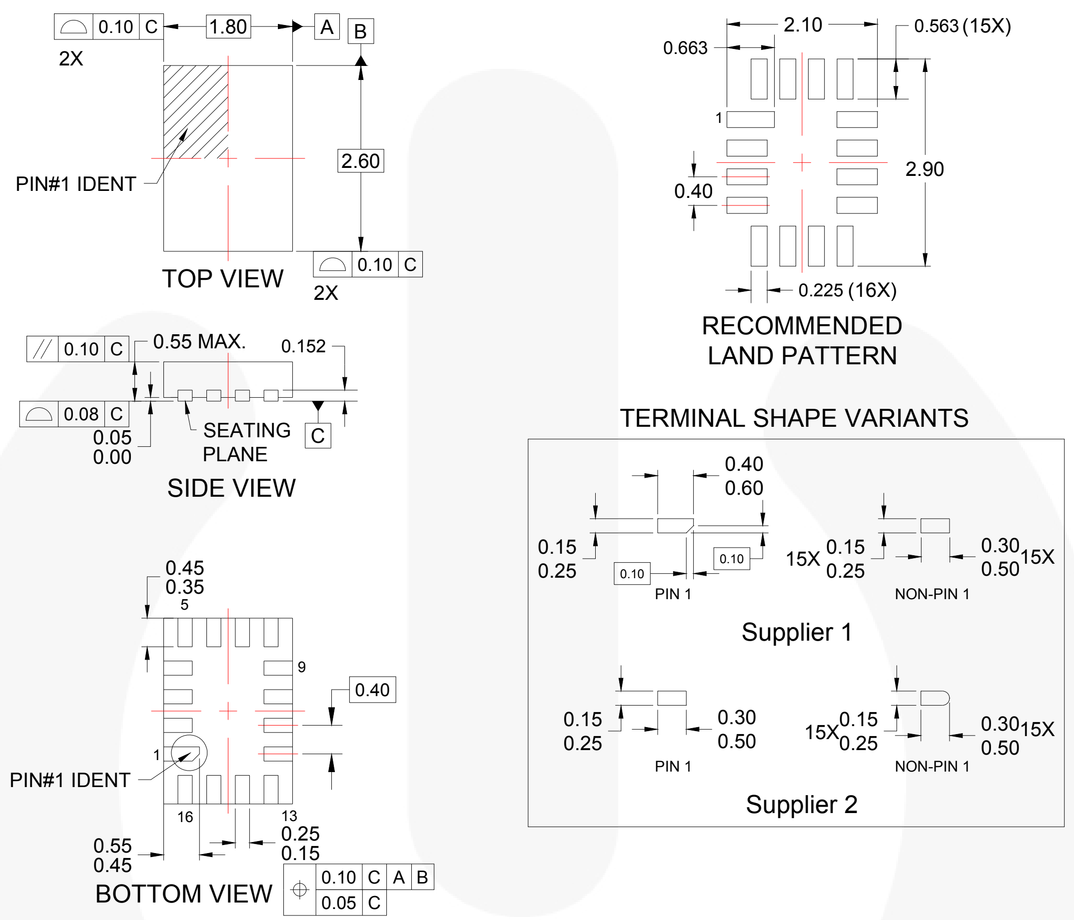
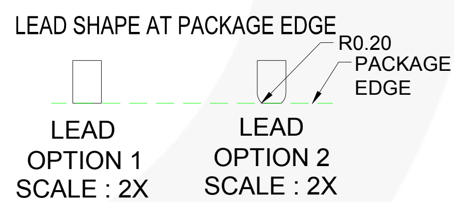


Figure 19. Typical FSA3200 "Self-Powered" Application Using V_{BAT}

Physical Dimensions





NOTES:

A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC STANDARD.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
D. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY.
E. DRAWING FILENAME: MKT-UMLP16Arev4.
F. TERMINAL SHAPE MAY VARY ACCORDING TO PACKAGE SUPPLIER, SEE TERMINAL SHAPE VARIANTS.

Figure 20. 16-Lead, Ultrathin Molded Leadless Package (UMLP)

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Dual Cool™
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Rev. I62

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