

# LM9076 150mA Ultra-Low Quiescent Current LDO Regulator with Delayed Reset Output

Check for Samples: [LM9076](#)

## FEATURES

- Available with 5.0V or 3.3V Output Voltage
- Ultra Low Ground Pin Current, 25  $\mu\text{A}$  Typical for 100  $\mu\text{A}$  Load
- $V_{\text{OUT}}$  Initial Accuracy of  $\pm 1.5\%$
- $V_{\text{OUT}}$  Accurate to  $\pm 3\%$  Over Load and Temperature Conditions
- Low Dropout Voltage, 200 mV Typical with 150 mA Load
- Low Off State Ground Pin current for LM9076BMA
- Delayed  $\overline{\text{RESET}}$  Output Pin for Low  $V_{\text{OUT}}$  Detection
- +70V/-50V Voltage Transients
- Operational  $V_{\text{IN}}$  up to +40V

## DESCRIPTION

The LM9076 is a  $\pm 3\%$ , 150 mA logic controlled voltage regulator. The regulator features an active low delayed reset output flag which can be used to reset a microprocessor system at turn-ON and in the event that the regulator output voltage falls below a minimum value. An external capacitor programs a delay time interval before the reset output pin can return high.

Designed for automotive and industrial applications, the LM9076 contains a variety of protection features such as thermal shutdown, input transient protection and a wide operating temperature range. The LM9076 uses an PNP pass transistor which allows low drop-out voltage operation.

## Typical Applications

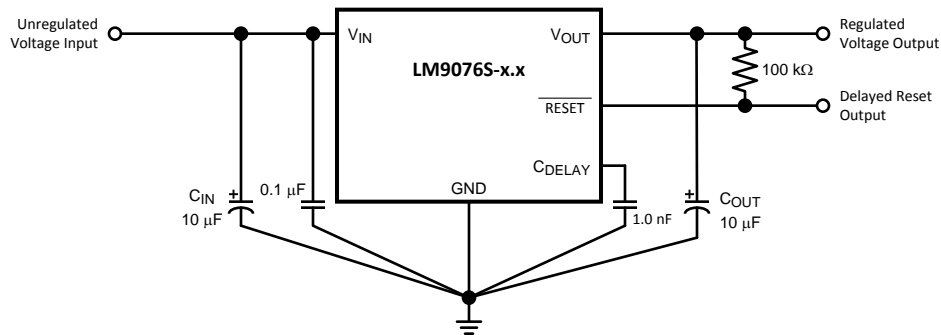


Figure 1. LM9076S-x.x in 5 lead SFM package

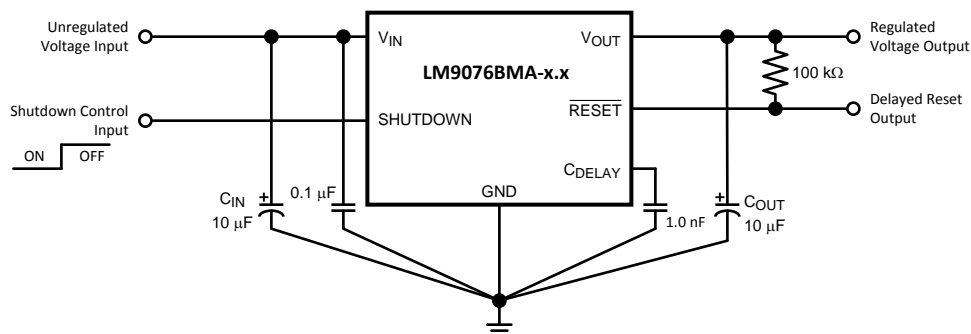


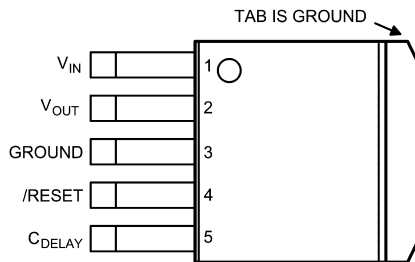
Figure 2. LM9076BMA-x.x in 8 lead SOIC package



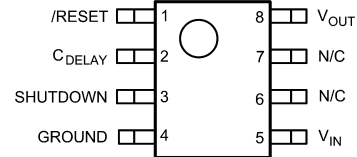
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

## Connection Diagram



**Figure 3. Top View**  
Part Numbers LM9076S-3.3 and LM9076S-5.0  
See SFM Package Number KTT0005B



**Figure 4. Top View**  
Part Numbers LM9076BMA-3.3 and  
LM9076BMA-5.0  
See SOIC Package Number D



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings<sup>(1)</sup>

$V_{IN}(DC)$	-15V to +55V
$V_{IN}(+Transient) t < 10ms, Duty Cycle < 1\%$	+70V
$V_{IN}(-Transient) t < 1ms, Duty Cycle < 1\%$	-50V
SHUTDOWN Pin	-15V to +52V
$\overline{RESET}$ Pin	-0.3V to 20V
$C_{DELAY}$ Pin	-0.3V to $V_{OUT} + 0.3V$
Storage Temperature	-65°C to +150°C
Junction Temperature ( $T_J$ )	+175°C
ESD, HBM, per AEC - Q100 - 002	+/- 2 kV
ESD, MM, per AEC - Q100 - 003	+/- 250V

(1) Absolute Maximum Ratings indicate the limits beyond which the device may cease to function, and/or damage to the device may occur.

### Operating Ratings<sup>(1)(2)</sup>

$V_{IN}$ Pin		5.35V to 40V
$V_{SHUTDOWN}$ Pin		0V to 40V
Junction Temperature		-40°C < $T_J$ < +125°C
Thermal Resistance KTT0005B <sup>(3)</sup>	$\theta_{JA}$	75°C/W
	$\theta_{JC}$	2.9°C/W
Thermal Resistance D <sup>(3)</sup>	$\theta_{JA}$	156°C/W
	$\theta_{JC}$	59°C/W

(1) Absolute Maximum Ratings indicate the limits beyond which the device may cease to function, and/or damage to the device may occur.

(2) Operating Ratings indicate conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and conditions refer to the Electrical Characteristics

(3) Worst case (FREE AIR) per EIA/JESD51-3.

### Electrical Characteristics for LM9076–3.3

The following specifications apply for  $V_{IN} = 14V$ ;  $I_{LOAD} = 10\text{ mA}$ ;  $T_J = +25^\circ\text{C}$ ;  $C_{OUT} = 10\text{ }\mu\text{F}$ ,  $0.5\Omega < \text{ESR} < 4.0\Omega$ ; unless otherwise specified. **Bold values indicate  $-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$ .** <sup>(1)(2)(3)</sup> Minimum and Maximum limits are specified through test, design or statistical correlation.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>LM9076–3.3 REGULATOR CHARACTERISTICS</b>						
$V_{OUT}$	Output Voltage		3.251	3.30	3.349	V
		$-20^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$ $1\text{ mA} \leq I_{LOAD} \leq 150\text{ mA}$	3.234	3.30	3.366	V
		$1\text{ mA} \leq I_{LOAD} \leq 150\text{ mA}$	<b>3.201</b>	<b>3.30</b>	<b>3.399</b>	V
		$V_{IN} = 60V$ , $R_{LOAD} = 1\text{ k}\Omega$ , $t \leq 40\text{ ms}$	2.970	3.30	3.630	V
	Output Voltage Off LM9076 BMA only	$V_{SHUTDOWN} \geq 2V$ , $R_{LOAD} = 1\text{ k}\Omega$	–	0	250	mV
	Reverse Battery	$V_{IN} = -15V$ , $R_{LOAD} = 1\text{ k}\Omega$	-300	0	–	mV
$\Delta V_{OUT}$	Line Regulation	$9.0V \leq V_{IN} \leq 16V$ , $I_{LOAD} = 10\text{ mA}$	–	4	25	mV
		$16V \leq V_{IN} \leq 40V$ , $I_{LOAD} = 10\text{ mA}$	–	17	35	mV
	Load Regulation	$1\text{ mA} \leq I_{LOAD} \leq 150\text{ mA}$	–	42	60	mV
$V_{DO}$	Dropout Voltage	$I_{LOAD} = 10\text{ mA}$	–	30	50	mV
		$I_{LOAD} = 50\text{ mA}$	–	80	–	mV
		$I_{LOAD} = 150\text{ mA}$	–	150	250	mV
$I_{GND}$	Ground Pin Current	$9V \leq V_{IN} \leq 16V$ , $I_{LOAD} = 100\text{ }\mu\text{A}$	–	25	45	$\mu\text{A}$
		$9V \leq V_{IN} \leq 40V$ , $I_{LOAD} = 10\text{ mA}$	–	125	160	$\mu\text{A}$
		$9V \leq V_{IN} \leq 40V$ , $I_{LOAD} = 50\text{ mA}$	–	0.6	–	mA
		$9V \leq V_{IN} \leq 16V$ , $I_{LOAD} = 150\text{ mA}$	–	3.6	4.5	mA
$I_{SC}$	$V_{OUT}$ Short Circuit Current	$V_{IN} = 14V$ , $R_{LOAD} = 1\Omega$	200	400	750	mA
PSRR	Ripple Rejection	$V_{IN} = (14V_{DC}) + (1V_{RMS} @ 120\text{ Hz})$ $I_{LOAD} = 50\text{ mA}$	50	60	–	dB
<b>RESET PIN CHARACTERISTICS</b>						
$V_{OR}$	Minimum $V_{IN}$ for valid RESET Status	(Note 3)	–	1.3	2.0	V
$V_{THR}$	$V_{OUT}$ Threshold for RESET Low	(Note 3)	0.83	0.89	0.94	$X V_{OUT}$ (Nom)
$V_{OH}$	$\overline{\text{RESET}}$ pin high voltage	External pull-up resistor to $V_{OUT} = 100\text{ k}\Omega$	$V_{OUT} \times 0.90$	$V_{OUT} \times 0.99$	$V_{OUT}$	V
$V_{OL}$	$\overline{\text{RESET}}$ pin low voltage	$C_{DELAY} < 4.0V$ , $I_{SINK} = 250\text{ }\mu\text{A}$	–	0.2	0.3	V

- (1) The regulated output voltage specification is not ensured for the entire range of  $V_{IN}$  and output loads. Device operational range is limited by the maximum junction temperature ( $T_J$ ). The junction temperature is influenced by the ambient temperature ( $T_A$ ), package selection, input voltage ( $V_{IN}$ ), and the output load current. When operating with maximum load currents the input voltage and/or ambient temperature will be limited. When operating with maximum input voltage the load current and/or the ambient temperature will be limited.
- (2) Pulse testing used maintain constant junction temperature ( $T_J$ ).
- (3) Not Production tested, Specified by Design. Minimum, Typical, and/or Maximum values are provided for informational purposes only.

### Electrical Characteristics for LM9076–3.3 (continued)

The following specifications apply for  $V_{IN} = 14V$ ;  $I_{LOAD} = 10\text{ mA}$ ;  $T_J = +25^\circ\text{C}$ ;  $C_{OUT} = 10\text{ }\mu\text{F}$ ,  $0.5\Omega < \text{ESR} < 4.0\Omega$ ; unless otherwise specified. **Bold values indicate  $-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$ .** <sup>(1)(2)(3)</sup> Minimum and Maximum limits are specified through test, design or statistical correlation.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>C<sub>DELAY</sub> PIN CHARACTERISTICS</b>						
$I_{DELAY}$	C <sub>DELAY</sub> Charging Current	$V_{IN} = 14V$ , $V_{DELAY} = 0V$	-0.70	-0.42	-0.25	$\mu\text{A}$
$V_{OL}$	C <sub>DELAY</sub> pin low voltage	$V_{OUT} < 4.0V$ , $I_{SINK} = I_{DELAY}$	–	0.100	–	V
$t_{DELAY}$	Reset Delay Time	$V_{IN} = 14V$ , $C_{DELAY} = 0.001\text{ }\mu\text{F}$ $V_{OUT}$ rising from 0V, $\Delta t$ from $V_{OUT} > V_{OR}$ to RESET pin HIGH	4.7	7.8	13.2	ms

### Electrical Characteristics for LM9076–5.0

The following specifications apply for  $V_{IN} = 14V$ ;  $V_{SHUTDOWN} = \text{Open}$ ;  $I_{LOAD} = 10\text{ mA}$ ;  $T_J = +25^\circ\text{C}$ ;  $C_{OUT} = 10\text{ }\mu\text{F}$ ,  $0.5\Omega < \text{ESR} < 4.0\Omega$ ; unless otherwise specified. **Bold Values indicate  $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ .** <sup>(1)(2)(3)</sup> Minimum and Maximum limits are specified through test, design, or statistical correlation.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>LM9076–5.0 REGULATOR CHARACTERISTICS</b>						
$V_{OUT}$	Output Voltage	$-20^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$ $1\text{ mA} \leq I_{LOAD} \leq 150\text{ mA}$	4.925	5.00	5.075	V
		$1\text{ mA} \leq I_{LOAD} \leq 150\text{ mA}$	4.900	5.00	5.100	V
		<b>4.850</b>	<b>5.00</b>	<b>5.150</b>	V	
		$V_{IN} = 60V$ , $R_{LOAD} = 1\text{ k}\Omega$ , $t \leq 40\text{ms}$	4.500	5.00	5.500	V
	Output Voltage Off LM9076 BMA only	$V_{SHUTDOWN} \geq 2V$ , $R_{LOAD} = 1\text{ k}\Omega$	–	0	250	mV
Reverse Battery	$V_{IN} = -15V$ , $R_{LOAD} = 1\text{ k}\Omega$	-300	0	–	mV	
$\Delta V_{OUT}$	Line Regulation	$9.0V \leq V_{IN} \leq 16V$ , $I_{LOAD} = 10\text{ mA}$	–	4	25	mV
		$16V \leq V_{IN} \leq 40V$ , $I_{LOAD} = 10\text{ mA}$	–	17	35	mV
	Load Regulation	$1\text{ mA} \leq I_{LOAD} \leq 150\text{ mA}$	–	42	60	mV
$V_{DO}$	Dropout Voltage	$I_{LOAD} = 10\text{ mA}$	–	30	50	mV
		$I_{LOAD} = 50\text{ mA}$	–	80	–	mV
		$I_{LOAD} = 150\text{ mA}$	–	150	250	mV
$I_{GND}$	Ground Pin Current	$9V \leq V_{IN} \leq 16V$ , $I_{LOAD} = 100\text{ }\mu\text{A}$	–	25	45	$\mu\text{A}$
		$9V \leq V_{IN} \leq 40V$ , $I_{LOAD} = 10\text{ mA}$	–	125	160	$\mu\text{A}$
		$9V \leq V_{IN} \leq 40V$ , $I_{LOAD} = 50\text{ mA}$	–	0.6	–	mA
		$9V \leq V_{IN} \leq 16V$ , $I_{LOAD} = 150\text{ mA}$	–	3.6	4.5	mA
	Ground Pin Current in Shutdown Mode	$9V \leq V_{IN} \leq 40V$ , $V_{SHUTDOWN} = 2V$	–	15	25	$\mu\text{A}$

(1) Pulse testing used maintain constant junction temperature ( $T_J$ ).

(2) The regulated output voltage specification is not ensured for the entire range of  $V_{IN}$  and output loads. Device operational range is limited by the maximum junction temperature ( $T_J$ ). The junction temperature is influenced by the ambient temperature ( $T_A$ ), package selection, input voltage ( $V_{IN}$ ), and the output load current. When operating with maximum load currents the input voltage and/or ambient temperature will be limited. When operating with maximum input voltage the load current and/or the ambient temperature will be limited.

(3) Not Production tested, Specified by Design. Minimum, Typical, and/or Maximum values are provided for informational purposes only.

**Electrical Characteristics for LM9076–5.0 (continued)**

The following specifications apply for  $V_{IN} = 14V$ ;  $V_{SHUTDOWN} = \text{Open}$ ;  $I_{LOAD} = 10 \text{ mA}$ ;  $T_J = +25^\circ\text{C}$ ;  $C_{OUT} = 10 \mu\text{F}$ ,  $0.5\Omega < \text{ESR} < 4.0\Omega$ ; unless otherwise specified. **Bold Values indicate  $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ .**<sup>(1)(2)(3)</sup> Minimum and Maximum limits are specified through test, design, or statistical correlation.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{SC}$	$V_{OUT}$ Short Circuit Current	$V_{IN} = 14V$ , $R_{LOAD} = 1\Omega$	200	400	750	mA
PSRR	Ripple Rejection	$V_{IN} = (14V_{DC}) + (1V_{RMS} @ 120\text{Hz})$ $I_{LOAD} = 50 \text{ mA}$	50	60	–	dB
<b>RESET PIN CHARACTERISTICS</b>						
$V_{OR}$	Minimum $V_{IN}$ for valid RESET Status	(Note 3)	–	1.3	2.0	V
$V_{THR}$	$V_{OUT}$ Threshold for RESET Low	(Note 3)	0.83	0.89	0.94	X $V_{OUT}$ (Nom)
$V_{OH}$	$\overline{\text{RESET}}$ pin high voltage	External pull-up resistor to $V_{OUT} = 100 \text{ k}\Omega$	$V_{OUT} \times 0.90$	$V_{OUT} \times 0.99$	$V_{OUT}$	V
$V_{OL}$	$\overline{\text{RESET}}$ pin low voltage	$C_{DELAY} < 4.0V$ , $I_{SINK} = 250 \mu\text{A}$	–	0.2	0.3	V
<b><math>C_{DELAY}</math> PIN CHARACTERISTICS</b>						
$I_{DELAY}$	$C_{DELAY}$ Charging Current	$V_{IN} = 14V$ , $V_{DELAY} = 0V$	-0.70	-0.42	-0.25	$\mu\text{A}$
$V_{OL}$	$C_{DELAY}$ pin low voltage	$V_{OUT} < 4.0V$ , $I_{SINK} = I_{DELAY}$	–	0.100	–	V
$t_{DELAY}$	Reset Delay Time	$V_{IN} = 14V$ , $C_{DELAY} = 0.001 \mu\text{F}$ $V_{OUT}$ rising from 0V, $\Delta t$ from $V_{OUT} > V_{OR}$ to RESET pin HIGH	7.1	11.9	20.0	ms
<b>SHUTDOWN CONTROL LOGIC — LM9076BMA-5.0 Only</b>						
$V_{IL(SD)}$	SHUTDOWN Pin Low Threshold Voltage	$V_{SHUTDOWN}$ pin falling from 5.0V until $V_{OUT} > 4.5V$ ( $V_{OUT} = \text{On}$ )	1	1.5	–	V
$V_{IH(SD)}$	SHUTDOWN Pin High Threshold Voltage	$V_{SHUTDOWN}$ pin rising from 0V until $V_{OUT} < 0.5V$ ( $V_{OUT} = \text{Off}$ )	–	1.5	2	V
$I_{IH(SD)}$	SHUTDOWN Pin High Bias Current	$V_{SHUTDOWN} = 40V$	–	35	–	$\mu\text{A}$
		$V_{SHUTDOWN} = 5V$	–	15	35	$\mu\text{A}$
		$V_{SHUTDOWN} = 2V$	–	6	10	$\mu\text{A}$
$I_{IL(SD)}$	SHUTDOWN Pin Low Bias Current	$V_{SHUTDOWN} = 0V$	–	0	–	$\mu\text{A}$

Typical Performance Characteristics

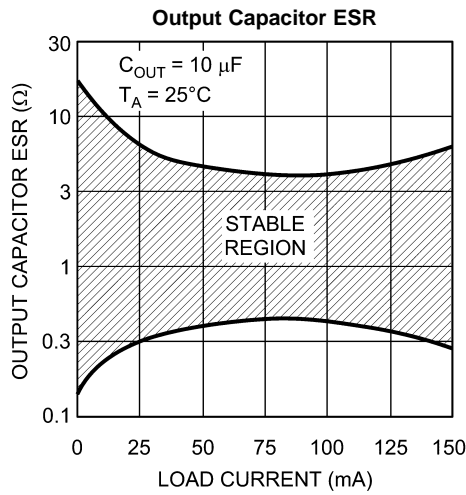


Figure 5.

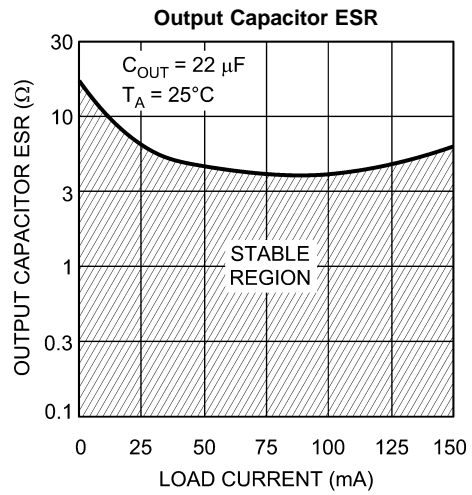


Figure 6.

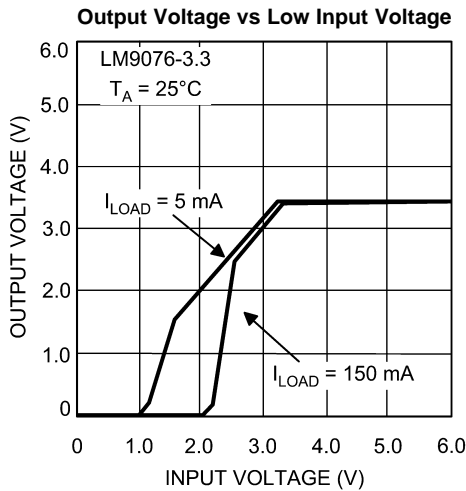


Figure 7.

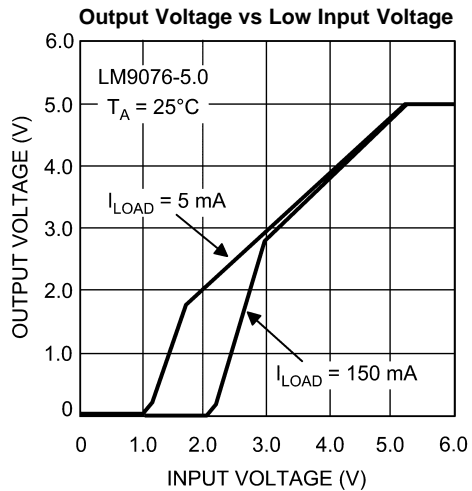


Figure 8.

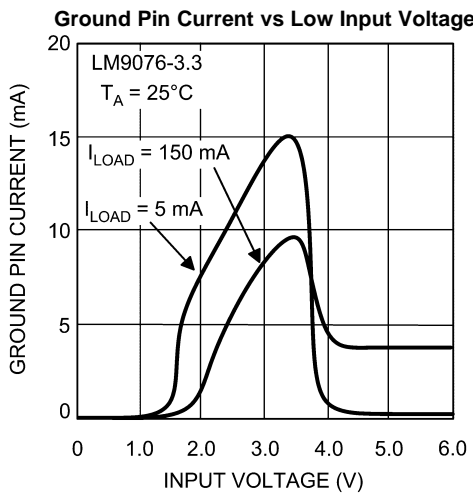


Figure 9.

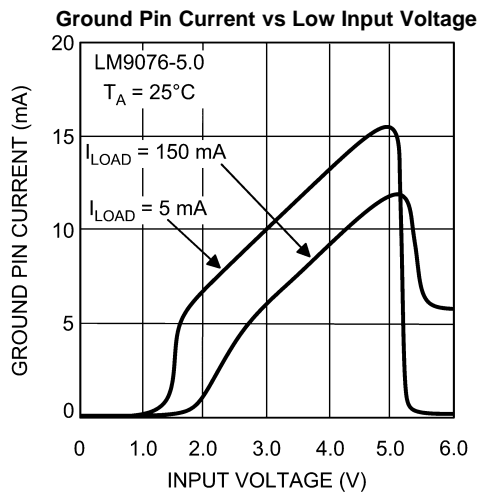


Figure 10.

Typical Performance Characteristics (continued)

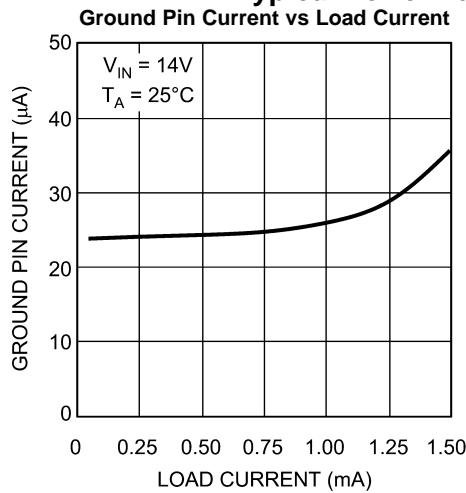


Figure 11.

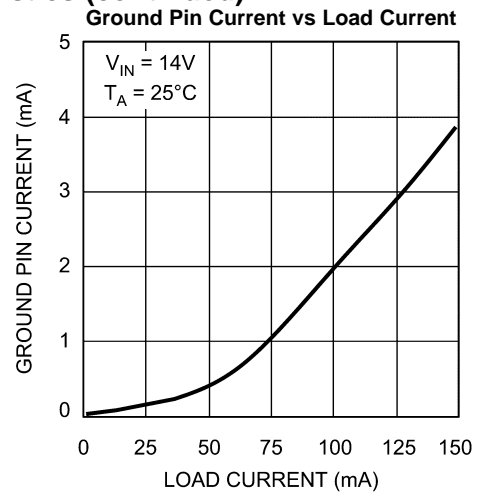


Figure 12.

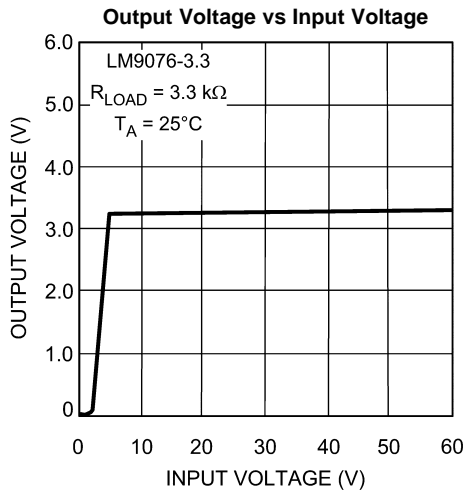


Figure 13.

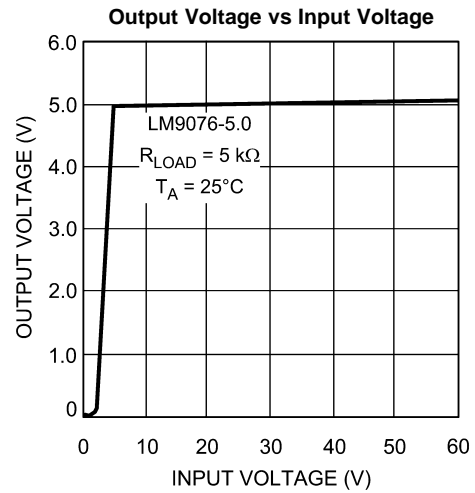


Figure 14.

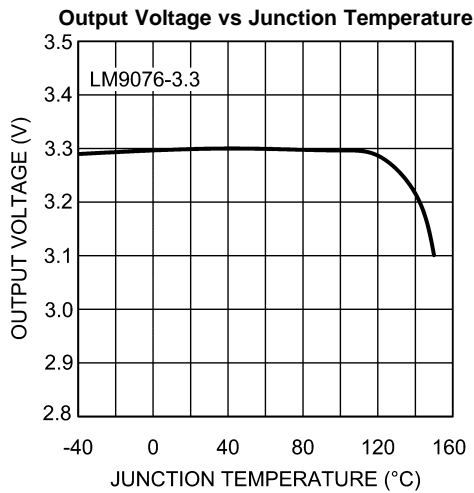


Figure 15.

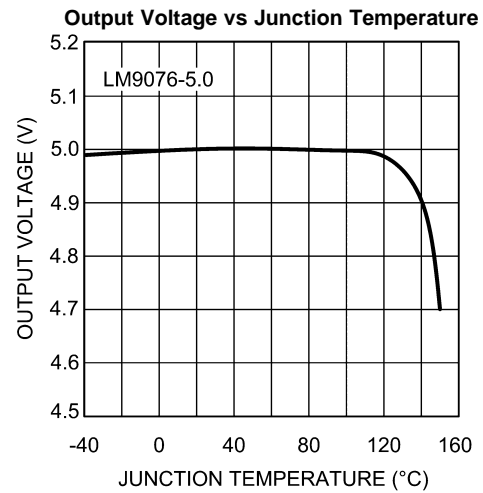


Figure 16.

**Typical Performance Characteristics (continued)**

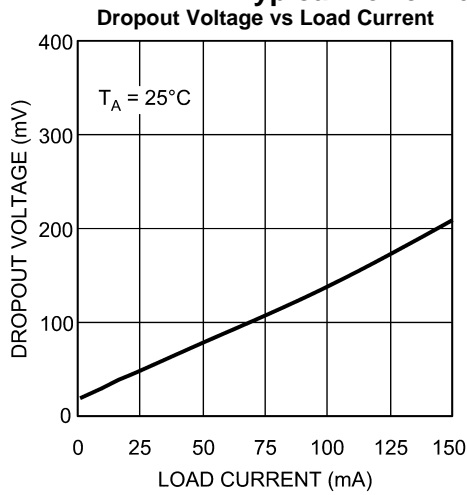


Figure 17.

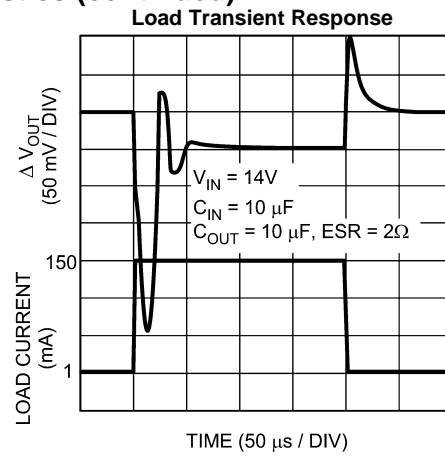


Figure 18.

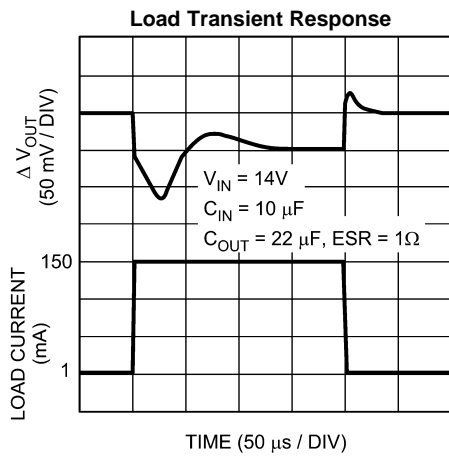


Figure 19.

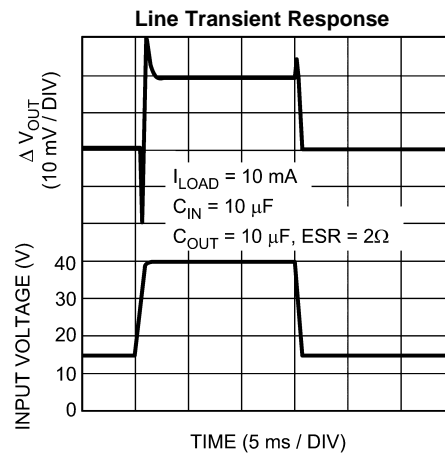


Figure 20.

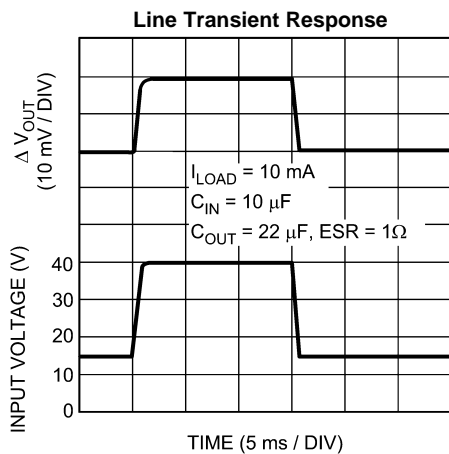


Figure 21.

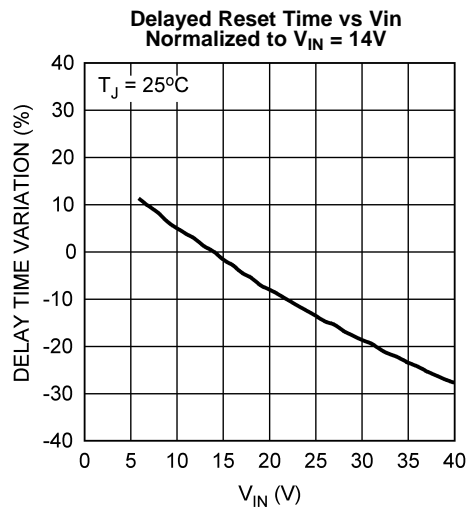
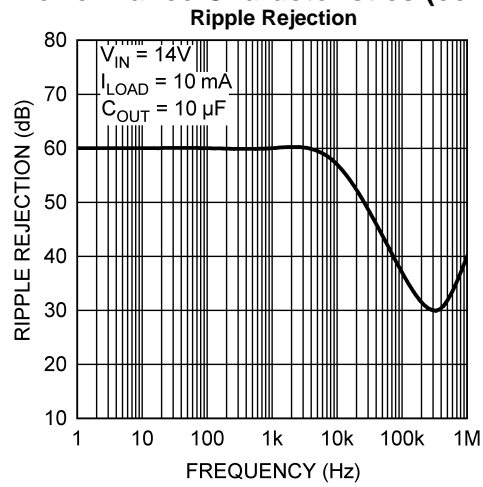


Figure 22.



**Typical Performance Characteristics (continued)**



**Figure 23.**

## APPLICATION INFORMATION

### REGULATOR BASICS

The LM9076 regulator is suitable for Automotive and Industrial applications where continuous connection to a battery supply is required (refer to [Typical Applications](#)).

The pass element of the regulator is a PNP device which requires an output bypass capacitor for stability. The minimum bypass capacitance for the output is 10  $\mu\text{F}$  (refer to ESR limitations). A 22  $\mu\text{F}$ , or larger, output bypass capacitor is recommended for typical applications

### INPUT CAPACITOR

The LM9076 requires a low source impedance to maintain regulator stability because critical portions of the internal bias circuitry are connected to directly to  $V_{\text{IN}}$ . In general, a 10  $\mu\text{F}$  electrolytic capacitor, located within two inches of the LM9076, is adequate for a majority of applications. Additionally, and at a minimum, a 0.1  $\mu\text{F}$  ceramic capacitor should be located between the LM9076  $V_{\text{IN}}$  and Ground pin, and as close as is physically possible to the LM9076 itself .

### OUTPUT CAPACITOR

An output bypass capacitor is required for stability. This capacitance must be placed between the LM9076  $V_{\text{OUT}}$  pin and Ground pin, as close as is physically possible, using traces that are not part of the load current path.

The output capacitor must meet the requirements for minimum capacitance and also maintain the appropriate ESR value across the entire operating ambient temperature range. There is no limit to the maximum output capacitance as long as ESR is maintained.

The minimum bypass capacitance for the output is 10  $\mu\text{F}$  (refer to ESR limitations). A 22  $\mu\text{F}$ , or larger, output bypass capacitor is recommended for typical applications.

Solid tantalums capacitors are recommended as they generally maintain capacitance and ESR ratings over a wide temperature range. Ceramic capacitor types XR7 and XR5 may be used if a series resistor is added to simulate the minimum ESR requirement. See [Figure 24](#).

Aluminum electrolytic capacitors are not recommended as they are subject to wide changes in capacitance and ESR across temperature.

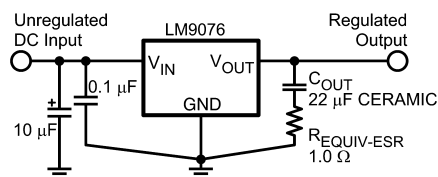


Figure 24. Using Low ESR Capacitors

### DELAY CAPACITOR

The capacitor on the Delay pin must be a low leakage type since the charge current is minimal (420 nA typical) and the pin must fully charge to  $V_{\text{OUT}}$ . Ceramic, Mylar, and polystyrene capacitor types are generally recommended, although changes in capacitance values across temperature changes will have some effect on the delay timing.

Any leakage of the  $I_{\text{DELAY}}$  current, be it through the delay capacitor or any other path, will extend the delay time, possibly to the point that the Reset pin output does not go high.

### SHUTDOWN PIN - LM9076BMA ONLY

The basic On/Off control of the regulator is accomplished with the SHUTDOWN pin. By pulling the SHUTDOWN pin high the regulator output is switched Off. When the regulator is switched Off the load on the battery will be primarily due to the SHUTDOWN pin current.

When the SHUTDOWN pin is low, or left open, the regulator is switched On. When an unregulated supply, such as V BATTERY , is used to pull the SHUTDOWN pin high a series resistor in the range of 10KΩ to 50KΩ is recommended to provide reverse voltage transient protection of the SHUTDOWN pin. Adding a small capacitor (0.001uF typical) from the SHUTDOWN pin to Ground will add noise immunity to prevent accidental turn on due to noise on the supply line.

## RESET FLAG

The  $\overline{\text{RESET}}$  pin is an open collector output which requires an external pull-up resistor to develop the reset signal. The external pull-up resistor should be in the range of 10 kΩ to 200 kΩ.

At  $V_{\text{IN}}$  values of less than typically 2V the  $\overline{\text{RESET}}$  pin voltage will be high. For  $V_{\text{IN}}$  values between typically 2V and approximately  $V_{\text{OUT}} + V_{\text{BE}}$  the  $\overline{\text{RESET}}$  pin voltage will be low. For  $V_{\text{IN}}$  values greater than approximately  $V_{\text{OUT}} + V_{\text{BE}}$  the  $\overline{\text{RESET}}$  pin voltage will be dependent on the status of the  $V_{\text{OUT}}$  pin voltage and the Delayed Reset circuitry. The value of  $V_{\text{BE}}$  is typically 600 mV at 25°C and will decrease approximately 2 mV for every 1°C increase in the junction temperature. During normal operation the  $\overline{\text{RESET}}$  pin voltage will be high .

Any load condition that causes the  $V_{\text{OUT}}$  pin voltage to drop below typically 89% of normal will activate the Delayed Reset circuit and the  $\overline{\text{RESET}}$  pin will go low for the duration of the delay time.

Any line condition that causes  $V_{\text{IN}}$  pin voltage to drop below typically  $V_{\text{OUT}} + V_{\text{BE}}$  will cause the  $\overline{\text{RESET}}$  pin to go low without activating the Delayed Reset circuitry.

Excessive thermal dissipation will raise the junction temperature and could activate the Thermal Shutdown circuitry which, in turn, will cause the  $\overline{\text{RESET}}$  pin to go low.

For the LM9076BMA devices, pulling the SHUTDOWN pin high will turn off the output which, in turn, will cause the  $\overline{\text{RESET}}$  pin to go low once the  $V_{\text{OUT}}$  voltage has decayed to a value that is less than typically 89% of normal. See [Figure 25](#).

## RESET DELAY TIME

When the regulator output is switched On, or after recovery from brief  $V_{\text{OUT}}$  fault condition, the  $\overline{\text{RESET}}$  flag can be programmed to remain low for an additional delay time. This will give time for any system reference voltages, clock signals, etc., to stabilize before the micro-controller resumes normal operation.

This delay time is controlled by the capacitor value on the  $C_{\text{DELAY}}$  pin. During normal operation the  $C_{\text{DELAY}}$  capacitor is charged to near  $V_{\text{OUT}}$  . When a  $V_{\text{OUT}}$  fault causes the  $\overline{\text{RESET}}$  pin to go low, the  $C_{\text{DELAY}}$  capacitor is quickly discharged to ground. When the  $V_{\text{OUT}}$  fault is removed, and  $V_{\text{OUT}}$  returns to the normal operating value, the  $C_{\text{DELAY}}$  capacitor begins charging at a typical constant 0.420 uA rate. When the voltage on the  $C_{\text{DELAY}}$  capacitor reaches the same potential as the  $V_{\text{OUT}}$  pin the  $\overline{\text{RESET}}$  pin will be allowed to return high.

The typical  $\overline{\text{RESET}}$  delay time can be calculated with the following formula:

$$t_{\text{DELAY}} = V_{\text{OUT}} \times (C_{\text{DELAY}} / I_{\text{DELAY}}) \quad (1)$$

For the LM9076–3.3 with a  $C_{\text{DELAY}}$  value of 0.001 uF and a  $I_{\text{DELAY}}$  value of 0.420 uA the typical  $\overline{\text{RESET}}$  delay time is:

$$t_{\text{DELAY}} = 3.3\text{V} \times (0.001 \text{ uF} / 0.420 \text{ uA}) = 7.8 \text{ ms} \quad (2)$$

For the LM9076–5.0 with a  $C_{\text{DELAY}}$  value of 0.001 uF and a  $I_{\text{DELAY}}$  value of 0.420 uA the typical  $\overline{\text{RESET}}$  delay time is:

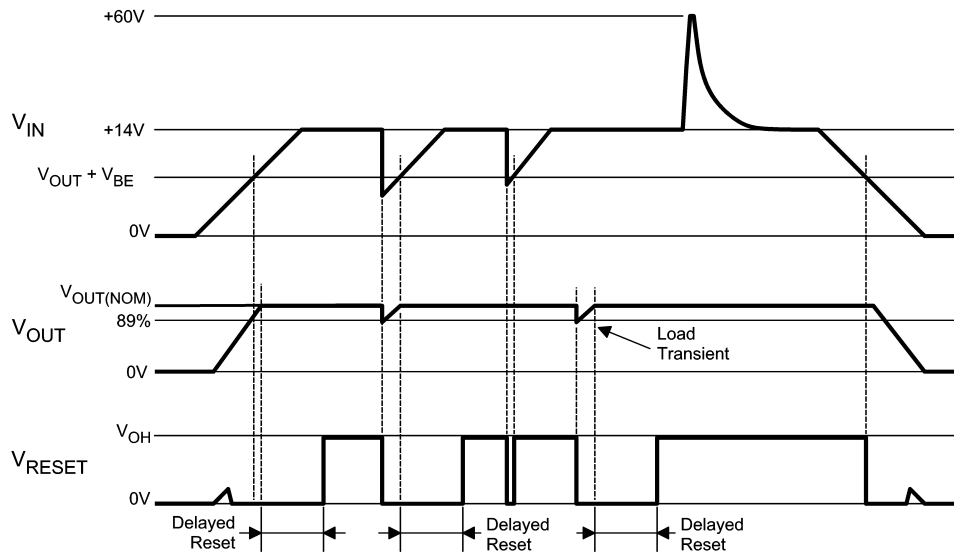
$$t_{\text{DELAY}} = 5.0\text{V} \times (0.001\text{uF} / 0.420\text{uA}) = 11.9 \text{ ms} \quad (3)$$

## THERMAL PROTECTION

Device operational range is limited by the maximum junction temperature ( $T_J$ ). The junction temperature is influenced by the ambient temperature ( $T_A$ ), package selection, input voltage ( $V_{IN}$ ), and the output load current. When operating with maximum load currents the input voltage and/or ambient temperature will be limited. When operating with maximum input voltage the load current and/or the ambient temperature will be limited.

Even though the LM9076 is equipped with circuitry to protect itself from excessive thermal dissipation, it is not recommended that the LM9076 be operated at, or near, the maximum recommended die junction temperature ( $T_J$ ) as this may impair long term device reliability.

The thermal protection circuitry monitors the temperature at the die level. When the die temperature exceeds typically  $160^\circ\text{C}$  the voltage regulator output will be switched off.



**Figure 25. Typical Reset Pin Operational Waveforms**

---

**REVISION HISTORY**

<b>Changes from Revision K (March 2013) to Revision L</b>	<b>Page</b>
<hr/> <ul style="list-style-type: none"><li>• Changed layout of National Data Sheet to TI format .....</li></ul> <hr/>	<hr/> <a href="#">12</a> <hr/>

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM9076BMA-3.3/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	9076B MA3.3	<a href="#">Samples</a>
LM9076BMA-5.0	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 125	9076B MA5.0	
LM9076BMA-5.0/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	9076B MA5.0	<a href="#">Samples</a>
LM9076BMAX-3.3/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	9076B MA3.3	<a href="#">Samples</a>
LM9076BMAX-5.0/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	9076B MA5.0	<a href="#">Samples</a>
LM9076S-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	SN	Level-3-245C-168 HR	-40 to 125	LM9076S -3.3	<a href="#">Samples</a>
LM9076S-5.0	NRND	DDPAK/ TO-263	KTT	5	45	TBD	Call TI	Call TI	-40 to 125	LM9076S -5.0	
LM9076S-5.0/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	SN	Level-3-245C-168 HR	-40 to 125	LM9076S -5.0	<a href="#">Samples</a>
LM9076SX-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	SN	Level-3-245C-168 HR	-40 to 125	LM9076S -3.3	<a href="#">Samples</a>
LM9076SX-5.0/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	SN	Level-3-245C-168 HR	-40 to 125	LM9076S -5.0	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM9076BMAX-3.3/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM9076BMAX-5.0/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM9076SX-3.3/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LM9076SX-5.0/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM9076BMAX-3.3/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM9076BMAX-5.0/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM9076SX-3.3/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LM9076SX-5.0/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



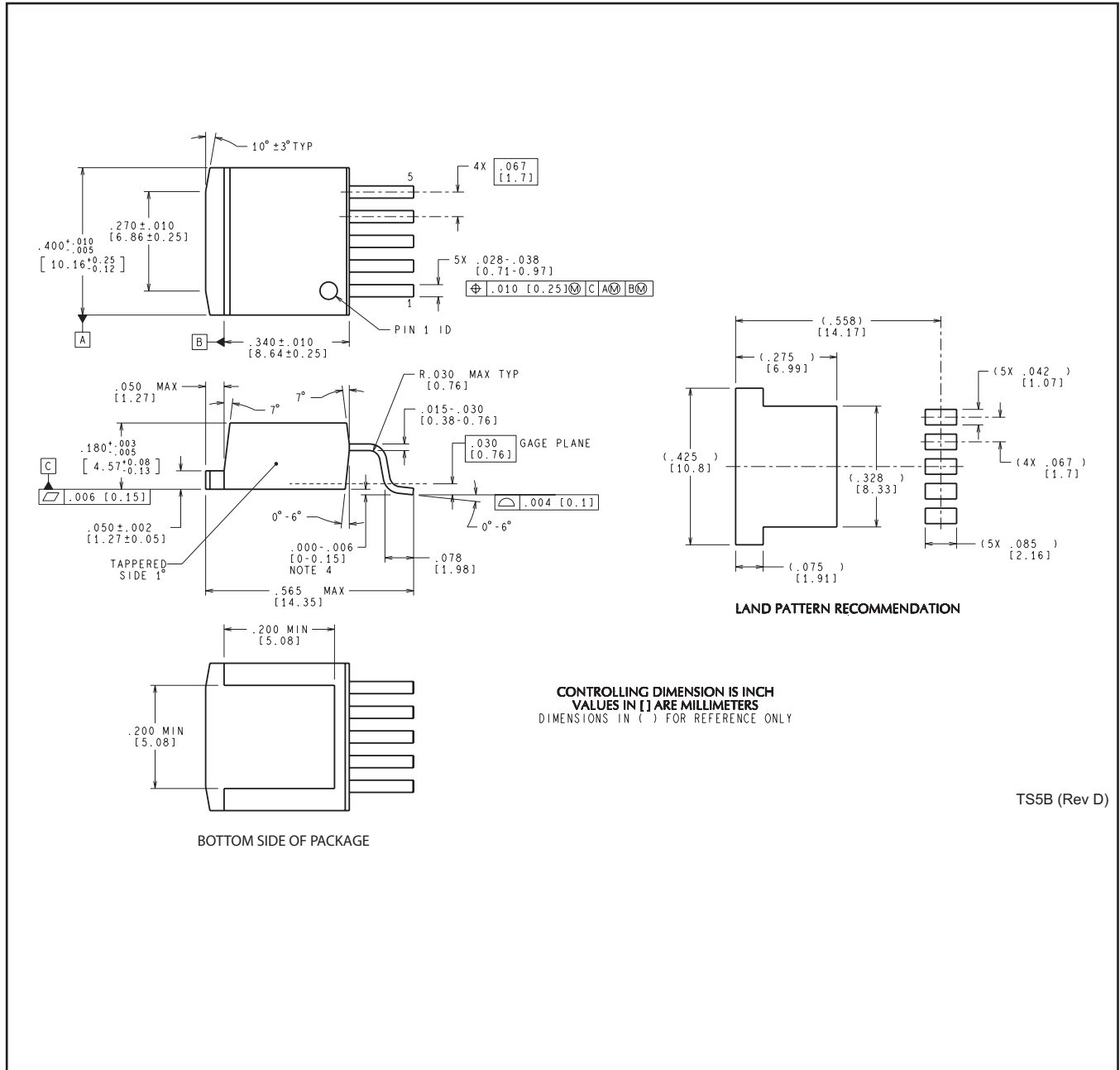
SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

KTT0005B



CONTROLLING DIMENSION IS INCH  
 VALUES IN [ ] ARE MILLIMETERS  
 DIMENSIONS IN ( ) FOR REFERENCE ONLY

TS5B (Rev D)

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2020, Texas Instruments Incorporated