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October 2014

# FDMS7694

## N-Channel PowerTrench<sup>®</sup> MOSFET

30 V, 9.5 mΩ

### Features

- Max  $r_{DS(on)}$  = 9.5 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 13.2\text{ A}$
- Max  $r_{DS(on)}$  = 14.5 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 10.5\text{ A}$
- Advanced Package and Silicon combination for low  $r_{DS(on)}$  and high efficiency
- Next generation enhanced body diode technology, engineered for soft recovery
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

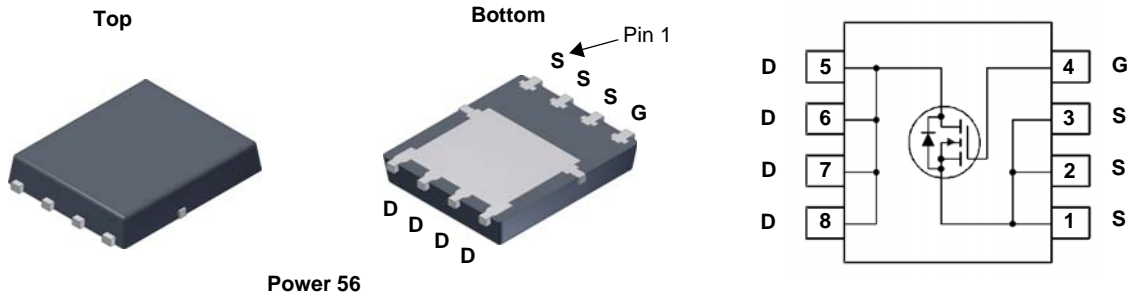


### General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $r_{DS(on)}$ , fast switching speed and body diode reverse recovery performance.

### Applications

- IMVP Vcore Switching for Notebook
- VRM Vcore Switching for Desktop and server
- OringFET / Load Switching
- DC-DC Conversion



### MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage (Note 4)	$\pm 20$	V
$I_D$	Drain Current -Continuous (Package limited) $T_C = 25\text{ °C}$	20	A
	-Continuous (Silicon limited) $T_C = 25\text{ °C}$	44	
	-Continuous $T_A = 25\text{ °C}$ (Note 1a)	13.2	
	-Pulsed	50	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	21	mJ
$P_D$	Power Dissipation $T_C = 25\text{ °C}$	27	W
	Power Dissipation $T_A = 25\text{ °C}$ (Note 1a)	2.5	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^{\circ}\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	4.5	$^{\circ}\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS7694	FDMS7694	Power 56	13 "	12 mm	3000 units

FDMS7694 N-Channel PowerTrench<sup>®</sup> MOSFET

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}, V_{GS} = 0\ \text{V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , referenced to $25^\circ\text{C}$		16		mV/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\ \text{V}, V_{GS} = 0\ \text{V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current, Forward	$V_{GS} = 20\ \text{V}, V_{DS} = 0\ \text{V}$			100	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.0	2.0	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , referenced to $25^\circ\text{C}$		-6		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}, I_D = 13.2\ \text{A}$		7.6	9.5	m $\Omega$
		$V_{GS} = 4.5\ \text{V}, I_D = 10.5\ \text{A}$		11.1	14.5	
		$V_{GS} = 10\ \text{V}, I_D = 13.2\ \text{A}, T_J = 125^\circ\text{C}$		10.6	13.3	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\ \text{V}, I_D = 13.2\ \text{A}$		55		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 15\ \text{V}, V_{GS} = 0\ \text{V}, f = 1\ \text{MHz}$		1060	1410	pF
$C_{oss}$	Output Capacitance			353	470	pF
$C_{rss}$	Reverse Transfer Capacitance			36	55	pF
$R_g$	Gate Resistance			0.8	1.6	$\Omega$

### Switching Characteristics

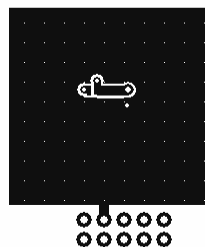
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\ \text{V}, I_D = 13.2\ \text{A}, V_{GS} = 10\ \text{V}, R_{GEN} = 6\ \Omega$		8.4	17	ns
$t_r$	Rise Time			2	10	ns
$t_{d(off)}$	Turn-Off Delay Time			18	33	ns
$t_f$	Fall Time			1.6	10	ns
$Q_g$	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $10\ \text{V}$	$V_{DD} = 15\ \text{V}, I_D = 13.2\ \text{A}$	15	22	nC
$Q_g$	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $4.5\ \text{V}$		7	10	nC
$Q_{gs}$	Gate to Source Charge			3.3		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			2.0		nC

### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}, I_S = 2.1\ \text{A}$ (Note 2)		0.76	1.1	V
		$V_{GS} = 0\ \text{V}, I_S = 13.2\ \text{A}$ (Note 2)		0.85	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 13.2\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		23	37	ns
$Q_{rr}$	Reverse Recovery Charge			7	14	nC
$t_{rr}$	Reverse Recovery Time	$I_F = 13.2\ \text{A}, di/dt = 300\ \text{A}/\mu\text{s}$		18	33	ns
$Q_{rr}$	Reverse Recovery Charge			14	26	nC

Notes:

- $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a) 50 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



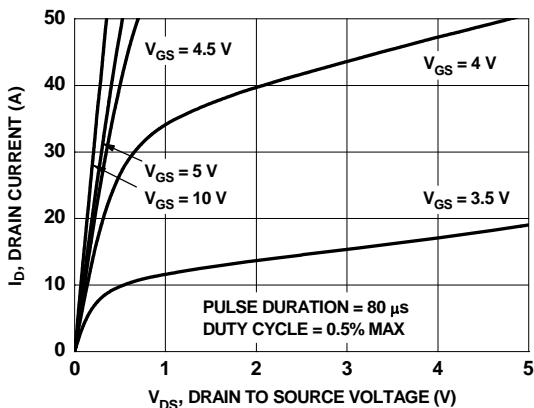
b) 125 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

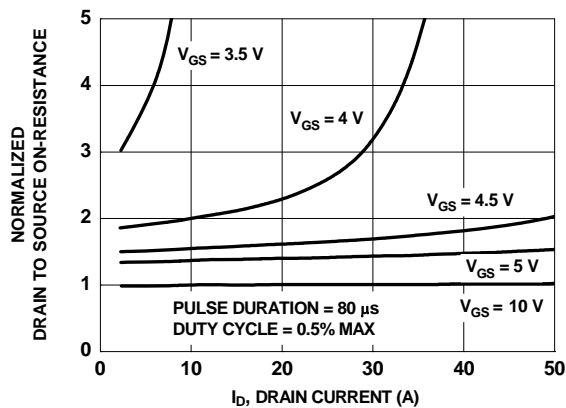
3.  $E_{AS}$  of 21 mJ is based on starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.3\ \text{mH}$ ,  $I_{AS} = 12\ \text{A}$ ,  $V_{DD} = 27\ \text{V}$ ,  $V_{GS} = 10\ \text{V}$ . 100% test at  $L = 0.1\ \text{mH}$ ,  $I_{AS} = 20\ \text{A}$ .

4. As an N-ch device, the negative  $V_{GS}$  rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

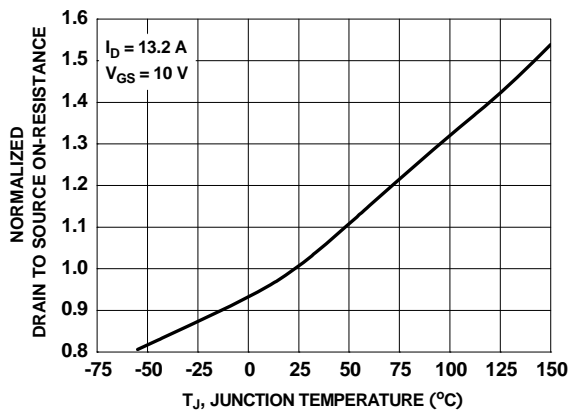
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



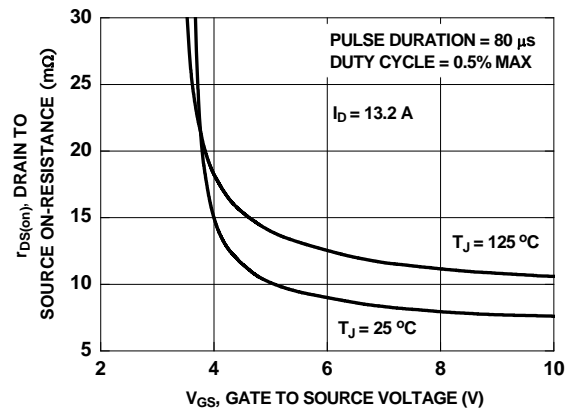
**Figure 1. On Region Characteristics**



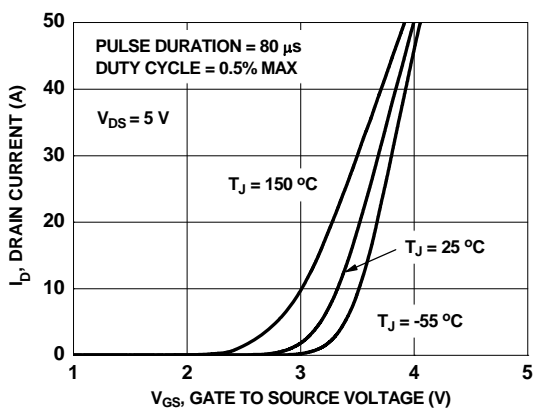
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



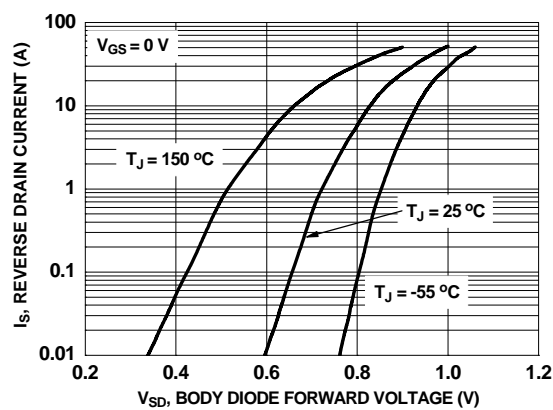
**Figure 3. Normalized On Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

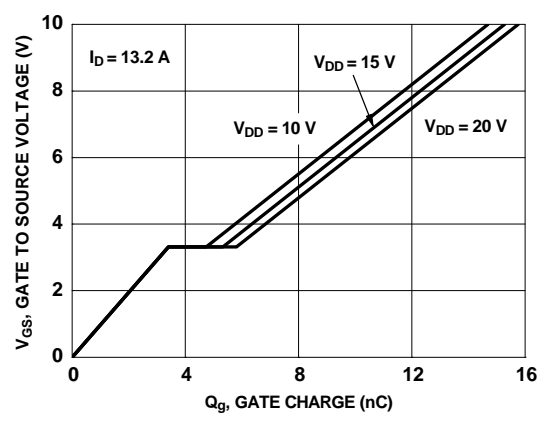


**Figure 5. Transfer Characteristics**

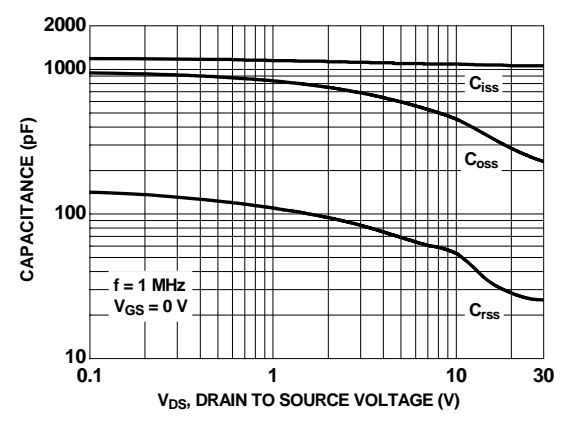


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

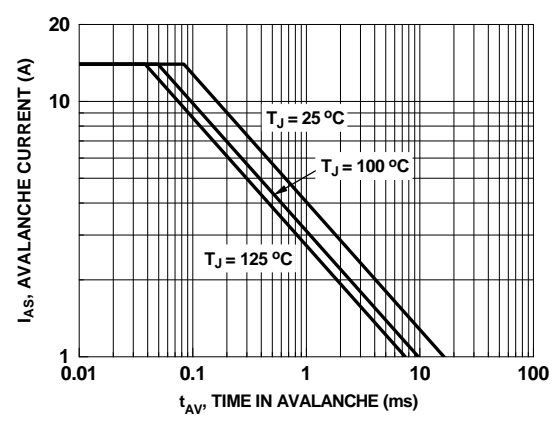
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



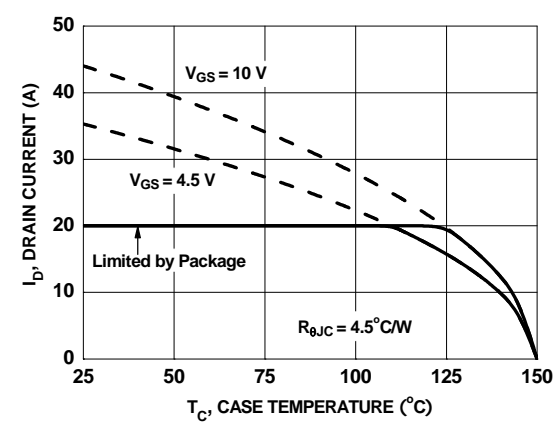
**Figure 7. Gate Charge Characteristics**



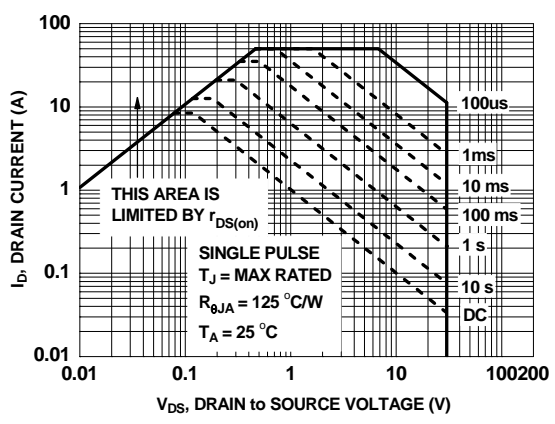
**Figure 8. Capacitance vs Drain to Source Voltage**



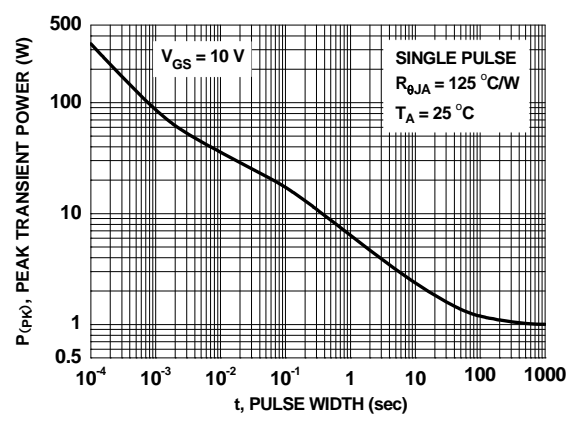
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

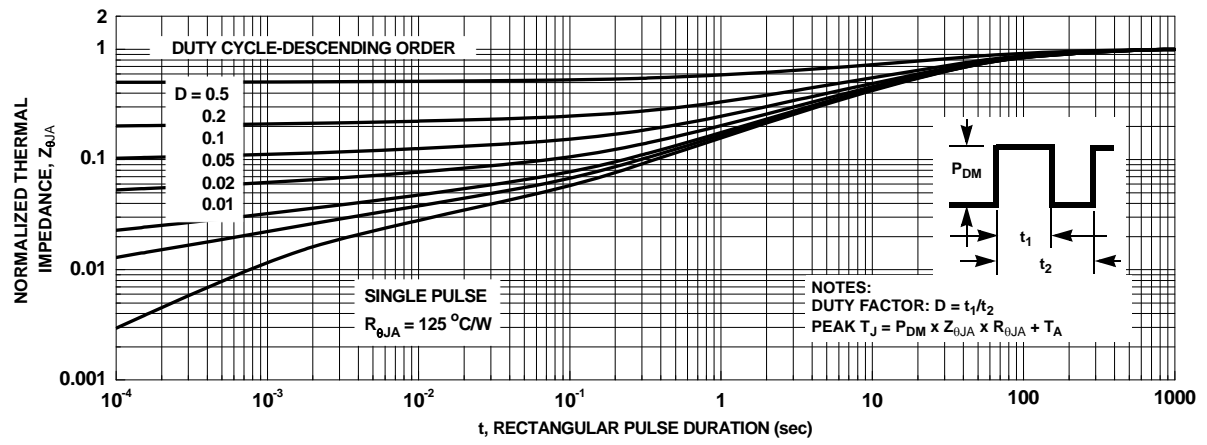


**Figure 11. Forward Bias Safe Operating Area**



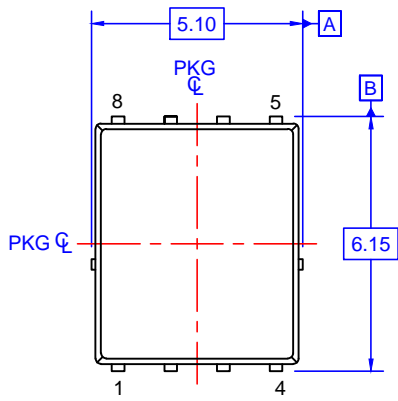
**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

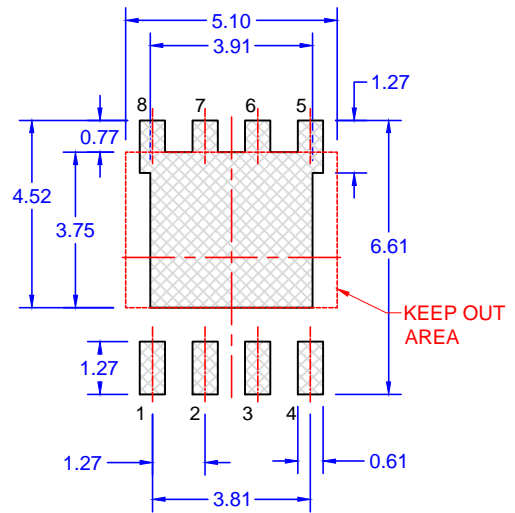
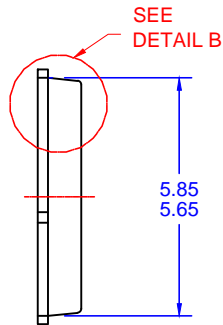


**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**

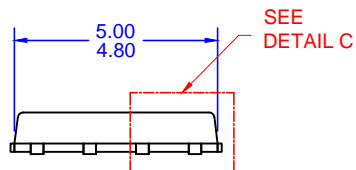
PQFN8 5X6, 1.27P  
CASE 483AE  
ISSUE A



TOP VIEW

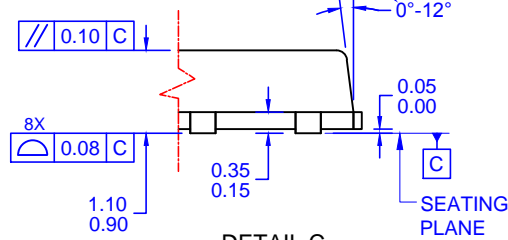


LAND PATTERN RECOMMENDATION

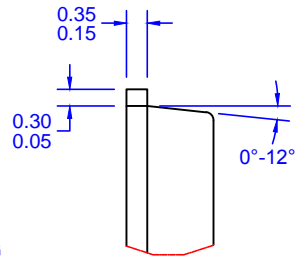


SIDE VIEW

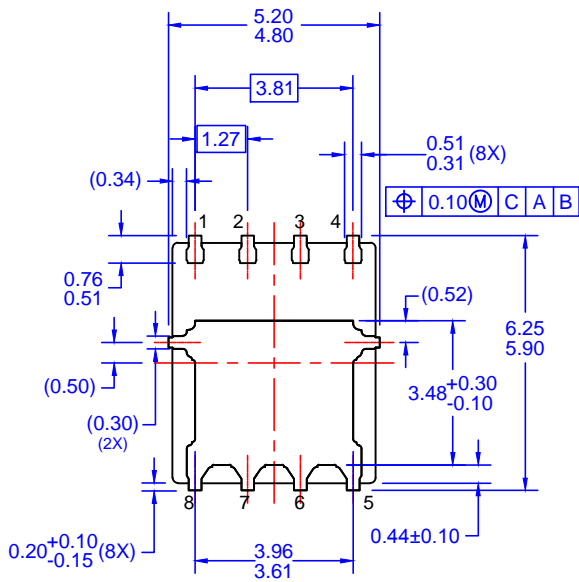
OPTIONAL DRAFT ANGLE MAY APPEAR ON FOUR SIDES OF THE PACKAGE



DETAIL C  
SCALE: 2:1



DETAIL B  
SCALE: 2:1



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

- A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA.
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

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