

FEATURES

- Two independent differential 2:1 multiplexers
- Guaranteed AC performance over temperature and voltage:
 - DC-to >10.7Gbps data rate throughput
 - < 290ps IN-to-Out t_{pd}
 - < 80ps t_r / t_f
- Unique, patent-pending input isolation design minimizes crosstalk
- Ultra-low jitter design:
 - <1ps_{RMS} random jitter
 - <10ps_{pp} deterministic jitter
 - <10ps_{pp} total jitter (clock)
 - <0.7ps_{RMS} crosstalk-induced jitter
- Unique, patent-pending 50 Ω input termination and VT pin accepts DC-coupled and AC-coupled inputs (CML, LVDS, PECL)
- 400mV LVPECL output swing
- Power supply 2.5V $\pm$ 5% or 3.3V $\pm$ 10%
- -40°C to +85°C temperature range
- Available in 32-pin (5mm $\times$ 5mm) MLF® package



Precision Edge®

DESCRIPTION

The SY58027U features two ultra-fast, low jitter 2:1 differential muxes with a guaranteed maximum data throughput of 10.7Gbps.

The SY58027U differential inputs include a unique internal termination design that allows access to the termination network through a VT pin. The device easily interfaces to different logic standards, both AC- and DC-coupled, without external resistor-bias and termination networks. The result is a clean, stub-free, low jitter interface solution. The differential 400mV LVPECL outputs have extremely fast rise/fall times guaranteed to be less than 80ps.

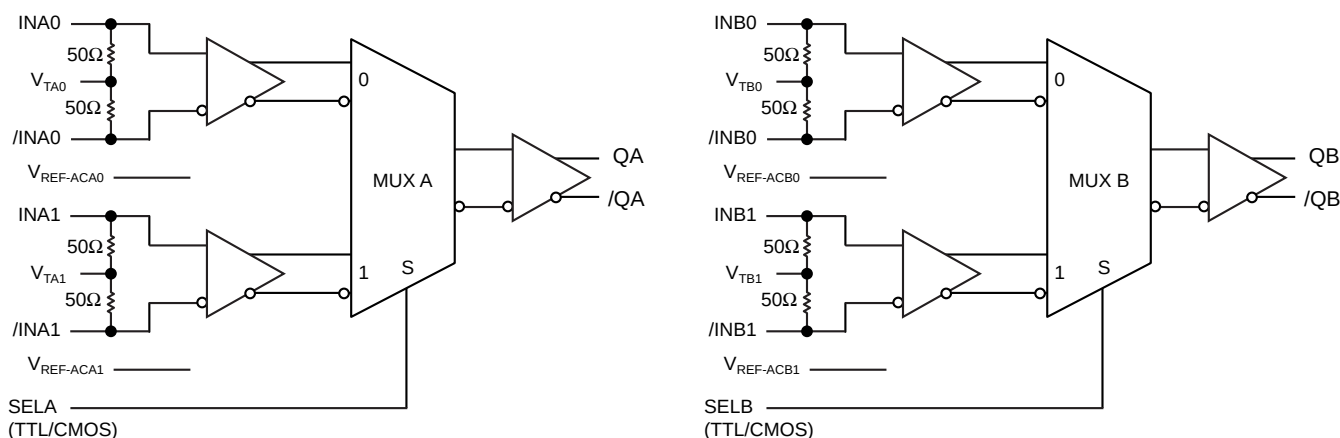
The SY58027U operates from a 2.5V or 3.3V supply and is guaranteed over the full industrial temperature range (-40°C to +85°C). The SY58027U is part of Micrel's Precision Edge® product family.

All support documentation can be found on Micrel's web site at www.micrel.com.

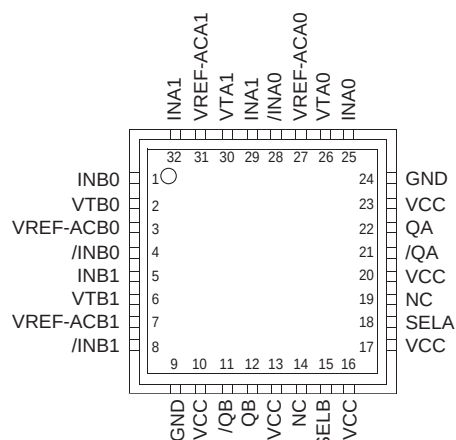
APPLICATIONS

- Data communication systems
- All SONET OC3-OC768 applications
- All Fibre Channel applications
- All GigE applications

FUNCTIONAL BLOCK DIAGRAM



PACKAGE/ORDERING INFORMATION



32-Pin MLF® (MLF-32)

Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY58027UMI	MLF-32	Industrial	SY58027U	Sn-Pb
SY58027UMITR ⁽²⁾	MLF-32	Industrial	SY58027U	Sn-Pb
SY58027UMG ⁽³⁾	MLF-32	Industrial	SY58027U with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY58027UMGTR ^(2, 3)	MLF-32	Industrial	SY58027U with Pb-Free bar-line indicator	Pb-Free NiPdAu

Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25^\circ\text{C}$, DC electricals only.
2. Tape and Reel.
3. Pb-Free package recommended for new designs.

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
25, 28, 29, 32, 1, 4, 5, 8	INA0, /INA0, INA1, /INA1, INB0, /INB0, INB1, /INB1	Differential Inputs: These input pairs are the differential signal inputs to the device. Inputs accept AC- or DC-coupled differential signals as small as 100mV. Each pin of a pair internally terminates to a VT pin through 50 Ω . Note that these inputs will default to an indeterminate state if left open. Unused differential input pairs can be terminated by connecting one input to V_{CC} and the complementary input to GND through a 1k Ω resistor. The VT pin is to be left open in this configuration. Please refer to the "Input Interface Applications" section for more details.
26, 30, 2, 6	VTA0, VTA1, VTB0, VTB1	Input Termination Center-Tap: Each side of the differential input pair, terminates to a VT pin. Each VT pin provides a center-tap to a termination network for maximum interface flexibility. See "Input Interface Applications" section for more details.
18, 15	SELA, SELB	Bank A, Bank B Input Channel Select (TTL/CMOS): These TTL/CMOS-compatible inputs select the inputs to the multiplexers. These inputs are internally connected to a 25k Ω pull-up resistor and will default to a logic HIGH state if left open. Input switching threshold is $V_{CC}/2$.
27, 31, 3, 7	VREF-ACA0, VREF-ACA1, VREF-ACB0, VREF-ACB1	Reference Output Voltage: These outputs bias to $V_{CC} - 1.2\text{V}$. Connect to VT pin when AC-coupling the data inputs. Bypass with 0.01 μF low ESR capacitor to V_{CC} . Maximum current source or sink is 0.5mA. See "Input Interface Applications" section.
10, 13, 16, 17, 20, 23	VCC	Positive Power Supply: Bypass with 0.1 μF ™ 0.01 μF low ESR capacitors.
22, 21, 12, 11	QA, /QA, QB, /QB	Differential 100k LVPECL Outputs: MUX A and MUX B selected LVPECL outputs. See "Output Interface Applications" section for termination. Refer to the "Truth Table" for logic operation.
9, 24	GND, Exposed pad	Ground: Ground pins and exposed pad must be connected to the same ground plane.
14, 19	NC	Not connected.

Absolute Maximum Ratings⁽¹⁾

Power Supply Voltage (V_{CC})	–0.5V to +4.0V
Input Voltage (V_{IN})	–0.5V to V_{CC}
LVPECL Output Current (I_{OUT})	
Continuous	50mA
Surge	100mA
Termination Current ⁽³⁾	
Source or sink current on V_T	±100mA
Input Current	
Source or sink current on IN, /IN	±50mA
Current (V_{REF-AC})	
Source or sink current on V_{REF-AC} ⁽³⁾	±1.5mA
Lead Temperature (soldering, 20 sec.)	260°C
Storage Temperature Range (T_S)	–65°C to +150°C

Operating Ratings⁽²⁾

Power Supply Voltage (V_{CC})	+2.375V to +2.625V
	+3.0V to +3.6V
Ambient Temperature Range (T_A)	–40°C to +85°C
Package Thermal Resistance	
MLF® (θ_{JA})	
Still-Air	35°C/W
500lpfm	28°C/W
MLF® (ψ_{JB}) ⁽⁴⁾	
Junction-to-board	20°C/W

DC ELECTRICAL CHARACTERISTICS⁽⁵⁾

T_A = –40°C to +85°C; Unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply	$V_{CC} = 2.5V$ $V_{CC} = 3.3V$	2.375 3.0	2.5 3.3	2.625 3.6	V
I_{CC}	Power Supply Current	No load, max. V_{CC} .		100	140	mA
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		80	100	120	Ω
R_{IN}	Input Resistance (IN-to- V_T , /IN-to- V_T)		40	50	60	Ω
V_{IH}	Input High Voltage (IN, /IN)	Note 6	$V_{CC}-1.6$		V_{CC}	V
V_{IL}	Input Low Voltage (IN, /IN)		0		$V_{IH}-0.1$	V
V_{IN}	Input Voltage Swing (IN, /IN)	See Figure 1a.	0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage Swing IN – /IN	See Figure 1b.	0.2			V
$V_{T\ IN}$	In to V_T (IN, /IN)				1.28	V
V_{REF-AC}	Output Reference Voltage		$V_{CC}-1.3$	$V_{CC}-1.2$	$V_{CC}-1.1$	V

Notes:

1. Permanent device damage may occur if ratings in the “Absolute Maximum Ratings” section are exceeded. This is a stress rating only and functional operation is not implied for conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Due to the limited drive capability, use for input of the same package only.
4. Junction-to-board resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential (GND) on the PCB. ψ_{JB} uses 4-layer θ_{JA} in still air unless otherwise stated.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6. V_{IH} (min) not lower than 1.2V.

LVPECL OUTPUTS DC ELECTRICAL CHARACTERISTICS⁽⁶⁾

$V_{CC} = 2.5V \pm 5\%$ or $3.3V \pm 10\%$; $T_A = -40^\circ C$ to $+85^\circ C$; $R_L = 50\Omega$ to $V_{CC}-2V$, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage Q, /Q		$V_{CC}-1.145$	—	$V_{CC}-0.895$	V
V_{OL}	Output LOW Voltage Q, /Q		$V_{CC}-1.545$	—	$V_{CC}-1.295$	V
V_{OUT}	Output Voltage Swing Q, /Q	See Figure 1a.	150	400		mV
$V_{DIFF-OUT}$	Differential Output Voltage Swing Q-/Q	See Figure 1b.	300	800		mV

LVTTTL/CMOS DC ELECTRICAL CHARACTERISTICS⁽⁶⁾

$V_{CC} = 2.5V \pm 5\%$ or $3.3V \pm 10\%$; $T_A = -40^\circ C$ to $85^\circ C$ unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current		-175		75	μA
I_{IL}	Input LOW Current	$V_{IL} = 0V$	-300			μA

Note:

6. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC ELECTRICAL CHARACTERISTICS⁽⁷⁾

$V_{CC} = 2.5V \pm 5\%$ or $3.3V \pm 10\%$; $T_A = -40^\circ C$ to $+85^\circ C$; $R_L = 50\Omega$ to $V_{CC} - 2V$, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	NRZ Data Clock $V_{OUT} \geq 200mV$	10.7	7		Gbps GHz
t_{pd}	Propagation Delay IN-to-Q	$V_{IN} \geq 300mV$	140	215	290	ps
	SEL-to-Q		100	220	400	ps
t_{SKEW}	Input-to-Input Skew (Within-bank)	Note 8		6	15	ps
	Bank-to-Bank Skew	Note 9		8	20	ps
	Part-to-Part Skew	Note 10			100	ps
t_{JITTER}	Data Random Jitter (RJ)	Note 11			1	ps _{RMS}
	Deterministic Jitter (DJ)	Note 12			10	ps _{PP}
	Clock Cycle-to-Cycle Jitter (RJ)	Note 13			1	ps _{RMS}
	Total Jitter (TJ)	Note 14			10	ps _{PP}
	Crosstalk-Induced Jitter Channel-to-Channel	Note 15 , Within-bank.			0.7	ps _{RMS}
t_r, t_f	Output Rise/Fall Time 20% to 80%	At full swing.	20	55	80	ps

Notes:

- High-speed AC parameters are guaranteed by design and characterization. V_{IN} swing $\geq 100mV$ unless otherwise noted.
- Input-to-input skew is the difference in time between two inputs to the output within a bank.
- Bank-to-bank skew is the difference in time from input to the output between bank.
- Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.
- Random jitter is measured with a K28.7 comma detect character pattern, measured at 5Gbps and 2.5Gbps/3.2Gbps.
- Deterministic jitter is measured at 2.5Gbps/3.2Gbps, with both K28.5 and 2²³-1 PRBS pattern.
- Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, $T_n - T_{n-1}$ where T is the time between rising edges of the output signal.
- Total jitter definition: with an ideal clock input of frequency - f_{MAX} , no more than one output edge in 10¹² output edges will deviate by more than the specified peak-to-peak jitter value.
- Crosstalk is measured at the output while applying two similar frequencies that are asynchronous with respect to each other at the inputs.

TRUTH TABLES

INA0	/INA0	INA1	/INA1	SELA	QA	/QA
0	1	X	X	0	0	1
1	0	X	X	0	1	0
X	X	0	1	1	0	1
X	X	1	0	1	1	0

INB0	/INB0	INB1	/INB1	SELB	QB	/QB
0	1	X	X	0	0	1
1	0	X	X	0	1	0
X	X	0	1	1	0	1
X	X	1	0	1	1	0

SINGLE-ENDED AND DIFFERENTIAL SWINGS

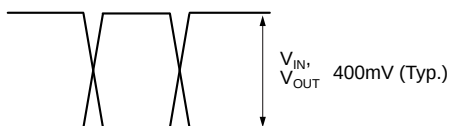


Figure 1a. Single-Ended Voltage Swing

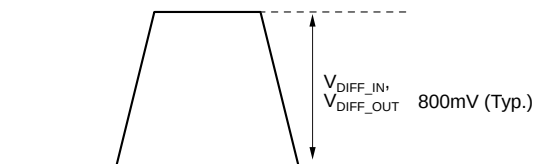
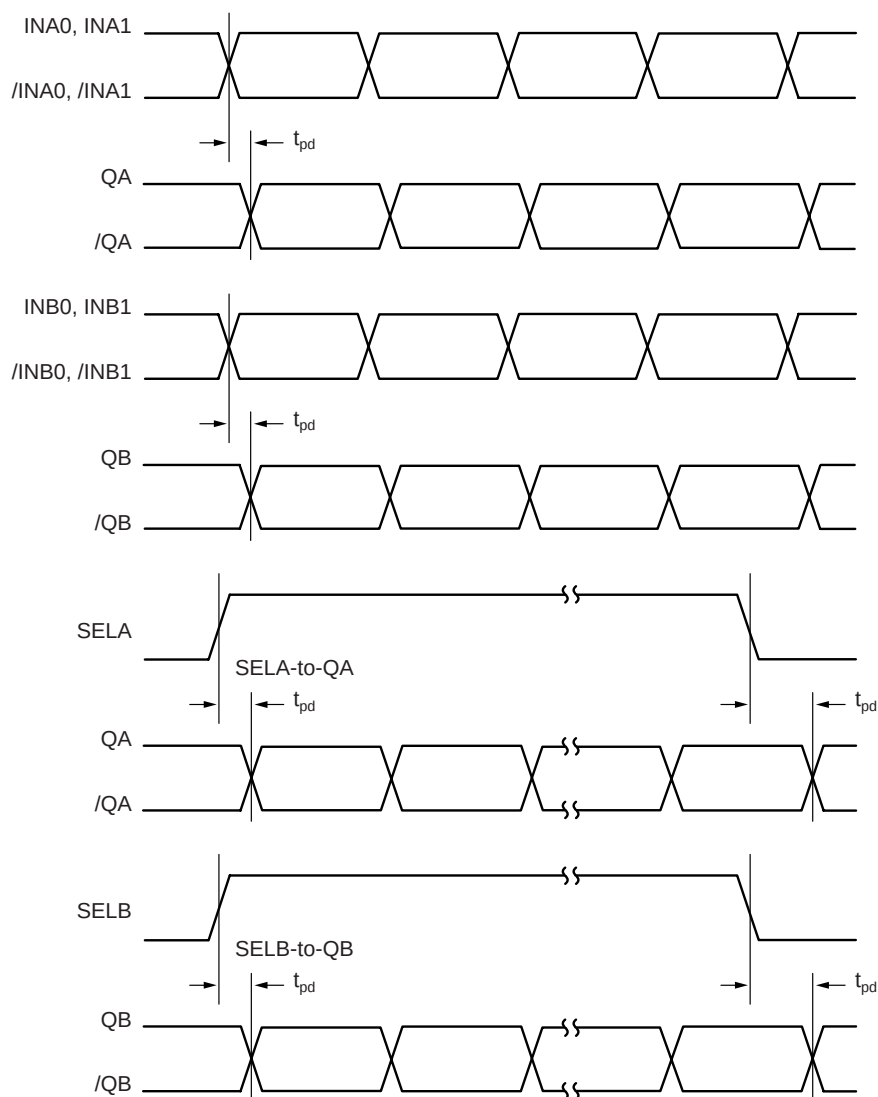


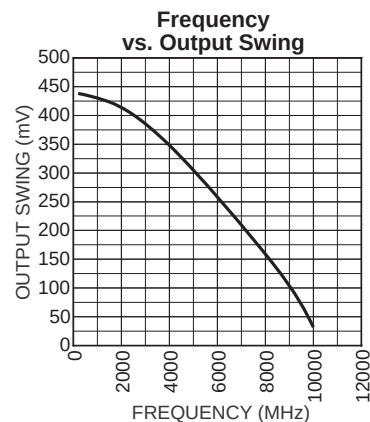
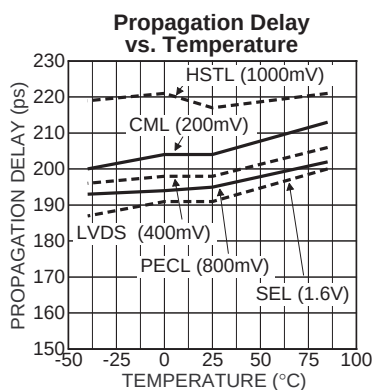
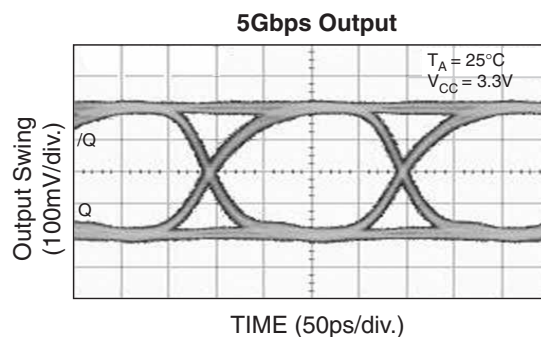
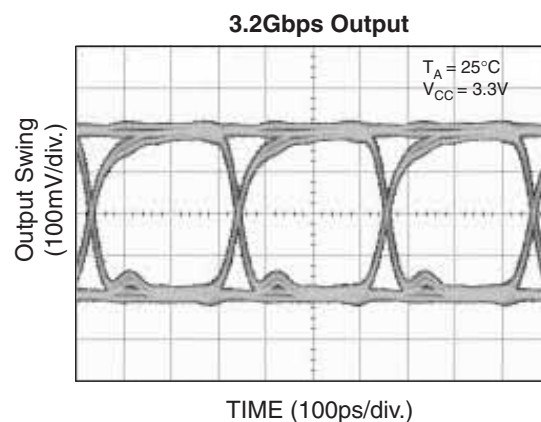
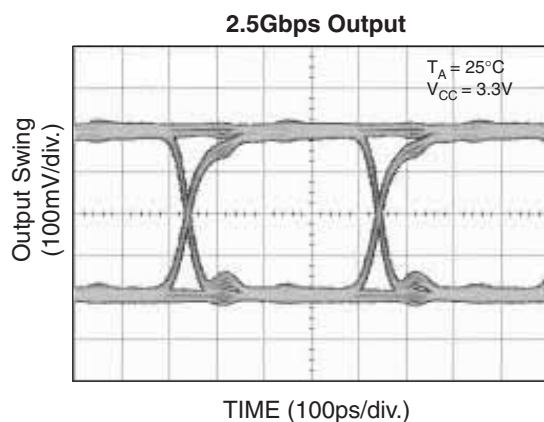
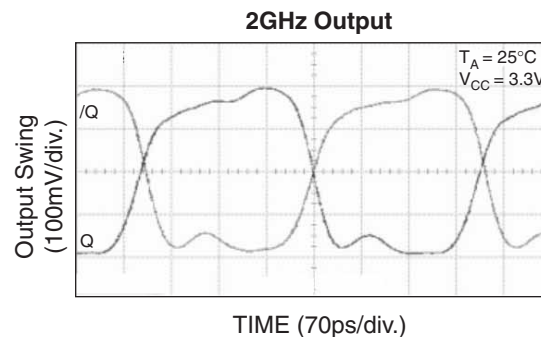
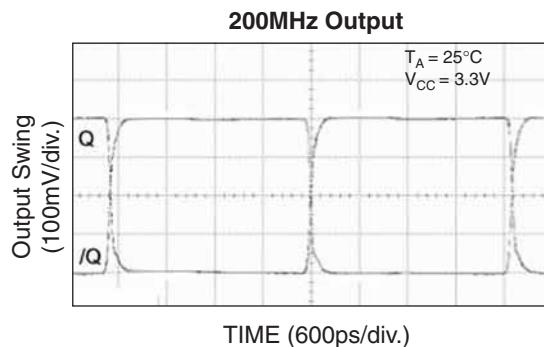
Figure 1b. Differential Voltage Swing

TIMING DIAGRAM



TYPICAL OPERATING CHARACTERISTICS

$V_{CC} = 3.3V$, $T_A = 25^\circ C$, $R_L = 50\Omega$ to $V_{CC} - 2V$, DC coupled, unless otherwise stated.



The diagram shows a differential pair of NMOS transistors. The gates of both transistors are connected to an input signal labeled 'IN'. The sources of both transistors are connected to a common source node, which is connected to ground (GND) through a current source represented by a circle with a downward arrow. The drains of the two transistors are connected to a supply voltage V_{CC} through resistors. The output of the differential pair is taken from the drains, with one output labeled 'OUT' and the other labeled 'OUT' (implied). The input signal 'IN' is also connected to a voltage divider consisting of two 50Ω resistors, with the input voltage labeled V_T and the input signal labeled 'IN'.

The diagram shows a differential pair of NPN BJTs. The emitters of both transistors are connected to a common node, which is then connected to ground through a resistor labeled R_{EE} . The bases of the transistors are connected to a common bias voltage V_{CC} . The collectors are connected to a common load resistor R_C , which is also connected to V_{CC} . The output signals are taken from the collectors, labeled I_C and Q .

For $V_{CC} = 3.3V$, $R_p = 50\Omega$.
 For $V_{CC} = 2.5V$, $R_p = 19\Omega$.

For $V_{CC}=3.3V$, $R_p = 100\Omega$.
 For $V_{CC}=2.5V$, $R_p = 50\Omega$.

8

OUTPUT INTERFACE APPLICATIONS

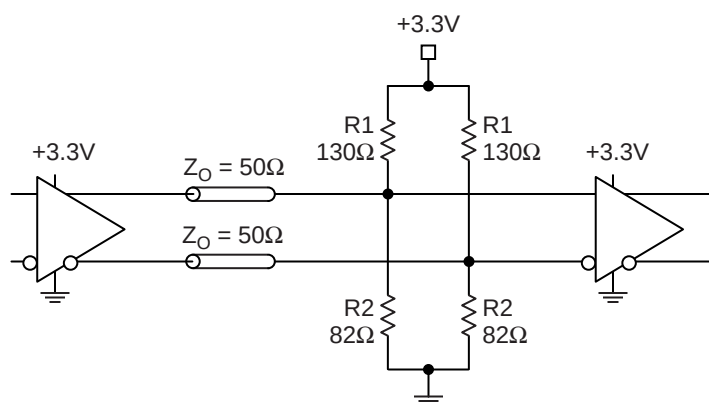


Figure 4a. Parallel Thevenin-Equivalent Termination

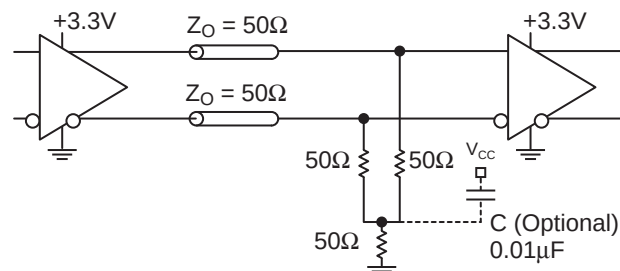


Figure 4b. Parallel Termination (3-Resistor)

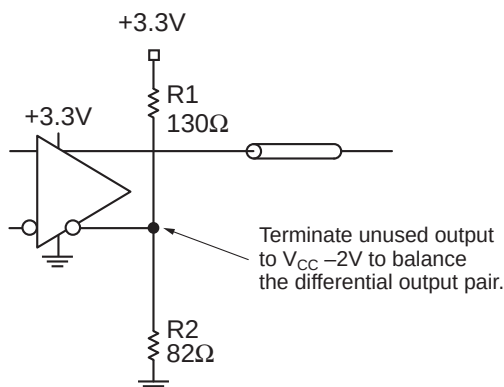
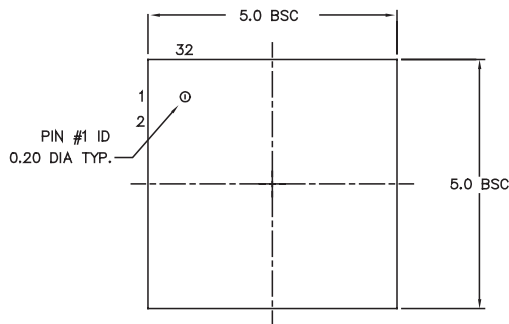


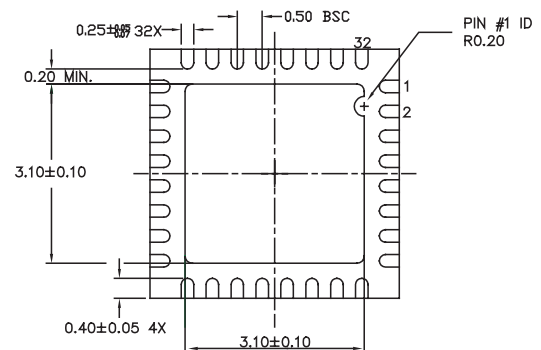
Figure 4c. Terminating Unused Output

RELATED MICREL PRODUCTS AND SUPPORT DOCUMENTATION

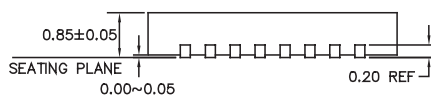
Part Number	Function	Data Sheet Link
SY58016L	3.3V 10Gbps Differential CML Line Driver/Receiver with Internal Termination	http://www.micrel.com/product-info/products/sy58016l.shtml
SY58017U	10.7Gbps Differential CML 2:1 MUX with Internal Termination	http://www.micrel.com/product-info/products/sy58017u.shtml
SY58018U	5Gbps LVPECL 2:1 MUX with Internal Termination	http://www.micrel.com/product-info/products/sy58018u.shtml
SY58019U	10.7Gbps 400mV LVPECL 2:1 MUX with Internal Termination	http://www.micrel.com/product-info/products/sy58019u.shtml
SY58025U	10.7Gbps Dual 2:1 CML MUX with Internal Termination	http://www.micrel.com/product-info/products/sy58025u.shtml
SY58026U	5Gbps Dual 2:1 LVPECL MUX with Internal Termination	http://www.micrel.com/product-info/products/sy58026u.shtml
SY58051U	10.7Gbps AnyGate® with Internal Input and Output Termination	http://www.micrel.com/product-info/products/sy58051u.shtml
SY58052U	10Gbps Clock/Data Retimer with 50Ω Input Termination	http://www.micrel.com/product-info/products/sy58052u.shtml
	MLF™ Application Note	www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

32-PIN MicroLeadFrame® (MLF-32)

TOP VIEW

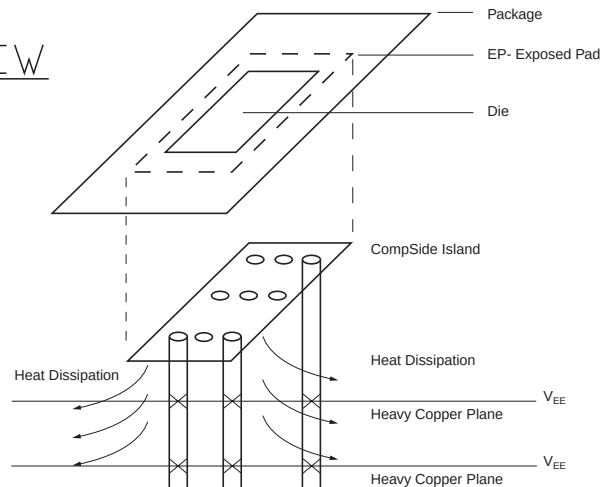


BOTTOM VIEW



SIDE VIEW

- NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
 2. MAX. PACKAGE WARPAGE IS 0.05 mm.
 3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
 4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



PCB Thermal Consideration for 32-Pin MLF® Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

1. Package meets Level 2 Moisture Sensitivity Classification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

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